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Design of Low Power Low Offset Dynamic latch Comparator using DTMOS Technique

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Abstract: *Analog to Digital converters plays an essential role in signal processing and medical applications. SAR ADC is best suited for biomedical applications because of its low power and medium resolution. Low power dynamic comparators are essentially desired in the design of SAR ADC. In this paper, a lowpower dynamic type latch comparator is designed which is based on Dynamic Threshold Metal Oxide Semiconductor (DTMOS) technique to reduce the power dissipation which is achieved by reducing the supply voltage. The circuit has been implemented atthe supply voltage of 0.8 V. The simulations for this comparator are carried out in CADENCE SPECTRE using 45nm CMOS technology. The simulation outcomes validate that the designed dynamic latch comparator with DTMOS techniques is 20% morepower saving in comparison to the conventional comparator. Thetotal power consumption is as low as 156.18nW which makes it suitable for low-power bio-medical applications.*

Keywords: Dynamic latch comparator, Low power, SAR- ADC, DTMOS..

I. INTRODUCTION

The vital demand of low-power mixed mode devices like Analog to digital converters (ADCs) [15] has enforced the design of low power [24], [17]. Various portable and small feature sized electronic devices which are used in medical systems require ADCs with low power and fast switchingspeed [20]. The dominant block of ADC is comparator, which determines the overall performance of ADC. So as to enhance the battery life and accuracy of ADC, the comparator must be of high speed and energy efficient.The comparator predominantly incorporates two stages, firstone is a reset stage and the second one is a comparing stage. The one of most eminent standard for deducting power consumption is to scale down the input voltage supply, since in CMOS circuits average power consumption is square of the input supply voltage.

$$P = Vdd^2 I_d$$

As the CMOS technology is down scaling, the problem of low voltage has occurred in case of low power -high speed comparators, because the threshold voltage is not scaledwith respect to the supply voltage [24]. This constrains the voltage head room [25] as well as Input Common Mode Range (ICMR). Also, the offset of CMOS devices which is causedby the mismatches in capacitance and current factor, approx- imately doubles for every process variation below 100nm CMOS technology [9]. Thus it has become a major challenge to design a high speed low-power comparator in the design of ADC.

Comparators with various design techniques have been proposed to meet the accuracy and the overall performance requirements of ADCs [22]. The various techniques are as such fully differential approach [22], body driven technique [26]- [16], offset cancellation technique [7]- [12], zero thresh- old voltage MOS based technique [21] and supply voltage boosting method [11] etc. These techniques are absolutely satisfactory but not supportive for low supply voltage at Ultra Deep Submicron (UDSM) CMOS technology. These drawbacks of low power consumption are overcome by design the comparator circuit with DTMOS technique.

When compared to the static type comparators, dynamic comparators exploits dynamic bias and positive feedback, because of which they provide low static power consumption [11]

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II. DTMOS TECHNIQUE

In the recent days the size of the transistor is reducing, because of this reduced size of MOS transistor, it demands the lower supply voltage [10]. In fields of biomedical deviceslike EEG, ECG, EMG portable monitoring systems requires minimum sized batteries, therefore low voltage low power circuits are required. This can be achieved by reducing the supply voltage, but this will effectively degrade the signal quality, output resistance of MOS transistor and voltage gain. Hence So LVLP (Low Voltage Low Power) techniques have been developed in CMOS technology [2], [19], [5], [13], [8]. One of the LVLP term is DTMOS (Dynamic Threshold MOS) transistor. DTMOS was first suggested by [4], [23]. DTMOS transistor have the ability to dynamically regulate the threshold voltage (V_{th}) of transistor, using body biasing technique.

In DTMOS technique, threshold voltage can be reduced by connecting together the gate of the MOS transistor to its body. This meaningfully enhances the current drive of the DTMOS [1], [18].

Figures 1 ans 2. show the DTMOS structures for NMOS and PMOS transistors. When DTMOS transistor is in conduction (ON), its threshold voltage (Vt) decreases and driving current increases, propagation delay decreases. On the other hand, if a DTMOS transistor is not conducting(OFF), then the threshold voltage increases, leakage current decreases and thus power consumption also decreases. In this paper, a dynamic latch comparator is designed with DTMOS technique and compared it with the conventional dynamic latch comparator. The design is simulated using 45 nm CMOS technology.

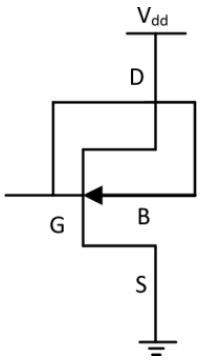

Fig. 1. n-MOSFET structure of DTMOS

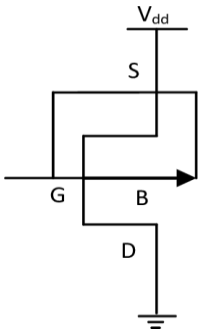

Fig. 2. p- MOSFET structure of DTMOS

III. EXISTING DESIGN OF DYNAMIC LATCH COMPARATORCIRCUIT DESCRIPTION

The schematic diagram of conventional dynamic latch type comparator is illustrated in Fig.3, where the comparator is designed and simulted in 180nm CMOS technology. CLK1 is the level shifted signal of CLK with a delay of nearly 90ps. This comparator operates in two phases. In reset phase i.e., when clock is LOW, the transistors M6, M7, M0, M1 and VDD are ON, and M2 and M3 are OFF. The input nodes are discharge to ground via transistors M6 and M7, and nodesOUTp AND OUTn are charged to VDD via transistor M0 andM1.

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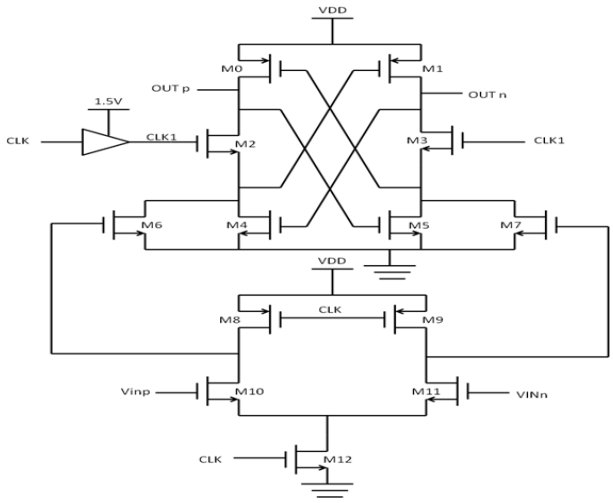

Fig. 3. Schematic of conventional Dynamic Latch Comparator (DLC)

When the clock goes HIGH, the reset transistors are switched OFF and the currents starts flowing in M12 as well as in the differential pair. Based on the input voltage, one of the cross-coupled inverters M0, M1, M4, M5, that makes the regeneration, receives large current, which determines the final output state. when regeneration is finished, one of the output node is at VDD; the next output and both the drains of the differential pair have a 0-V potential. In this context, there is no supply current and hence power efficiency is maximized.

While the drain voltage of any one of the transistors falls below VDD- IVth I, NMOS transitor of the inverter will turn ON and output node will start to discharge ; positive feedback is turned ON. When the output reaches VDD- IVth I PMOS transistor of another inverter will turn ON. Consequently output is regenerated and after the regeneration phase one of the output is logic ‘0’ and the other is logic ‘1’. Fig.4 shows that power consumption of the conventional circuit is 39.516µW.

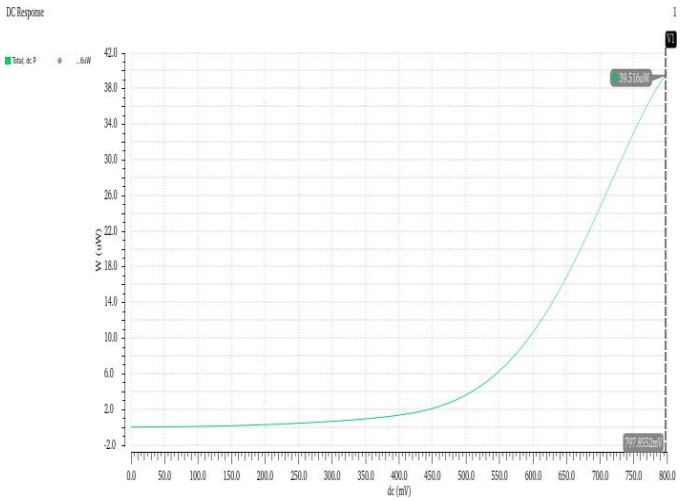

Fig. 4. Power consumption of conventional Dynamic Latch Comparator

IV. PROPOSED DESIGN OF DTMOS DYNAMIC LATCH COMPARATOR

4.1 Circuit Description

Fig. 5 Shows the design of proposed dynamic latch com- parator using dynamic threshold MOS transistor logic. The circuit is redesigned at 45nm CMOS technology. The main objective of redesigning the circuit at 45nm CMOS process this circuit is to reduce the power consumption. So the technique of DTMOS which is a low power technique is utilized in implementing a low power dynamic latch comparator. The proposed dynamic comparator also operates like a conventional circuit at two stages. In first stage i.e. when the clock is logic '0' the transistors of M1/M6 and M2/M5 are

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reset the output node and drain of the various transistors M9/M10 are connected to VDD. The tail transistor M11 is OFF and no supply current remains. When the clock logic '1' the reset transistors are turned OFF and theflows begins streaming in M11 as well as in the differential pair. In view of the input voltage, one of the cross- coupled inverters M7/M3 or M8/M4 that makes the recovery, gets huge current, which decides the last output state. at thepoint when recovery is done, one of the output node is at VDD; the following output and both the channels of the differential pair have a 0-V potential. In this unique situation, there is no stockpile current and henceforth power effectiveness is expanded. While the channel voltage of any of the transistors falls underneath VDD-|Vth|, NMOS transistor of the inverter will turn ON and output node will begin to release ; positive input is turned ON. At the point when the output arrives at VDD-|Vth| PMOS transistor of another inverter will turn ON. Subsequently output is recovered and after the recovery stage one of the output is rationale '0' and the other is rationale '1'. In this process the supply voltage is divided at the transistors of M7/M8 and M9/M10 here the half of the supply voltage will be flowing and that design operates in that supply voltage

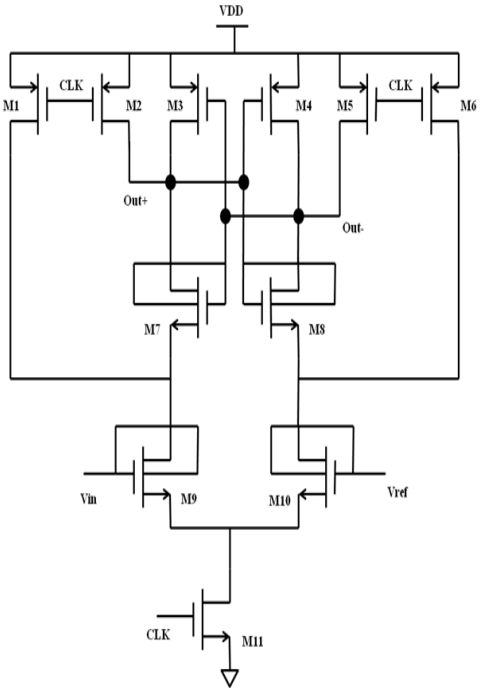

Fig. 4. Schematic diagram of proposed DTMOS- Dynamic Latch Comparator

TABLE.1 TRANSISTOR ASPECT RATIOS IN THE PROPOSED DYNAMIC LATCHCOMPARATOR

Transistor ID	Aspect Ratios (µm)
M1,2	18/0.26
M3,4	0.9/0.26
M5,6	0.45/0.26
M7,8,9,10	0.9/0.26
M11	0.45/0.26

Potential dividing theorem is used to find the values of R1 andR2. The technique of DTMOS is applied in NMOS and PMOS pairs to reduce the total power consumption.

Applying potential dividing concept in NMOS and PMOS pairs, dynamic threshold voltage is determined.

$$V \times R2 / R1 + R2$$

From the DC response of the proposed circuit we can state that power consumption is reduced to 156.18nW of power consumption reduced by employing the DTMOS technique.

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V. SIMULATION RESULTS AND DISCUSSION

The proposed dynamic latch comparator with Dynamic Threshold MOS (DTMOS) is compared with the existing dynamic latch comparator using SPECTRE simulator in CADENCE at 45nm CMOS process at VDD = 0.8 V. The samesimulation environment is used to make a fair comparison.

Figures below depict the comparison of power dissipation of existing and proposed comparator circuits. Fig. 5 shows the transient response of the proposed circuit

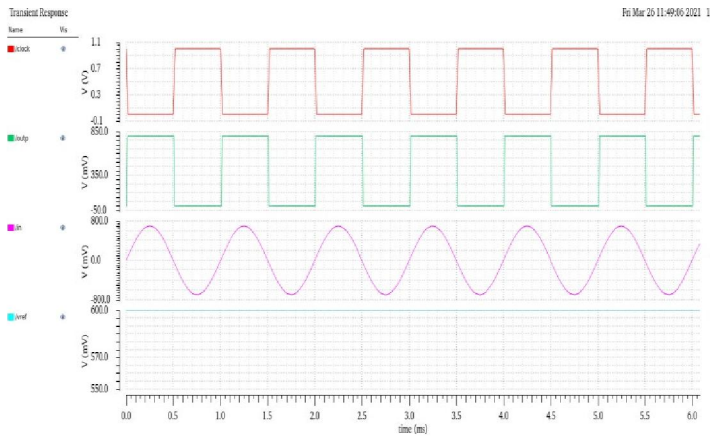

Fig.5. **Transient response of dynamic latch comparator**

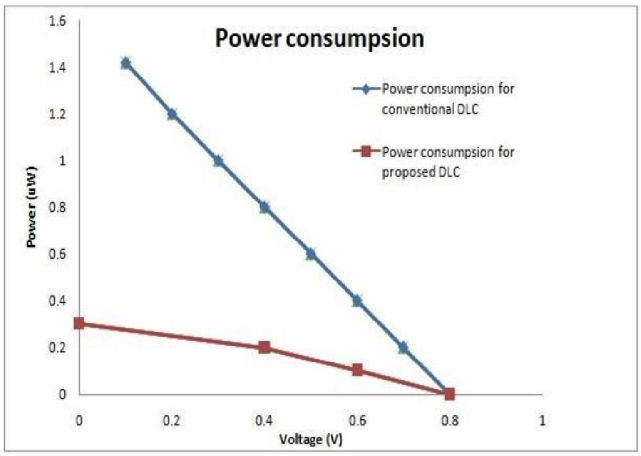

Fig. 6. Power consumption versus voltage of proposed DTMOS and Conventional Dynamic Latch Comparator

Fig. 6 shows that power dissipation is lower compared to the existing circuit without affecting the performance of the circuit.

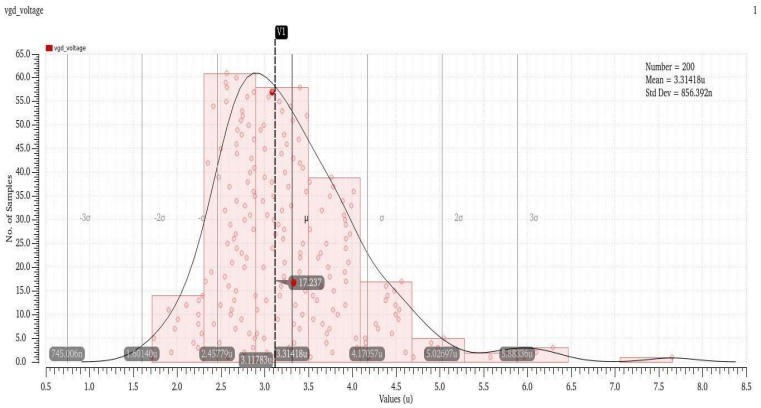

Fig.7. Monte Carlo Simulation Of The Dynamic Bias Latch Comparator

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Fig. 7 shows the standard deviation of the offset of the proposed comparator, that is 856.392nV using Monte Carlo Simulations for a run of 200 samples. Based on the simulation results, Table-I presents the comparison between the proposed and other two dynamic comparators.

TABLE-II PERFORMANCE COMPARISON OF PROPOSED COMPARATOR WITH AN EXISTING COMPARATOR

Parameters	[1]	[2]	Proposed
CMOS Technology	180nm	45nm	45nm
Supply voltage	1.8V	0.8V	0.8V
Power consumption	72.2µW	39.516µW	156.18nW
Delay	268ps	-	105.6µs

VI. CONCLUSION

A low power dynamic latch comparator design is presented in this paper to decline the supply voltage and power consumption. The structure of the existing comparator circuit is modified by applying dynamic threshold MOS technique. The simulation results approve the reduction in input supply voltage and power consumption as well in comparison with the existing comparator. The proposed comparator dissipates very less power of 156.18nW at a supply voltage of 0.8V.

VII. FUTURE SCOPE

The proposed dynamic latch comparator was designed with the objective of decreasing the power. A low power technique called a Dynamic Threshold MOS (DTMOS) technique is implemented in the design of the dynamic latch comparator. The proposed comparator achieves the lowest power consumption of 156.18nW. However, the delay could not be decreased than that of the reference comparators. This circuitcan be further modified to reduce the delay

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