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Design of High Performance 2-4 Mixed Logic Line Decoders

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Abstract: *This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic; pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoders a 14 transistor topology aiming on minimizing transistor count and power dissipation and a 15transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders are designed by using mixed-logic2–4 pre decoders combined with standard CMOS post decoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulation sat 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.*

Keywords: Low Power, 2-4 Mixed Logic, Line Decoders, CMOS, Transistor Topology.

I. INTRODUCTION

Static CMOS circuits are used for the majority of logic gates in integrated circuits. They consist of complementary N-type metal-oxide-semiconductor (n MOS) pull down and P type metal-oxide semiconductor (p MOS) pull up networks and present good performance as well as resistance to noise and device variation. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design.

Pass transistor logic (PTL) was mainly developed in the 1990s, when various design styles were introduced, aiming to provide a viable alternative to CMOS logic and improve speed, power, and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual n MOS /p MOS pass transistors or parallel pairs of n MOS and p MOS called transmission gates. The most conventional one is complementary CMOS full adder (C-CMOS). It is based on regular CMOS structure with pull-up and pull-down transistors and has 28 transistors. Another conventional adder is the Complementary Pass Transistor Logic (CPL) with swing restoration which uses 32 transistors. CPL produces many intermediate nodes and their complement to make the outputs. The basic difference between the pass transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. A Transmission Gate Full-Adder (TGA) presented in contains 20 transistors. Double pass transistor full adder cell has 48 transistors and operation of this cell is based on the double pass transistor logic in which both NMOS and PMOS logic.

Networks are used. In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines toa maximum of 2n unique output lines or fewer if the n-bit coded information has unusedcombinations. The circuits examined here are n-to-m line decoders, which generate them = 2n minters of n input variables. In present scenario, power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. The chip density and higher operating speed leads to the design of very complex chips with high clock frequencies. So, designing of low power VLSI circuits is a technological need in these due to the high demand for

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portable consumer electronics products. The development of electronic technology was started with the use of vacuum tube as active component in electronic series before semiconductor transistor replaces it. The development of microelectronic technology especially for those of mono-lyrical can produce interfaced circuit by combining all active and passive components in one chip.High speed serialize/ deserializers (SerDes) are now more and more widely used in communication systems for serial interconnections.

Decoders are used whenever an output or a group of outputs is to activate only onthe occurrence of specific combination of input levels. These input levels are often provided by the outputs of a counter or register. When the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially, and they can be used as timing or sequencing the signals to turn devices ON or OFF at specific times. Decoders are widely used in memory systems of computers, where they respond to the address code input from the central processor to activate the memory storage location specified by the address code. Low power consumption has been a priority and so pass transistor based tree decoders have been selected due to the lower leakage and dynamic switching currents.

II. DECODER

The concept of digital data manipulation changes the society in attractive way even all the electronic gadgets are in digital formats. Due to invention of various digitalIC technologies we are in VLSI era. These digital technologies have their own advantages and disadvantages. Due to invention of Bipolar Junction Technology (BJT)the first IC had been implemented that is TTL (Transistor- Transistor Logic). TTL logic provides higher packing density but slow turn off process. A new technology had been developed called ECL (emitter coupled logic) which is fastest logic but provides higherpower dissipation.

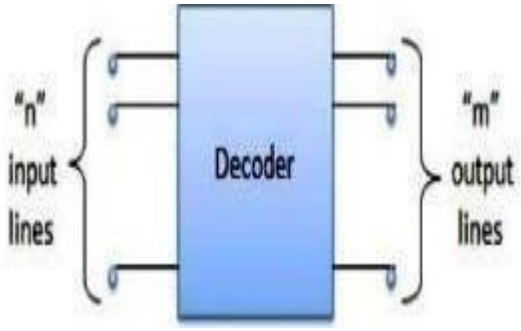

Figure 1: General Block diagram of decoder

But unfortunately, in VLSI era, BJT is defeated by MOS technology.MOS provides lower power dissipation and high packing density than BJT. But again, CMOS beat the MOS technology as it provides excellent static characteristics like lowest static power dissipation and highest Noise margin. But the problem with the CMOS ICs is their dynamic power dissipation and digital switching noise. This problem is solved if we use differential amplifier. Because these amplifiers are not only less sensitive to noise but also enable us to bias amplifier and couple the amplifier stage together without the requirement for bypass and coupling capacitor. Thisborn various technologies like SCL (source coupled logic), FSCL (folded SourceCoupled Logic), MCML (MOS current Mode Logic). Static CMOS logic provides several advantages in designing digital circuit, that are low sensitivity to noise, good performance, low power consumption, etc. But it shows some disadvantages while designing mixed mode ICs. In VLSI circuit, several logic gates switch simultaneously and resulting current causes switching noise. The mixed mode IC has both analog and digital circuit on single semiconductor die so this noise affect analog circuit through substrate coupling. This reduces speed and accuracy of mixed mode ICs. Various methods are used to reduce this noise in mixed mode ICs like separate analog and digitalsupply line, diffuse guard band, bonding pads etc. Source coupled logic(SCL) was developed to reduce this digital switching noise and it is most successful methods amongall the constant current source technique. Now a day's power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. Chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. So, designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products. Decoder is a

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combinational logic circuit that converts a binary integer value to an associated patternof output bits. Applications of decoders are wide; they include data demultiplexing, memory address decoding, seven segment display etc. A decoder is a simple circuit thatconverts a code into a set of signals. It is named as decoder because it changes the big coded data into different simple combinations which can be used to drive any signal but we will begin our study of encoders and decoders because they are simpler to design.Active instructions occur only within a sub-set of all instructions. Address decoder is essential elements in all SRAM memory block whichrespond to very high frequency. Access time and power consumption of memories is largely determined by decoder design. Design of a random access memory (RAM) is generally divided into two parts, the decoder, which is the circuitry from the address input to the word line, and the sense and column circuits, which includes the bit line to the data input/output circuits. Due to large amount of storage cells in memories it can be found various solutions of address decoder designs leading to power consumption reduction and performance improvement. Usually different kinds of pre charging dynamic decoders are used. Design of dynamic decoder is complex and having more probability of wrong sensing. Traditional static decoder gives more accurate result but it is having more number of transistors with large delay. Some solutions use hierarchicaldecoders with pre decoding and implemented binary tree decoder built by Demultiplexers. Decoders plays a crucial role in memory applications, so we introducehigh-speed a mixed-logic design method for line decoders. Address decoder using NAND-NOR alternate stages with pre decoder and replica inverter chain circuit is proposed and compared with traditional and universal block architecture, using 130nm CMOS technology. Delay and power dissipation is reduced in proposed design over existed design. Recently reported logic style comparisons based on full-adder circuits claimed complementary pass-transistor logic (CPL) to be much more power efficient than complementary CMOS. High speed multiplier is implemented with the help of Complementary Pass transistor Logic (CPL)is a family of CMOS design. Same CPL technique is used to implement Arithmetic and Logic Unit [ALU] in for increasing the design speed. Transmission switch theory is introduced which is used for CMOS digital circuit design. Complex logic gate is implemented in based on pass transistor dual voltage logic for low power applications. Paper describes about develop a Karnaugh map based method that can be used to efficiently synthesize pass transistor logic circuits, which have balanced loads on true and complementary input signals. The method is applied to the generation of basic twoinput and three-input logic gates in CPL, DPL and DVL. The method is general andcan be extended to synthesize any pass-transistor network. Above papers describes. different techniques to implement logic designs which gives better results in terms of area, delay and power consumption. Three different decoder designs are implemented, they are AND–NOR, Sense–Amp, and the AND decoder. These pre charge based designs are analyzed the constraints (area, energy consumption and delay). AND based decoder.

III. LITERATURE SURVEY

R. Zimmermann and W. Fichtner, Jul.1997, Recently reported logic style comparisons based on full-adder circuits claimed complementary pass-transistor logic (CPL) to be much more power-efficient than complementary CMOS. However, new comparisons performed on more efficient CMOS circuit realizations and a wider range of different logic cells, as well as the use of realistic circuit arrangements demonstrate CMOS to be superior to CPL in most cases with respect to speed, area, power dissipation, and power-delay products. An implemented 32-b adder using complementary CMOS has a power-delay product of lessthan half that of the CPL version. Robustness with respect to voltage scaling and transistor sizing, as well as generality and ease-of-use, are additional advantages of CMOS logic gates, especially when cell-based design and logic synthesis are targeted. This paper shows that complementary CMOS is the logic style of choice for the implementation of arbitrary combinational circuits if low voltage, low power, and smallpower-delay products are of concern THE increasing demand for low-power very largescale integration (VLSI) can be addressed at different design levels, such as thearchitectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits.

K. Yano *et al.*, 1990. A 3.8-ns, 257-mW, 16*16-b CMOS multiplier with a supply voltage of 4 V is described. A complementary pass-transistor logic (CPL) is proposed and applied to almost the entire critical path. The CPL consists of complementary inputs/outputs, an nMOS passtransistor logic network, and CMOS output inverters. The CPL is twice as fast as conventional CMOS due to lower input capacitance and high logic functionality. Its multiplication time is the

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fastest ever reported, even for bipolar and GaAs ICs, and it can be enhanced further to 2.6 ns with 60 mW at 77 K.

M. Suzuki *et al.*, 1993, A 32-b CMOS ALU (arithmetic and logic unit), fabricated using 0.25- mu m CMOS technology, that has a 1.5-ns addition time with a 2.5-V supply, is described. This addition time is achieved using double pass-transistor logic (DPL) and a conditional carry-selection (CCS) carry look-ahead circuit. The measured supply-voltage dependence of ALU addition time is shown, revealing excellent low-voltage performance. DPL AND/NAND and OR/NOR ring oscillators show measured speed improvements of 15% and 30% over CMOS NAND and NOR ring oscillators.

V. G. Oklobdzija and B. Duchene, 1995, New pass-transistor logic termed DVL which contains fewer transistors than its counterpartDPL yet maintain comparable performance. A method for synthesis of such networksis also developed and demonstrated in this paper. The new logic is characterized by good speed and low power.

Pass-Transistor Logic (DIPL), developed by Hitachi demonstrated a 1.511s 32- bit ALU and 4.4nS 54-bit multiplier in 0.25 pm technology. However, DPL has not yet been fully adopted because of its high transistor count. The objective of the new logicgates and the synthesis method developed for pass-transistor logic is to minimize thenumber of transistors used in DPL and preserve the speed of the logic.

IV. PROPOSED SYSTEM

Transmission gate logic (TGL) can efficiently implement AND/OR gates , thus itcan be applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 2 (a) and (b), respectively. They are full swinging, but not restoring for all input combinations. Regarding PTL, there are two main circuit styles: those that use nMOS only pass transistor circuits, like CPL, and those that use both nMOS and pMOS pass transistors, like DPL and DVL. The style we consider in this work is DVL, which preserves the full swing operation of DPL with reduced transistor count . The 2-input DVL AND/OR gates are shown in Fig. 2 (c) and (d), respectively. They are full swinging but non-restoring, as well. Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors. Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, i.e. the fact that they do not have balanced input loads.

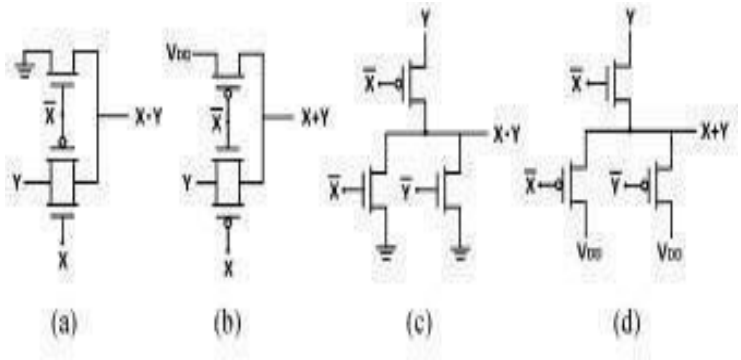

Figure. 2 Three-transistor AND/OR gates considered in this work. (a) TGL AND gate. (b) TGL OR gate. (c) DVL AND gate. (d) DVL OR gate

As shown in Fig. 4.1, we labeledthe 2 gate inputs X and Y . In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gateterminal and propagates through a pass transistor to the output. We will refer to X and Y as the control signal and propagate signal of the gate, respectively. Using a complementary input as the propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A B) or implication (A + B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) orOR (A + B) function, either choice is equally efficient. Finally, when implementing theNAND (A + B) or NOR (A B) function, either choice results to a complementary propagate signal, perforce.

(i) 14-Transistor 2–4 Low-Power Topology-Designing a 2–4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the

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same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14. Let us assume that, out of the two inputs, namely, A and B, we aim to eliminate the B inverter from the circuit. The Do minterm (A B) is implemented with a DVL gate, where A is used as the propagate signal. The D1 minterm (AB) is implemented with a TGL gate, where B is used as the propagate signal. The D2 minterm(A B) is implemented with a DVL gate, where A is used as the propagate signal. Finally,The D3 minterm (AB) is implemented with a TGL gate, where B is used as the propagatesignal. These particular choices completely avert the use of the complementary B signal therefore, the B inverter can be eliminated from the circuit, resulting in a 14-transistor topology (9 nMOS and 5 pMOS). Following a similar procedure with OR gates, a 2–4 inverting line decoder can be implemented with 14 transistors (5 nMOS and 9 pMOS) as well: I0 and I2 are implemented with TGL (using B as the propagate signal), and I1 and I3 are implemented with DVL (using A as the propagate signal). The B inverter can once again be elided. Inverter elimination reduces the transistor count, logical effort and overall switching activity of the circuits, thereby reducing power dissipation. The two new topologies are named "2-4LP" and "2–4LPI," where "LP" stands for "low power" and "I" for "inverting." Their schematics are shown in Fig. 3(a) and (b), respectively.

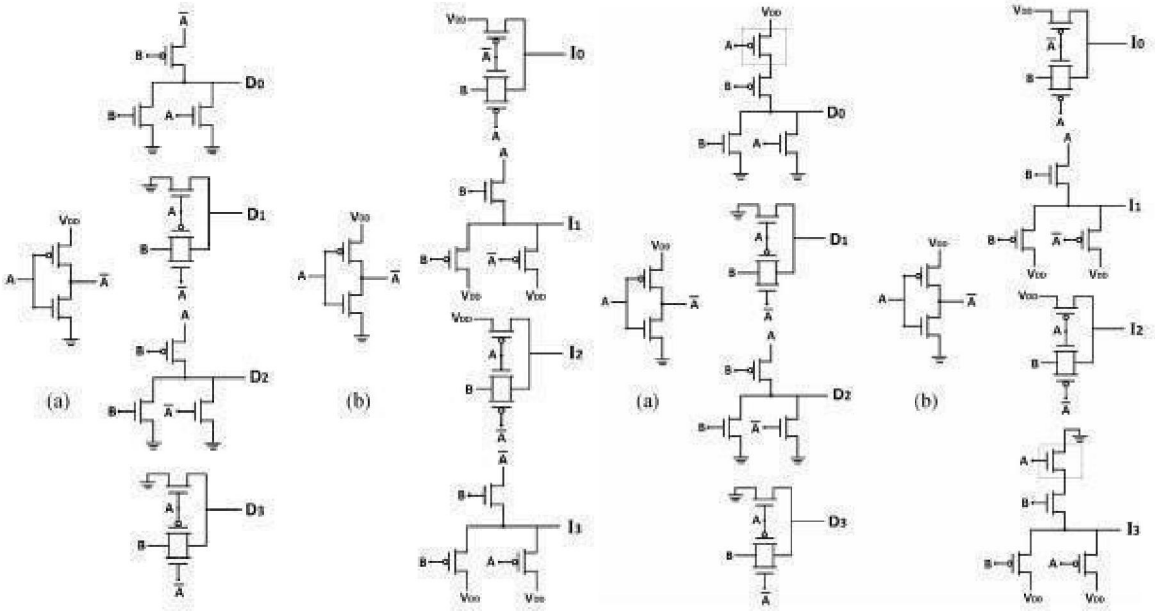

Figure. 3. New 14-transistor 2–4 line decoders Figure. 4. 15-transistor 2–4 line decoders
(a) 2–4LP. (b) 2–4LPI (a) 2–4HP. (b) 2–4HPI

(ii) 15-Transistor 2–4 High-Performance Topology- The low-power topologies presented above have a drawback regarding worst casedelay, which comes from the use of complementary A as the propagate signal in the case of D0 and I3. However, D0 and I3 can be efficiently implemented using static CMOS gates, without using complementary signals. Specifically, D0 can be implemented with a CMOS NOR gate and I3 with a CMOS NAND gate, adding one transistor to each topology. The new 15T designs present a significant improvement in delay while only slightly increasing power dissipation. They are named "2–4HP" (9 nMOS, 6 pMOS) and "2–4HPI" (6 nMOS, 9 pMOS), where "HP" stands for "high performance" and "I" stands for "inverting." The 2–4HP and 2–4HPI schematics are shown in Fig. 4.(a) and (b), respectively.

V. CONCLUSION

This brief has introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2–4 line decoder topologies, namely 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer reduced transistor count and improved power delay performance in relation to conventional CMOS decoders. Furthermore, four new 4–16 line decoder topologies were presented, namely 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, realized by using the mixed-logic 2-4 decoders as pre decoding circuits, combined with post decoders implemented in static CMOS to provide driving capability. A variety of comparative spice simulations was performed

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at 32 nm, verifying, in most cases, a definite advantage in favour of the proposed designs. The 2–4LP and 4–16LPI topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2–4LPI, 2–4HP, and 2–4HPI, as well as the corresponding 4–16 topologies (4–16LP, 4–16HPI, and 4–16HP), proved to be viable and all-around efficient designs; thus, they can effectively be used as building blocks in the design of larger decoders, multiplexers, and other combinational circuits of varying performance requirements. Moreover, the presented reduced transistor count and low power characteristics can benefit both bulk CMOS and SOI designs as well. The obtained circuits are to be implemented on layout level, making them suitable for standard cell libraries and RTL design.

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