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Review on Compensating Voltage Sag in Single Phase and Three Phase Lines Using Fault Current Limiter

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Abstract: *A high potential fault current levels in power grid is not a new approach, and should eventually exceed, the limitation of short-circuit-current would be existed protection devices. Different to pricey system upgrades of protection devices, Fault Current Limiters (FCL's) gives an additional cost efficient solutions to forestall recent protection devices and different instrumentality on the system from being broken by excessive fault currents. Evaluation of short circuit faults may usually the origin of voltage sags at a purpose of common coupling point (PCC) during a power network, the extent of the voltage sag is proportional to the short current level, reducing the fault current level at intervals the networks will scale back voltage sags throughout faults and defend sensitive loads that are interfaced to a similar PCC. The planned structure prevents voltage sag and counter balance the phase-angle of the PCC once fault prevalence. As a result, different feeders which are interlinked to the sub-station PCC can have attentive power quality. During this paper a high performance 3-phase fault current electrical model is planned. A Matlab/Simulink model is developed and simulation results are conferred.*

Keywords: Fault current limiter (FCL), point of common coupling (PCC), power quality (PQ), semiconductor switch

I. INTRODUCTION

Power quality varieties are delegated either unsettling influences or relentless state varieties. Of The Aggravation relate to variations from the norm in the framework voltages or flows because of a deficiency or some irregular operations. Consistent state varieties allude to rms deviations from the ostensible amounts or harmonic distortions. By regularly, these are observed by aggravation of the analysers, voltage recorders, symphonies analysers and so forth. However, with the headway in the computer innovation, better, speedier and more faultless instruments can now be intended for monitoring the power quality checking and accurate analysis [1], the data information for any power quality checking gadget is acquired through transducers. This incorporates the current-transformers, voltage-transformers, as well a hall impact current and voltage transducers and so forth. Aggravation analysers and unsettling influence screens are instruments that are particularly intended for power quality estimations. There are two classifications of these gadgets - traditional analysers and representation based analysers. Classical analysers give data like magnitude content, and span of sags/swells, under/over voltages and so forth. Realistic based analysers are furnished with memory, such that the ongoing information could be spared [2]. The focal point of this device is that the saved information could be examined later to focus the source and reason for the power-quality issues. Voltage sags is an essential PQ issue on account of the high sensitive load developer. The overall experience has been indicated that short circuit deficiencies (faults) are the principle inception of voltage sags and, consequently, there is a misfortune of voltage quality. This issue seems particularly in buses which are associated with radial/spiral feeders [3]–[5]. Shortcomings at either the transmission or distributed level may cause transient voltage droop or swell in the whole framework or an extensive a piece of it. Additionally, under overwhelming burden conditions, a noteworthy voltage drop may happen in the framework. Voltage droops can happen at any moment of time, with amplitudes extending from 10–90% and a span enduring for a large portion of a half a cycle to one moment. Further, they could be either adjusted or unequal, contingent upon the kind of deficiency and they could have eccentric magnitudes, contingent upon variables, for example, separation from the fault and the transformer associations. Voltage swell, then again, is characterized as a sudden expanding of supply voltage up 110% to 180% in RMS voltage at the system crucial recurrence with the length of time from 10 ms to 1 ms moment [6]. Voltage swells are not as paramount as voltage sags due to they are less normal in distribution frameworks. Voltage droop and swell can result in sensitive supplies, (for example, found in semiconductor or compound plants) to fail to flat, or completely lay-down, and make an expansive current unbalance that could blow wires or outing breakers. The voltage droop throughout the fault is relative to the short out present quality. A successful methodology to forestall expected voltage droop and enhance the quality nature of voltage at common coupling point (PCC) is the deficiency current limit by method for a device interfaced at the start of most uncovered outspread feeders [7]. This can also be attributed to the concern over power quality (PQ) as FCLs can be used to mitigate voltage sags caused by faults. For an exceptionally dependable power supply, the fault current limiter (FCL) is turning into a fundamental part in advanced based power system network. The current-constraining device is obliged to be acquainted into the power system network to enhance the fault current presence from climbing to its full prospective worth. This can additionally be credited to the more concern over power quality (PQ) as FCLs might be utilized to relieve voltage sags brought on by faults These will abstain from updating switchgears throughout framework development and enhance the PQ conveyed to customers. FCLs are required to give a constrained and maintained short circuit current present through the fault/flaw for a sufficient time (e.g., 1s) to empower legitimate coordination of defensive relays in optimal protection schemes.

II. LITERATURE SURVEY

[1]. A 22.9 kV/630 A-class superconducting fault current limiter (SFCL) was installed on a distribution line in Icheon Substation for real-grid operation. The substation is located in a semi-urban area with moderate loads. The SFCL is of hybrid type. After installation it was subjected to a series of on-site tests. Test procedures were determined by following convention in testing both superconductivity-related and not-related specifications of the SFCL. Tests performed were minimum limiting current test, temperature test, dielectric test, and impedance measurement. After successfully passing the tests, the cooling system of the SFCL was operated for more than 5 months under various load conditions to optimize the operation condition. During that period, temperatures, liquid nitrogen level, and internal pressure remained within ±0.1 K, ±0.5 cm, and ±0.5 bar range, proving stability in cooling superconducting elements. The SFCL was then energized and went into real-load operation successfully.

[2] In this paper, a new dual function fault current limiter-dynamic voltage restorer (FCL-DVR) topology is proposed. The proposed structure, in addition to performing routine FCL tasks, can be used to improve the voltage quality of point of common coupling (PCC). A salient feature of this FCL-DVR is its reduced number of semiconductor switches and gate drive and control circuit components. Perhaps, variety structure of FCL-DVR have been proposed but most distinctive feature of proposed structure is lower power loss. The operation modes and the control strategy of the FCL have been presented and studied. In addition, the proposed structure has been compared with other structures to prove the efficiency of proposed structure. The simulation results as well as experimental outcomes from a laboratory scaled-down prototype are provided, which prove the efficiency and feasibility of the proposed structure.

[3] As electric power systems become more complicated, the fault current experiences more frequent changes. To solve this problem, we suggest a novel hybrid-type superconducting fault current limiter (SFCL). Some issues accompany application of resistive-type SFCLs to electric power systems, including initial installation price, operation and maintenance costs, and high-current problems. To overcome these problems, hybrid SFCLs have been developed in some institutions. This paper presents experimental tests of a novel hybrid-type SFCL composed of a resistive superconducting coil, two thyristors, and a control circuit. The superconducting coil limits the first peak of the fault current, and the thyristors control the magnitude of the fault current other than the first peak by adjusting the firing angles. The interactions between the superconducting coil and the thyristors reduce the use of superconducting wire.

[4] Enlarging the electric power supply capacity of 22.9 kV distribution line by upgrading the main transformer from 60 MVA to 100 MVA has been under consideration in order to cope with increasing electric power demands of distriution line in Korea which aims to replace some 154 kV supply demands by 22.9 kV large-capacity distribution systems. In this case, the prospective fault current of 22.9 kV distribution line is much bigger than the rated withstand fault current level of conventional electric equipment's. As a major feasible solution to reduce excessive fault current, superconducting fault current limiters (SFCLs) are considered to be installed at 154 kV/22.9 kV substation. But until now, certified specifications or test procedures were not available considering utilities' requirements. And the performances of various types of SFCLs were not deeply investigated regarding the reclosing scheme of conventional networks. In this paper, in order to determine the suitable type of SFCL for newly installed 22.9 kV large distribution line in Korea, requirements

and specifications of SFCLs were proposed considering the installation spots of large-capacity distribution line. Four types of SFCLs were modeled and analyzed using EMTP and their performances focusing on the coordination with recloses were investigated to verify the suitability into the large-capacity distribution line. Consequently, detailed specifications and expected installation sites were proposed and suitable types of SFCLs for 22.9 kV large-capacity distribution line were suggested.

[5].In this paper, a novel bridge-type fault current limiter (FCL) based on self-turnoff devices for three-phase power systems is proposed. Compared with the SCR-based bridge type FCL, the new one is smaller in size, better in dynamic performance, and simpler in control method and control circuitry. The novel FCL is composed of a rectifier bridge-a dc-limiting reactor and one/three bypass reactor/reactors-for a single-phase/three-phase structure. The increasing speed of the fault current just after the occurrence of a fault is limited by a dc-limiting reactor, whose inductance is designed according to the response speed of the control circuit. The bypass reactors are designed in terms of the requirements of the coordination of protective relays. The source currents during limiting events are sinusoidal and do not have any harmful effects on the overall protection schemes, impedance relays, and conventional current and voltage transformers. The topologies of the proposed FCL for three-phase four-wire and three-phase three-wire power systems are investigated, respectively, in detail. Parameter design and optimization are presented. The fault and fault-mode judgment method is described briefly. Simulations and experimental results prove the feasibility of the new FCL.

[6]. This paper presents A high potential fault current levels in power grid is not a new approach, and should eventually exceed, the limitation of short-circuit-current would be existed protection devices. Different to pricey system upgrades of protection devices, Fault Current Limiters (FCL's) gives an additional cost-efficient solutions to forestall recent protection devices and different instrumentality on the system from being broken by excessive fault currents. Evaluation of short circuit faults may usually the origin of voltage sags at a purpose of common coupling point (PCC) during a power network, the extent of the voltage sag is proportional to the short current level, reducing the fault current level at intervals the networks will scale back voltage sags throughout faults and defend sensitive loads that are interfaced to a similar PCC. The planned structure prevents voltage sag and counter balance the phase-angle of the PCC once fault prevalence. As a result, different feeders which are interlinked to the sub-station PCC can have attentive power quality. During this paper a high performance 3-phase fault current electrical model is planned. A Matlab/Simulink model is developed and simulation results are conferred. Finally a computer simulated results are conclusive through prototype design..

III. RESEARCH OBJECTIVES

Design and simulation of FCL for the compensation of power quality problems to make the distribution system more efficient using MATLAB software.

- Main objective of project to eliminate the power quality problem in single phase and three phase line
- To minimize the sag using FCL in single phase and three phase line
- To Reduce Total Harmonic Distortion
- No power loss at fault conditions;\

IV. PROPOSED METHODOLOGY

- Implementing a single phase and three phase line without FCL.
- Implementation of Fault current limiter
- Implementation will be the desirable operation of the system for undesirable conditions for example Sag mitigation and harmonics reduction.
- Simulation of the model can be done in MATLAB software. Evaluation of the performance.

As Fig. 1 depicts the schematic diagram of proposed FCL topology which is comprised based on two following parts? 1) One is bridge part that contains a un-controlled rectifier form in bridge manner as a coordination of small dc limiting reactor (Ldc). (Note here internal resistance (Rdc) is engaged too), a power electronic switch (may be IGBT or GTO) with a supportive diode for freewheeling action (D5). 2) Another component is shunt branch, acts as a limiter for enhancing the fault currents; it involves a shunt resistor and a shunt inductor (Rsh + i Lsh).

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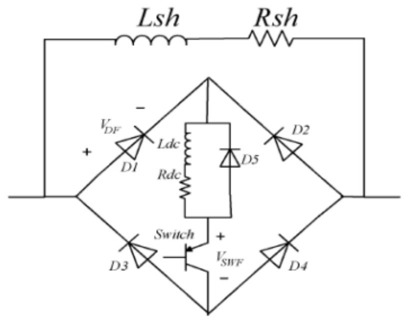

Fig 1 Proposed FCL technology

V. CONCLUSION

In proposed system single phase and three phase fault will be create due which voltage deep accures in the system. This power quality problem will be mitigate using Fault cuurent limiter. Proposed system will be simulated in MATLAB Simulink.

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