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A Single Phase Transformer Less DC- AC Multi Level Inverter for PV Applications

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Abstract: *There is a strong trend in the photovoltaic inverter technology to use transformer less topologies in order to acquire higher efficiencies combining with very low ground leakage current. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals' design. Also, the low-pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage. The switching losses and the voltage stress of power devices can be reduced in the proposed multilevel inverter. The operating principles of the proposed inverter and the voltage balancing method of input capacitors are discussed. Finally, simulation of multilevel inverter with 400-V input voltage and output 220 Vrms/2 kW is implemented. The multilevel inverter is controlled with sinusoidal pulse-width modulation (SPWM).*

Keywords: DC–AC inverter, Maximum Power Point Tracking (MPPT), multilevel

I. INTRODUCTION

As a result of high-technology development, the demand and the quality of electric power are higher than before. Because of the advancement of semiconductor, the specification of power device and power conversion technique is promoted. One of the power converters which can transform dc–ac is called inverter. Inverter is the intermedium which transmits power to other electrical equipment such as uninterruptible power supply, servo motor, air-conditioning system, and smart grid composed of renewable energy shown in Fig. 1. To satisfy different demands and characteristic of loads, the output frequency and voltage have to change with different loads [1]–[3]. In recent years, the amount of power equipment is increasing. Therefore, the harmonic pollution of power system becomes more serious. Several standards and regulations have been formulated to limit quality of harmonics and power factor of electric equipment such as IEEE Std. 1547 and UL 1741. [4]– [6]. Furthermore, in order to meet the industry requirements for high power applications, the voltage stress of the power device also increases. Although an insulated gate bipolar transistor (IGBT) has features of high power rating and high voltage stress, it cannot operate at high frequency. And the design of IGBT gate driver is complicated. AMOSFET is the appropriate component to operate at high frequency, but power rating is not as good as IGBT. To solve the problem, many different topologies of multilevel use low rating component at high-power application. The purpose of the multilevel topology is to reduce the voltage rating of the power switch. Therefore, it usually is used at high-power application. By combining output voltages in multilevel form, it has advantages of low dv/dt, low input current distortion, and lower switching frequency. As a result of advantages of multilevel topology, several topologies have emerged in recent years [7], [8]. A novel multilevel inverter is designed and implemented in this paper. The major feature of the proposed topology is the reduction of power components. The sinusoidal pulsewidth modulation (SPWM) is used to control proposed circuit.

II. PULSE-WIDTH MODULATION (PWM)

The proposed a novel topology used in a seven-level inverter. The input voltage divider consists of three C1, C2 and C3 series capacitors. Four MOSFETs and four diodes relay the divided voltage to the H-bridge. The voltage is sent to the H-bridge output terminal, which consists of four MOSFETs. The proposed multilevel inverter produces a seven-level ac output voltage with the correct gate signal configuration.

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Service Concepts: The appropriate 7 voltage output levels} (1/3Vdc,} 2/3Vdc,} Vdc, 0) are generated as follows.

1) In order to generate a voltage level Vo = 1/3Vdc, S1 is switched on at a positive half-cycle. Energy is given by the C1 capacitor and the H-bridge voltage is 1/3Vdc. S5 and S8 are turned on, and the voltage applied to the load terminal is 1/3Vdc. Fig.2 In this mode, 3 shows the current direction.2) S1 and S4 are turned on to produce voltage level Vo = 2/3Vdc. Energy is given by the C1 and C2

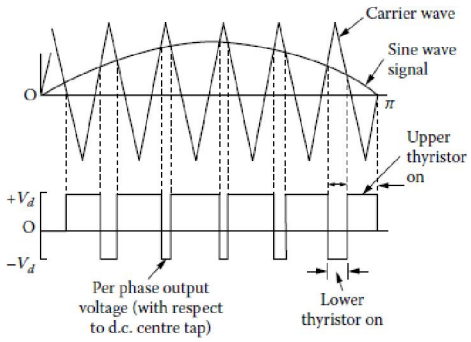

Figure 1 (The principle of pulse-width modulation (PWM). (From Arrillaga, J., Bradley, J.D., and Bodger, P. (1985), *Power System Harmonics,* John Wiley, Chichester, U.K. With permission.)

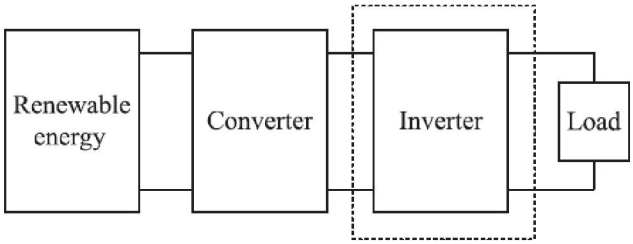

Figure 2 Block diagram of renewable system.

Layout of the circuitcapacitors. The voltage over the H-bridge is 2/3VDC. S5 and S8 are turned on, and the voltage applied to the load terminal is 2/3Vdc. Fig. 2 displays the current path in this mode.

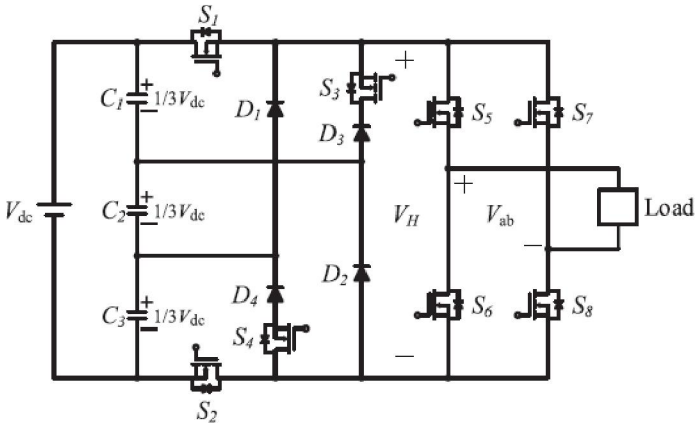

Figure 3. Proposed seven-level inverter topology.

3) To produce the voltage level Vo = Vdc, S1 and S2 are turned on. Energy is given by the C1 , C2 and C3 capacitors. The voltage over the H-bridge is VDC. S5 and S8 are switched on, and VDC is the voltage applied to the load terminals. Fig. 3 In this mode, 5 shows the current direction.

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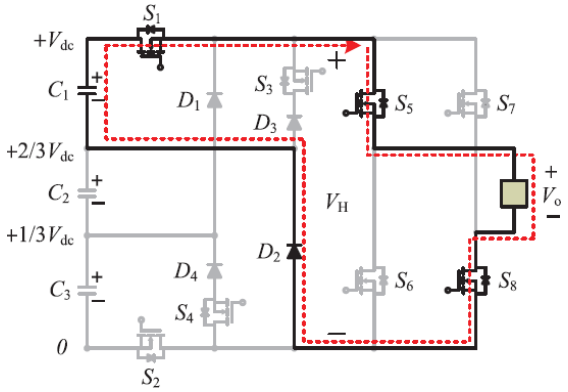

Figure 4. Switching combination of output voltage level 1/3*V*dc.

1) In order to generate the voltage level Vo = −1/3Vdc, S2 is switched on during the negative half cycle. Energy is provided by the C3 capacitor and the H-bridge voltage is 1/3Vdc. S6 and S7 are switched on and the voltage applied to the load terminals is −1/3Vdc. Fig. 6 shows the current path in this mode.

2) To produce the voltage level Vo = −2/3Vdc, S2 and S3 are turned on. Energy is provided by the C2 and C3 capacitors. The voltage over the H-bridge is 2/3VDC. S6 and S7 are turned on and the voltage applied to the load terminals is −2/3Vdc. Fig. Seven shows the current path in this mode.

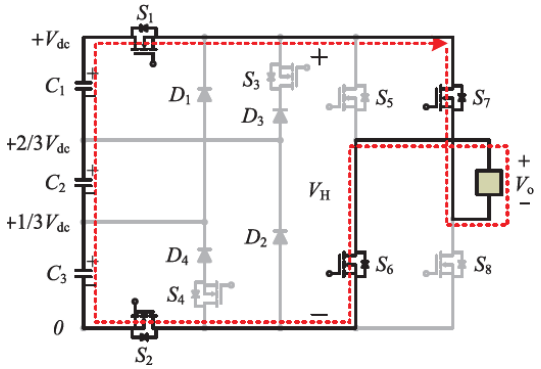

Figure 5. Switching combination of output voltage level 2/3*V*dc.

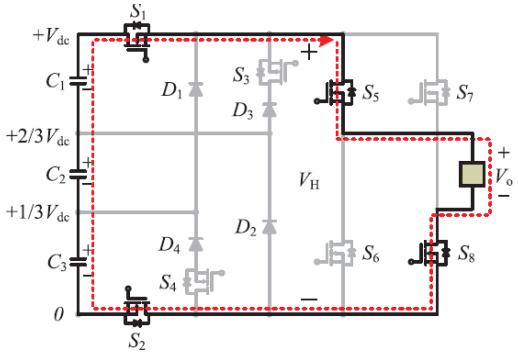

Figure 6. Switching combination of output voltage level *V*dc.

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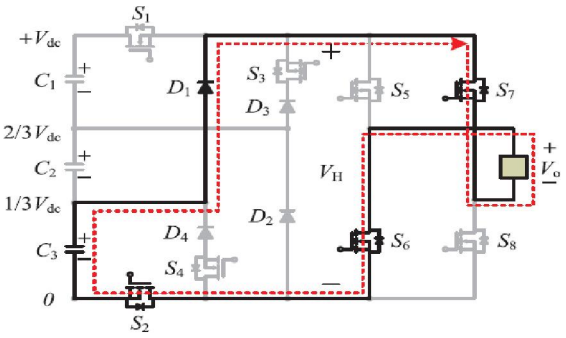

Figure 7. Switching combination of output voltage level −1/3*V*dc.

To generate the voltage level Vo = −Vdc, S1 and S2 are switched on. Power is given by the C1 , C2 and C3 capacitors, voltage is Vdc through the H-bridge. S6 and S7 are switched on, the voltage applied to the load terminal is −Vdc. Fig.Fig. 8 shows the current path at this mode

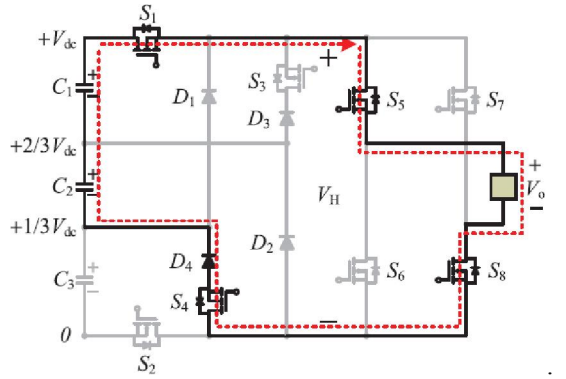

Figure 8. Switching combination of output voltage level −2/3*V*dc.

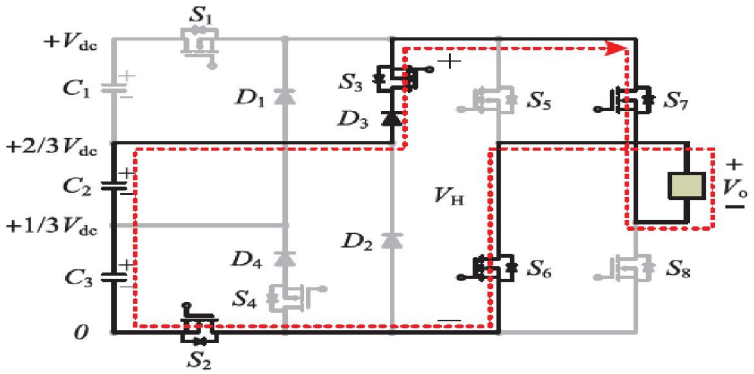

Figure 9. Switching combination of output voltage level −*V*dc.

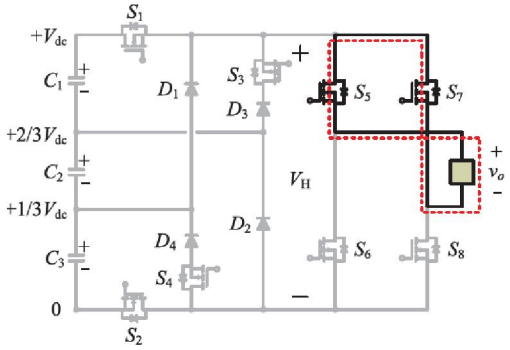

Fig. 10. Switching combination of output voltage level 0

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1) Vo = −Vdc, S1 and S2 are turned on to produce the voltage point. Power is supplied by the C1 , C2 and C3 capacitors, voltage is Vdc by the H-bridge. S6 and S7 are turned on and the voltage applied to the load terminal is −Vdc. Fig. 8 shows the current path in this mode.

III. SIMULATION RESULTS

Fig. 11 presents the output voltage waveform *v*ab showing the desired seven voltage levels and output waveform *vo*. The seven voltage levels in the figure are }133, }267, }400, and 0V.

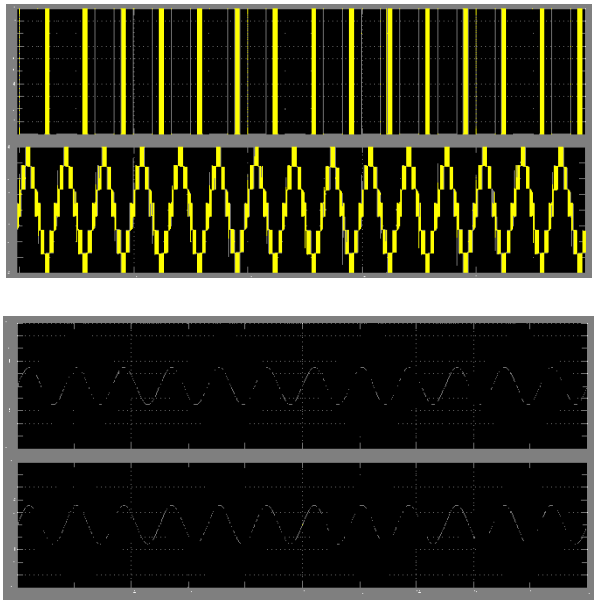

Fig. 11. Waveforms of *v*gs1, *v*ab, *vo*, and *io*at 500 W.

IV. CONCLUSION

Transformer less inverters offer better efficiency compared to those inverters with galvanic insulation. On the other hand, in the event that the transformer is omitted, the common-mode behavior of the inverter topology significantly influences the ground leakage current through the parasitic capacitance of the PV. The main idea of the proposed configuration is to reduce the number of power units. The reduction of the power supply is illustrated by contrast with conventional systems. Finally, a simulation setup of a seven-level inverter with an input voltage of 400 V and an output of 220 Vrms/2kW is implemented. Simulation tests show that the average efficiency is 96.9 per cent and the overall load efficiency is 94.6 per cent.

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