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Power Optimized High Speed Sense Amplifier for 6T SRAM

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Abstract : *Static Random Access Memory (SRAM) is used in a wide range of applications in modern VLSI like processors, microcontrollers, embedded systems and SoC due to its High Speed data access and reliable operation. A standard 6T SRAM cell is composed by 6 MOS transistors, two cross coupled inverters and two access transistors. While reading data there is a small voltage difference between complementary Bit Lines (BL and $B\bar{L}$) which needs to be correctly sensed using a Sense Amplifier. Problems faced by traditional sense amplifiers can include increased levels of power consumption, slower sensing speeds and reduced reliabilities especially during low voltages. This project proposes a Power Optimized High Speed Sense Amplifier for 6T SRAM. The system uses a 6T SRAM Cell, Bit Line Precharging Circuit and Optimised Sense Amplifier. LTspice was used to create the design. The circuit was analysed by using transient waveforms of voltage and currents. Key parameters were looked at such as power consumption, speed and Read Delay. This should give us a fast data sensing circuit with reduced power consumption and reliable reading. The design would be useful for Low Power VLSI memory applications.*

Keywords: SRAM, 6T SRAM, Sense Amplifier, Low Power, High Speed, VLSI, LTspice, Read Delay, Power Optimisation, Bit Lines

I. INTRODUCTION

SRAM is one of the most important types of semiconductor memories found within modern digital electronic systems. These memories are used within Microprocessors, Microcontrollers, Embedded Systems, Cache Memories and System-on-Chip (SoC). This is due to them having fast and reliable access times, also no refresh is required providing a power supply is present. With increasing demands for high performance and low power devices, improving SRAMs is a key aspect of VLSI technology. The 6T SRAM is a popular design due to its simplicity. It contains 6 transistors; two CMOS Inverters connected together with 2 access transistors. The cross connected CMOS Inverters act as a bistable memory which allows a single bit of data to be stored, either a Logic 0 or a Logic 1. The access transistors allow the memory nodes connect to complementary bitlines enabling data to be read and written. These access transistors will be controlled by the Word Line (WL). There are 3 main functions within an SRAM, storing, writing and reading. Data will be stored within the cross connected inverters. To write data you would send data to the complementary bitlines and activate the WL. To read data you would send data to the bitlines and capture it using the sensing circuitry. All of these functions are important however the reading function is very important as it needs to capture the data. First the complementary bitlines would be precharged to a certain voltage. Then the WL is activated. Depending on what data is being stored within the SRAM cell only one bitline would change by a small amount. This causes there to be a small voltage differential between both bitlines. This voltage differential can be very small so a Sense Amplifier is needed to capture this voltage change. The Sense Amplifier is a key component within the SRAM memory. It will take the voltage differential and amplify it to produce a full logic output. The Sense Amplifier will affect the speed, power consumption and reliability. A good Sense Amplifier should have accurate sensing capabilities allowing it to capture

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the small voltages on the inputs. It should also have the fastest delay and lowest power consumption. This is a key factor to optimise to create an efficient SRAM memory.

Traditional Sense Amplifiers may suffer from increased power consumption, sensing delays and reliability issues when running at low voltages. The Sense Amplifier may be affected by a number of factors, including the voltage differential on the inputs, transistor characteristics and conditions. This can be an issue within modern VLSI systems as they require faster speeds and have a demand for low power consumption within small circuits. Power consumption is an important factor to consider when designing an SRAM. We are making the SRAM circuits more complex to fit into high density VLSI circuits so we want to reduce any unnecessary power consumption. The Sense Amplifier will consume power when sensing data, if the sensing is not efficient this could increase the power consumption. The design should be optimised to create a balance between power consumption, sensing speed and reliability. This project will focus on the design and analysis of a Power Optimised High Speed Sense Amplifier for 6T SRAM. The design will include the traditional 6T SRAM cell, Bit Line Precharge and Optimised Sense Amplifier. The focus will be on optimising the sensing of the circuit. This will be achieved by analysing the circuit to create the best conditions for fast and low power consumption. The design and analysis was carried out using LTspice simulation software. This allowed us to see how much voltage change occurs on the bitlines when the Sense Amplifier is activated and what the output is. Using a transient analysis we can observe how quick the circuit is operating. The voltage and current waveforms will show us how the circuit is operating. Key factors including power consumption, sensing delay, output and reading were considered. The results from the simulations can be seen to observe how well the proposed design performs against the chosen traditional design. The aim of this project will be to design a Sense Amplifier to improve the sensing speed, reduce power consumption and capture reliable data within 6T SRAM. This will help to create an efficient memory circuit for modern VLSI applications.

II. RELATED WORK

Several researchers have worked on improving the performance of Static Random-Access Memory (SRAM), particularly in the areas of power consumption, read speed, sensing accuracy and circuit reliability. SRAM is widely used in modern VLSI systems because of its fast data access and stable storage operation. However, as the demand for high-speed and low-power electronic devices increases, improving the efficiency of SRAM circuits has become an important research area. One major area of research is the development of low-power sense amplifier circuits. In a conventional SRAM read operation, the sense amplifier detects a small voltage difference between the complementary bit lines, BL and $\overline{BL}$. During this process, the circuit consumes power to amplify the input signal and generate the required output. Researchers have investigated different circuit structures and transistor configurations to reduce power consumption during sensing. These techniques aim to improve energy efficiency while maintaining accurate data detection. Another important research direction is high-speed sensing. The read speed of an SRAM system depends on how quickly the sense amplifier can identify the voltage difference between the bit lines and produce a valid digital output. Conventional sensing methods may introduce additional delay, especially when the input voltage difference is very small. To overcome this limitation, researchers have explored different amplifier structures and circuit optimization techniques to improve the output response and reduce sensing time. Some research studies have focused on current-mode sense amplifiers for low-power SRAM applications. These architectures use current variations during the sensing process to identify the stored data. Their performance is studied in terms of sensing speed, sensitivity and power consumption. The selection of circuit topology and transistor operating conditions plays an important role in determining the overall performance of these designs. Researchers have also investigated cross-coupled sense amplifier structures. These circuits use positive feedback to strengthen the difference between the input signals and produce a clear output. The design of such circuits requires careful consideration of transistor sizing, switching behaviour and control signals. Proper circuit optimization can help improve the sensing response and support reliable operation.

Another significant research area is low-voltage SRAM operation. Modern electronic devices increasingly require memory circuits that operate with reduced supply voltage to improve energy efficiency. However, lower supply voltage

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can reduce the available voltage difference between the bit lines and make data sensing more difficult. Researchers have therefore studied different circuit techniques to improve sensing sensitivity and maintain reliable operation under low-voltage conditions. The precharge circuit is also an important part of SRAM read-operation research. Before the read operation begins, the complementary bit lines are brought to a suitable initial voltage level. Proper precharge timing helps establish the required initial conditions for sensing. Incorrect timing between precharge control, word-line activation and sense-amplifier enable signals may affect the read operation. Therefore, coordination between these control signals is essential for effective SRAM operation. In addition to circuit architecture, transistor sizing has received considerable attention in sense amplifier design. The width and length of MOS transistors influence current flow, switching behaviour, power consumption and sensing delay. Selecting suitable transistor dimensions is important for obtaining a balanced design. Researchers have studied the relationship between transistor characteristics and overall circuit performance to improve sensing efficiency. Simulation-based analysis is commonly used to study and evaluate SRAM and sense amplifier circuits. Tools such as LTspice help designers examine circuit operation through transient voltage waveforms, current waveforms and timing responses. Simulation allows different circuit configurations and operating conditions to be analysed before practical hardware implementation. It also helps identify possible design limitations and compare circuit performance under similar conditions.

Although several existing studies have focused on reducing power consumption, improving sensing speed and increasing sensing sensitivity, achieving all these improvements together remains a challenge. A design that focuses mainly on high-speed operation may consume more power, whereas a design that prioritizes low power may introduce additional sensing delay. Therefore, an optimized circuit should provide a suitable balance between power consumption, sensing speed and reliable data detection. Based on the understanding of existing research, the proposed project focuses on developing a Power-Optimized High-Speed Sense Amplifier for 6T SRAM. The system combines a conventional 6T SRAM cell, a bit-line precharge circuit and an optimized sense amplifier. The proposed design is analysed using LTspice simulation software to study the read-operation behaviour and sensing response. Voltage and current waveforms are used to examine the circuit operation, while power consumption and sensing delay are considered as important performance parameters. The main objective of the proposed work is to study and improve the sensing performance of a 6T SRAM system through circuit-level optimization. By focusing on both power efficiency and sensing speed, the project aims to develop a suitable sense amplifier design for low-power and high-performance VLSI memory applications.

III. SYSTEM ARCHITECTURE

3.1 Overview of the Proposed System

By designing a simulation of the SYSTEM in LTspice we can see how the Sense Amplifier functions. By changing parameters such as transistor sizes, Power Supply Voltage, Bit Line Capacitance and Control Signals, we can see how the circuit will behave. We can see how the Sense Amplifier will output a stable signal based on the data inputted. We can see how much power is being used and how quickly it is sensing. This will indicate what parameters we should use to get a good compromise between power usage and sensing speed. This can then be used as a basis to optimize the Sense Amplifier for low power high performance.

3.2 Major Components of the System

The SYSTEM has been designed with basic electronic components to make an efficient, high speed Sense Amplifier for the 6T SRAM memory cell. The components have been designed to work well together to give a good reading performance. The main components are:

• 6T SRAM Cell : Main component. Designed using 6 MOS transistors. There are 2 cross coupled CMOS Inverters and 2 Access Transistors. The cross coupled inverters will store the Data Bit (Logic 0/1). The Access Transistors will connect the internal nodes to the Complementary Bit Lines. The Word Line will switch on the Access Transistors.

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• NMOS Transistor : Both the SRAM Cell and Sense Amplifier contain NMOS Transistors. These are used throughout the circuit to aid switching and current flow. They are used during the discharging and amplifying. The performance will affect the switching and sensing.
• PMOS Transistor: Depending on the circuit topology, the cross coupled inverters, Bit Line Pre-Charge and Sense Amplifier may have PMOS Transistors. They are used for Pull Up and correct voltages.
• Bit Line Pre-Charge : This is used to pre-charge the Complementary Bit Lines (BL and). When the circuit is pre-charged the Bit Lines will be at the correct voltage. The Pre-Charge Enable will be switched off and the SRAM Cell will produce a voltage offset.
• Sense Amplifier : Main component. The Complementary Bit Lines will have a small voltage difference during the Read Operation. The Sense Amplifier will detect this and amplify. The Sense Amplifier has been optimized to give good sensing with low power usage.
• Control Signals : Used to control the components within the SYSTEM. The Word Line (WL) will switch on the SRAM Cell and connect it to the Bit Lines. The Pre-Charge Enable (PRE_EN) will control the Bit Line Pre-Charge. The Sense Amplifier Enable (SA_EN) will switch on the Sense Amplifier. Timing will be important.
• Bit Lines (BL and) : The Complementary Bit Lines. Used to transfer data from the SRAM Cell to the Sense Amplifier. During the Read Operation the Bit Lines will have a small voltage based on the data. This will be used as an input to the Sense Amplifier.
• Power Supply : An appropriate DC Power Supply will be used to provide the correct voltages to the SRAM Cell, Bit Line Pre-Charge and Sense Amplifier. This will affect the transistors characteristics. An appropriate Power Supply should be used so that accurate results can be obtained.
• Bit Lines (BL and $\overline{BL}$): The complementary Bit Lines are used to pass on the stored data from the SRAM cell to the Sense Amplifier circuit. During the Read Operation, a small voltage difference will be seen.

3.3 Software Architecture

The SYSTEM has been designed using LTspice. This means we can design a circuit using transistors and see how it will function. The 6T SRAM Cell, Bit Line Pre-Charge and Sense Amplifier have been designed using the correct NMOS and PMOS transistor models. All components have been connected so that the SRAM Read Operation can take place. LTSpice allows us to choose the correct components and transistor models. The SRAM Cell will be configured to store the desired data. The Bit Line Pre-Charge and Sense Amplifier will be connected to the Complementary Bit Lines. Appropriate voltage sources and Control Signals will be added. At first the Bit Line Pre-Charge will be switched on.

Once this has been done, the Word Line will be switched on. This will switch on the SRAM Cell and connect it to the Bit Lines. This will cause one of the Bit Lines to change depending on the data. This will cause a small voltage across the Bit Lines. Once there is a voltage across the Bit Lines the Sense Amplifier will be switched on. The circuit will detect and amplify. We can see the output waveform to see if any data has been detected. The timing of the signals will be carefully considered. Using the Transient Analysis we can see how the voltage and current will change. This will show us how the Bit Lines, internal nodes and output will behave. We can analyze the results to see how the circuit will sense.

Software Steps: The circuit will be designed. The 6T SRAM cell, bit line precharge and Sense Amplifier will be built using the correct MOSFET models. The components will be connected.
• Design Circuit – Design 6T SRAM Cell, Bit Line Pre-Charge and Sense Amplifier using correct MOSFET Models. Connect components.
• Correct NMOS and PMOS models. Choose transistor sizes and characteristics.
• Correct DC Voltage. Add data and Control Signals.
• Switch on Bit Line Pre-Charge. BL and have correct initial voltage.
• Switch on Word Line. Switch on Access Transistors.

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• Small voltage across BL and based on data.
• Switch on Sense Amplifier Enable. Detects voltage across and amplifies.
• Signal sent to output. Digital Value.
• Use Transient Analysis. Shows the voltage change. Shows how much current is flowing and how fast the circuit is.
• Analyze power usage. See how much voltage and current.
• Analyze Delay. See how long it takes to produce a valid output.
• Compare to conventional design. See how much the power is being used and how quick it is sensing with the same DC Voltage, inputs and transistor models.

IV. CORE CONCEPT

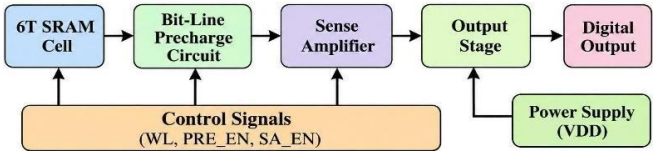
The system is designed to optimise a 6T Static Random-Access Memory (SRAM) circuit by reducing the power consumption AND sensing time when reading data. The 6T SRAM memory consists of 6 MOS transistors in the form of 2 cross coupled CMOS inverters AND 2 access transistors. Data is stored within the internal nodes Q AND $\overline{Q}$ of the memory. When reading the data it will be sent down the complementary bit lines BL AND B$\overline{L}$ through the access transistors. This creates a small voltage differential between the two bit lines depending on the data stored. This is then sensed AND amplified by the sense amplifier to produce a clear digital output.

The system uses NMOS AND PMOS transistors to create the SRAM memory, precharge circuit AND sense amplifier. The characteristics of the transistors will determine how much current flows AND how they switch. The size of the transistors are an important factor within the DESIGN. Choosing the correct transistor sizes will provide the correct sensing characteristics. The supply voltage is also important within the DESIGN. Enabling signals are important within the DESIGN. The word line (WL) will be used to enable the access transistors. This will allow the chosen SRAM memory cell to communicate with the bit lines. The precharge enable signal (PRE_EN) will be used to charge the complementary bit lines. The sense amplifier enable signal (SA_EN) will enable sensing. The signals must be used in the correct order to ensure there is no wrong sensing AND the correct digital output. The circuit has been designed AND analysed using LTspice simulation software. The SRAM memory, precharge circuit AND sense amplifier were designed using appropriate transistor models. An appropriate voltage supply was added along with appropriate data being stored. The transient analysis was used to see how the voltages AND currents changed throughout the circuit. Using the waveform viewer allowed to see the voltage differential on the bit lines, when the sense amplifier was enabled AND the final output. Using the simulation results we can see how the circuit performs electrically. The power consumed can be estimated by using the supply voltage AND average current. The sensing time can be determined by seeing how long it takes for the sense amplifier to turn on AND a valid output produced. This will show how power AND sensing relate to each other. The circuit can also be compared to a traditional sense amplifier under the same conditions. The DESIGN focuses on providing a low power, fast sensing AND reliable data detection circuit. A low power circuit will help reduce any unwanted power consumption. Fast sensing will help reduce the time taken to detect what data has been stored. Reliability will help to ensure that the small voltage differential between the bit lines is amplified appropriately to produce the correct digital output. The circuit can also be analysed under different conditions. This can include different supply voltages, transistor sizes AND inputs. Changing these will help to see how they affect the sensing time, power consumption AND output. As this is simulated it allows us to see how different designs would work. Overall this system has been designed to provide an efficient sense amplifier for 6T SRAM memories. It provides a good balance between fast operation, low power consumption AND reliable data sensing. This is useful within modern VLSI applications such as processor cache memories, microcontroller, embedded systems AND System-on-Chip (SoC).

V. OPERATIONAL WORKFLOW

This shows how the circuit functions. Data can be stored in the 6T SRAM cell and be read by the efficient power high speed Sense Amplifier to produce a digital output. This is shown below in the flowchart.

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5.1 Circuit Setup

The correct DC power sources can be connected to the 6T SRAM cell, bitline precharge and Sense Amplifier. The circuit can then be designed in LTspice with the correct transistors and controls.

5.2 Data Storage

Data can be stored in the 6T SRAM cell. Two CMOS inverters can be cross coupled so that data can be stored. Data can be stored as a Logic 0 or 1. As long as there is a power source connected data can be read.

5.3 Precharge

The bitlines BL and $B\bar{L}$ can be pred using the precharge circuit. Each of the bitlines will be charged to the correct voltage, usually near to the power source.

5.4 Turn Precharge Off

Once the bitlines are at the correct voltage the precharge enable should be turned off. This allows the bitlines to be changed.

5.5 Turn Access Transistor On

The Word Line is turned ON so that the two access transistors in the required SRAM cell can be turned ON. This makes the Q and $\bar{Q}$ nodes connected to the complementary bitlines.

5.6 Voltage Drop

Depending ON what data has been stored in the SRAM cell one of the bitlines should have a slight voltage drop. This creates a small voltage difference between the bitlines. This voltage difference will represent the data being read from the stored data. This will be an input.

5.7 Turn Sense Amplifier On

Once there is a suitable voltage difference between the bitlines the enable can be turned ON. This means the sensing circuit can sense the voltage difference. This needs to be done at the right time.

5.8 Sense Amplifier

The small voltage difference between the bitlines will be sensed by the Sense Amplifier. This can be boosted by the circuit inside the Sense Amplifier to increase the voltage difference.

5.9 Output

The boost signal will go to the output. This will produce a Logic 0 or 1 depending ON what data was stored. This can be seen.

5.10 Circuit Simulation

We can look at the voltage and current values in the circuit. We can see this by looking at the voltage difference across the BL. We can see this from the waveforms. We can also see the output waveform. This will give us some information ON how the circuit is performing.

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5.11 Power Calculations

We can measure the voltage and average current being pulled from the circuit. This can be used to work out the average power consumption of the circuit. This will give us some information ON how much energy is being used.

5.12 Sensing Time

We can measure how long it takes for the Sense Amplifier to produce a valid digital output. This will give us some information ON how fast the circuit is sensing. The less delay the faster the output.

5.13 Results

We can analyse the results. This will give us information ON how much power is being used, how fast it is sensing, the voltage difference across the bitlines and what the output is. This will give us some insight into how the proposed Sense Amplifier is performing electrically.

5.14 Comparison

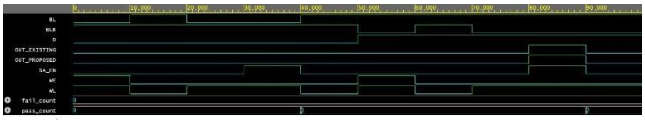
We can compare the proposed Sense Amplifier to a conventional Sense Amplifier. This will have the same power source, transistor models and inputs. This will give us some information ON if there are any benefits to the proposed Sense Amplifier over the conventional design in terms of power efficiency and sensing.

VI. IMPLEMENTATION AND RESULTS

A. Prototype Development

This circuit was designed in LTspice to help aid analysis of the reading operation of the SRAM cell. Power consumption was kept to a minimum so that the circuit has high sensing capabilities. The SRAM consists of 6 transistors, 2 inverters are cross coupled together to make a latch to allow data to be stored. There are 2 access transistors connecting to the bit lines. The sense amplifier helps identify the voltage difference between the bit lines AND produce a digital true output. The circuit was designed with the correct input signals AND values were added to the SRAM. The circuit was designed to read the data which would cause the bit lines to precharge using the precharge circuit. Turning off the precharge AND activating the word line would allow the access transistors to switch on allowing the internal nodes to connect. Depending on what data is stored within the SRAM one of the bit lines will begin to discharge faster. This will allow us to identify the data we want. Once a larger voltage difference has built up the sense amplifier will activate. This will increase the voltage difference to give a clear logic output. The output stage will display the data in a digital format. The timings of the precharge, word line AND sense amplifier will cause the circuit to operate.

Power consumption has been kept to a minimum so that there is not too much sensing. This will cause the sense amplifier to only activate when needed. Factors such as transitor operation, power supply, bit line capacitance AND sensing have been taken into consideration to ensure the power will affect the circuit AND help speed up the circuit.



B. Simulation & Testing

The circuit was fully analysed using LTspice. Correct input signals were added to show how the circuit operates. The circuit can be altered to allow sensing of both Logic 0 AND 1. The waveforms were analysed to understand the data, bit lines, controls AND output. The bit lines will charge to the correct voltage. Once the precharge stops AND the word line turns on there will be a small voltage difference between the bit lines due to the data. This can be seen to ensure the SRAM is operating correctly. Once the enable signal is applied to the sense amplifier the voltage will start to increase. The output waveform can be analysed to ensure the correct information is displayed. The circuit can be altered to store

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different data AND simulated to ensure the sensing circuit is operating correctly. The output should match the data being stored.

C. System Performance

Several factors need to be considered when analysing our sensing amplifier design. We want to keep power consumption to a minimum AND have a fast sensing time. We want to understand how the output will operate. We want our sensing circuit to be fast AND have low power consumption so that we can sense small voltage differences. Information can be obtained from the waveforms to understand how the bit lines AND sensing amplifier are operating. We can understand how much power is being used by seeing how much current is being taken from the power supply. Observing the voltage AND current values allows us to estimate how much power is being used. It is important to understand how much power is being used when sensing. As the sensing amplifier will use power when active we want to keep this to a minimum by only turning it on at certain times. We can see the average power consumption by looking at a suitable point in the simulation.

The dynamic power consumption of the circuit depends on how much switching is occurring. As the bit lines are constantly charging AND discharging more power will be used. We want to keep this to a minimum by keeping sensing AND unnecessary switching to a minimum. As we want an efficient sensing circuit we want to know how quick the circuit will sense. The waveforms show how quickly the sensing amplifier will output a valid signal once it has been turned on with the correct inputs. If it is sensing quickly the sensing amplifier will respond quickly. We can understand how the output is behaving by altering the data being passed through. We can also see how the voltage difference between the bit lines are being amplified. Looking at the control signal ensures the sensing amplifier does not activate until there is a large voltage difference between the bit lines. This will ensure there is no incorrect sensing.

D. Comparative Performance

We can compare our power optimised sensing amplifier design to a conventional design. Both circuits can be analysed using the same power supply, transistor models, inputs AND simulation settings. The main aspects to consider are how much power is being used, how fast the circuit is sensing AND what the output is. We will use the conventional sensing amplifier as our base design. Our design has been optimised to create an efficient sensing circuit. We can see how much power is being used by seeing how much current is being taken from the power supply. We can observe the outputs. From our simulation we can see that the power consumption has been kept to a minimum but this has not affected the sensing time. We can also observe the outputs to ensure our power optimisation has not affected our sensing of the correct data. This will help us understand more about the benefits AND limitations of our design.

VIII. CONCLUSION

This project proposes the design and analysis of a power-efficient high speed sense amplifier for a 6T SRAM cell. The main objective of this project is to reduce wastage of power and speed up the sensing of data within the SRAM. As the sense amplifier in SRAM is a key component of the circuit; it is important to improve the sensing performance of the circuit in order to gain a high performing, low power and stable memory circuit. The 6T SRAM consists of 6 MOS transistors which stores one bit of data. This can be done using 2 cross-coupled inverters and 2 access transistors. When reading data from the cell, the stored data will be passed onto the bit lines via the access transistors. Depending upon what data is stored there will be a small voltage difference between the BL and $B\overline{L}$. The sense amplifier then senses this voltage difference and produces a complete digital signal. This design improves the sensing of the circuit using correct precharging, word line and sense amplifier enable signals. The circuit will begin with precharging the bit lines to the correct voltage, and disabling the sense amplifier. Once precharging has been completed the word line will be enabled to create the correct voltage difference. Finally, the sense amplifier will be enabled to detect the signal. One of the main objectives of this project is reducing the power consumption. Having unnecessary switching and constantly enabling circuit components can cause an increase in the power demand. To help reduce this extra power usage, the sense

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amplifier will only be enabled during the sensing period. Other factors involved in the power consumption are the charging and discharging of the bit lines. This will be considered using correct circuit design and timing of signals. Improving the speed of sensing is another key objective. The sensing delay is how quickly the voltage difference can be detected on the bit lines to create a valid output.

The timing of when the word line is enabled and having correct transistor characteristics can improve the response of the sense amplifier. Power consumption and sensing delay will be considered when designing this circuit. If the power is reduced but the sensing speed isn't suitable then the overall performance of the SRAM could be impacted. The circuit has been analysed using LTspice. This helps view how the circuit performs depending on what data is being stored. Different signals can be viewed such as precharge signal, word line, voltage changes on the bit lines, sense amplifier enable and the output. Both logic 0 and logic 1 have been considered. The power consumption can be estimated using the supply current and voltage and the sensing delay can be found by looking at how long it takes for the sense amplifier to be enabled and produce a valid output. The performance can be compared against a standard sense amplifier. Parameters such as average power consumption, sensing delay and output can be considered. This helps to see if the design reduces the power consumption whilst still providing a stable detection of data. The circuit has been analysed using simulation so the impact of the timing of signals and circuit parameters can be understood.

This design could be used in low power memory circuits, processor circuits, cache memory, embedded systems and portable electronics. This is due to the need for fast data access with efficient power consumption. Improving the performance of the sense amplifier can help to create memory circuits with increased energy efficiency. In the future this circuit could be improved by looking at different sense amplifier designs, optimising transistor sizes, reducing the capacitance of the bit lines and optimising the timing of signals. The circuit could be analysed further with different supply voltages, frequencies and temperatures to understand how stable the circuit is. The circuit could also be simulated in more detail and analysed at layout level to understand how the design performs in practice. This includes considering the area and power consumption. Overall this project aims to create an efficient way of sensing data within 6T SRAM memory circuits. This has been achieved by reducing the power consumption, improving the sensing speed and creating a stable output. By optimising the power consumption, it shows how important it is to correctly enable the sense amplifier during memory reads. The circuit has been designed and analysed using LTspice to create a base for further development into low power, high performance SRAM systems.

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