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A Multibit Storage Element for Power Minimization in Sequential Logic System

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Abstract: *Power consumption is an important issue in modern high frequency and low power VLSI design. In modern VLSI designs, power consumed by clocking is taken as a major part of the design. The storage elements of designer considerations are Latches and flip flops. One way to boost the flip-flop performance is to combine the clock pulse given to MBFFs. The multi-bit flip-flop is configured by a single clock pulse thereby supporting the same functionality as that of two Single bit Flip-Flops. In the proposed work, the result of the power dissipation is compared with that of the conventional D Flip-Flops. The Sequential logic system is coded using Verilog using Vivado design suite. Simulator and it has been concluded from the comparison that the clock buffer, the number of flip-flops used, by using MBFFS..*

Keywords: Flip-Flops, Multi-bit Flip-Flop, Power Dissipation, Clock Gating, Low Power Techniques

I. INTRODUCTION

Recently, the multi-bit flip-flop (MBFF) technique was introduced as a way for reducing the facility consumption and chip area of integrated circuits (ICs) [1] during the physical implementation stage of their development process. From the attitude of the buyer, the most requirements for such an optimization method are high performance, low power usage and little area (PPA). Therefore, any new optimization technique should improve a minimum of one, if not all, of those requirements. This paper proposes a replacement low-power methodology, applying a MBFF merging solution during the physical implementation of an IC to realize better power consumption and area reduction. The aim of this study is to prove the advantage of this system on the facility saving capability of the system while demonstrating that the proposed methodology doesn't have a negative impact on the circuit performance and style routability. The experimental results show that MBFF merging of 76% can be achieved and preserved throughout the entire physical implementation process, from cell placement to the final interconnection routing, without impacting the system's performance or routability.

II. THEORETICAL BACKGROUND

This section deals with theoretical concepts related to power dissipation, power reduction techniques and the applications of the sequential circuit

2.1 Power Dissipation

Power dissipation is the process by which an device produces heat, energy loss or waste as an unbidden derivatives of its prime actions. In the circuit, the power dissipation outcome always results in the increase of the temperature which affect the device in both the conditions, circuit in operating mode or when the circuit isn't operating mode [1]. The number of intrinsic carriers tends increases, when the circuit is turned off. The minority charge carrier concentration based on the factors, temperature and leakage current. This when drainage current increases it turn rise in temperature as a result the device might collapse. The different kinds of power dissipations are Static power dissipation and dynamic power dissipation. Static power dissipation occurs in steady state due to the outflow of current through the transistors in the design when supply voltage is applied[2]. Dynamic power dissipation is the Logic transitions cause gates to charge and discharge load capacitance. This type of power dissipation occurs due to transistors switching activities.

2.2 Clock Gating

To reduce the dynamic power dissipation we apply a approach to switch off the clocks, when it is avoided. In this method to shut off and to prevent the wastage of switching power dissipation, during the optimal period. The clocks are

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disabled to Ideal function which rescue the power. When the clock is on, during the ideal period it causes the different issues like, clock loading and may cause the false logic activity. In clock gating methodology, an XOR-related lock gating is established to every available flip-flop, the gating circuit analyze both the output and input, and checks if input and output are identical or not[2]. When the signals are not matching then the clock is applied to the circuit. The clock gating can be used as a technique to decrease the power when the further gating can't be during synthesis.

2.3 Multibit Flip-flop

Multibit flops are used to lower the power without influence the performance of the design. Multibit flops are applied to develop switching power generally in clock networks. The multibit flip-flop can decrease the power usage as they have a common inverter with the flip-flop. The clock skew can be reduced with certain conditions to meet the requirements[3]. To obtain a multibit flip-flop from a single bit flip-flop, both the flip-flop should have a matching condition of clocks and reset or set condition. The one-bit delay flip flop and the delay latch are near but the output of delay flip flop has the state of input additionally the positive edge clock movement, thus the clock delays by one cycle. The multibit flip-flop takes further number of inputs and the output conclude in different number of outputs[4]. During the active state of the clock the flip-flop circuit latches the input and the output appropriately. The flip-flop carries the data in inactive state.

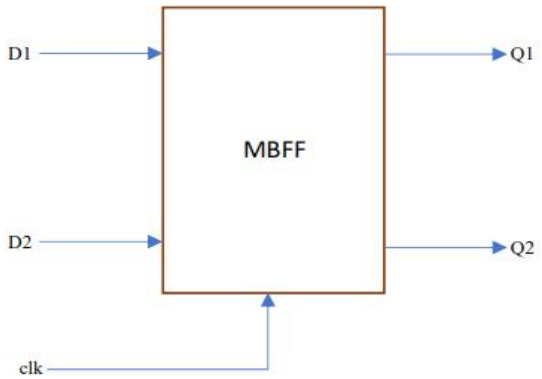

Figure 1: Multibit Flip Flop

2.4 Merging of Flip-flops

Figure 3 shows an example of merging two individual one-bit flip-flops into one 2-bit flip-flop. If we change the two individual 1-bit flip flops as shown in Figure 2 by the 2-bit flip-flop as shown in Figure 3, the total power consumption can be minimized because the two 1-bit flip-flops can dividend the same clock buffer [5]. However, the placement of some flip-flops would be swap after this replacement, and thus length of wires of connecting pins to a flip-flop are also altered. To avoid violating the timing restrictions, we constraint that the length wires of nets connecting pins to a flip-flop cannot be extended than described values after this process. Besides, that a new flip-flop can be set down within the desired region, we also required to consider the area volume of the domain. Minimization of dynamic clock power guides the way to merge the SBFF and constructed MBFF.

By combining single-bit flip-flops into a single multi-bit flip-flop, duplicate inverters can be avoided, and the overall clock dynamic power consumption can be reduced[6]. Additionally, the total area contributing to flip-flops can be minimized

- The clock in consecutive banked components consumes less power, resulting in lower power consumption.
- Smaller area and delay, due to shared transistors and optimized transistor-level layout.
- Reduced clock skew in sequential gates.

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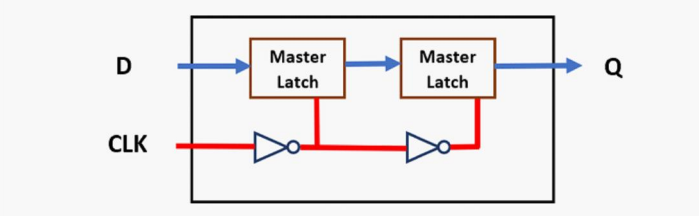

Figure 2: 1-Bit Flip Flop

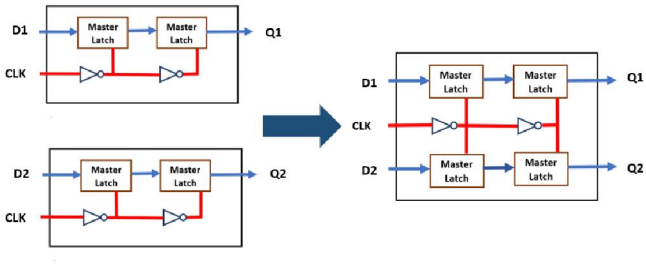

Figure 3: 2-Bit Flip Flop

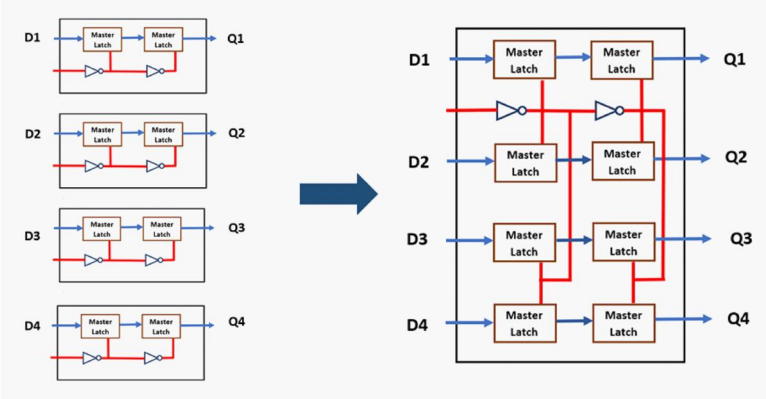

Figure 4: 4-Bit Flip Flop

2.5 Benefits of MBFF

- Total length of clock tree is minimized, this effects in reduction of clock tree buffers and clock tree power. Clock tree buffer level depletion improves overall balanced design skew.
- Area of multibit flip flops is less than two single flip flops because transistor level escalation of cell layout, which includes shared logic and power supply.

III. Literature Survey

Clock power is the major grantor to dynamic power for modern integrated circuit design [6]. A conventional single-bit flip-flop uses an inverter series with a high drive stability to operate the clock signal. A bunch of several such cells and forming a multibit flip-flop can share the operate strength, area of the inverter chain, dynamic power, and can even retain the clock network power and facilitate the skew control [7]. Hence, we focus on post placement MBFF grouping to gain these benefits.

Digital System Clocking is assuming ever larger importance as clock speeds increase. The method simultaneously performs, timing and activity occupying net weighting that lower net switching power by appointing a combination of timing weights and activity to the nets with higher switching rates or critical timing[8]. The gate control logic optimizes that set the gate enable signal higher if a register is active for a number of successive clock cycles. Experimental results will show that our outlook is able to reduce the power and total wire length of clock tree greatly with minimal overheads.

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IV. Existing Methodology

The problem of using multi-bit flip-flops to minimize power consumption in the post-placement level. They use the graph base method to deal with this issue. In a graph, each node defines a flip-flop. If two flip-flops can be restored by a new flip-flop without break the timing and capacity constraints, they build a border between the corresponding nodes. After the graph is construct, the problem of renewal of flip-flops can be solved by finding an m-clique in the graph. The flip-flops corresponding to the nodes in an m-clique can be restored by an m-bit flip-flop. They use the branch-and-bound and backtracking algorithm to discover all m-cliques in a graph. Because one node (flip-flop) may hand of to several m-cliques (m-bit flip-flop), they use ravenous heuristic algorithm to discover the maximum independent set of cliques, which every node only hands of to one clique, while finding m-cliques groups.

V. Proposed Methodology

This proposed methodology is depend on which gives the idea of fusing clock pulse. The working of single-bit D flip flop is same to the D latch omitting that the output of D Flip Flop grasp the state of the D input at the minute of a positive edge at the clock pin or negative edge [9] when clock input is active low and retard it by one clock cycle. Thus it's commonly called as delay flips flop. The D Flip-Flop can be demonstrated as a delay line or zero order hold. The betterment of the D flip flop on top of the D-type "transparent latch" is the signal on the D input pin is grasped the moment the flip-flop is clocked [10][11], and consequent changes on the D input will be neglected until the next clock event. From the timing aspect it is clear that the output Q changes only at the positive edge. At each positive edge the output Q becomes equal to the input D at that moment and this value of Q is carried until the next positive edge [12][13]. Multi-bit Flip Flop which hold multiple data input and gives solution in multiple data output. The MBFF operates similarly to the SBFF in that it latches all input to output whenever the clock enters the mobile active state[14][15]. For inactive state the flip flop holds on the data.

This paper experimented the proposed technique by designing multibit flip flops 2-bit flipflop, 4-bit flipflop, 8-bit flipflop individually compared the power with the multibit flipflops using clock gating technique. We can analyze both normal flip flop and clock gated flip flops work powers where the power dissipation or consumption reduced or not.

VI. Experimental Results

This section shows experimental results of proposed method. This date is implemented in Viva do software tool. The power of MBFF and FF using clock gating compared and is shown in Table I.

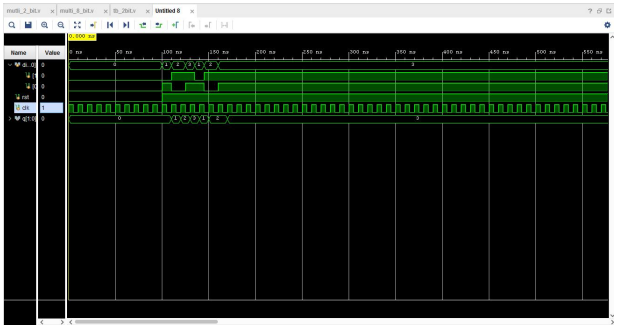

Figure 5: 2-Bit MBFF without clock gating

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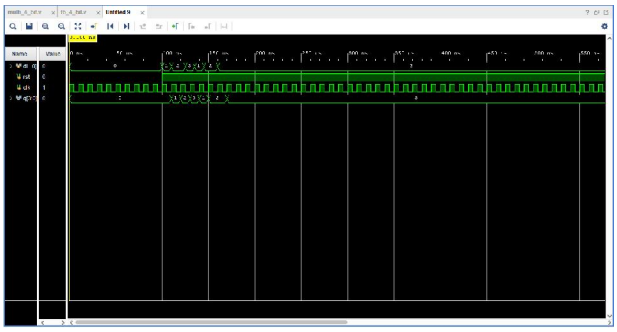

Figure 6: 4-Bit MBFF without clock gating

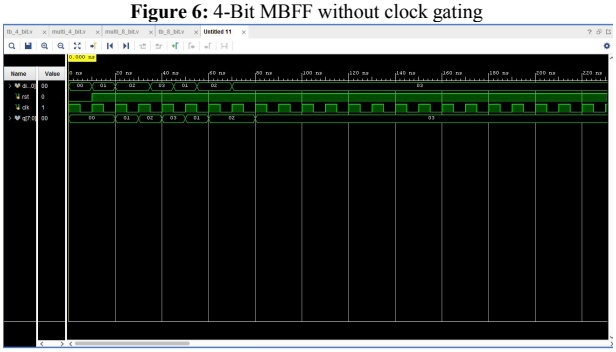

Figure 7: 8-Bit MBFF without clock gating

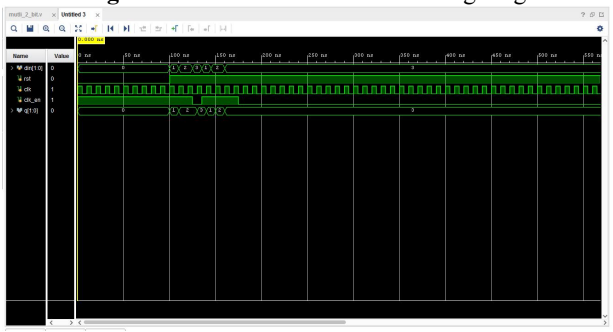

Figure 8: 2-Bit MBFF with clock gating

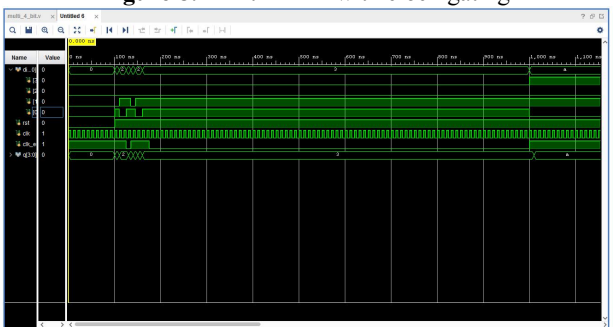

Figure 9: 4-Bit MBFF with clock gating

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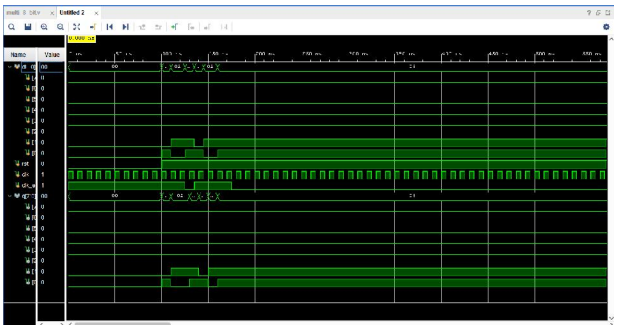

Figure 10: 8-Bit MBFF with clock gating

Table 1: Power comparison of proposed method

S.NO	Power comparison		
	MBFF without clock gating	***Dynamic power***	***Static power***
1.	2-bit multibit flipflop	80%	20%
2.	4-bit multibit flipflop	89%	11%
3.	8-bit multibit flipflop	81%	19%
S.NO	**Power comparison**		
	MBFF with clock gating	***Dynamic power***	***Static power***
1.	2-bit multibit flipflop	44%	56%
2.	4-bit multibit flipflop	56%	44%
3.	8-bit multibit flipflop	70%	30%

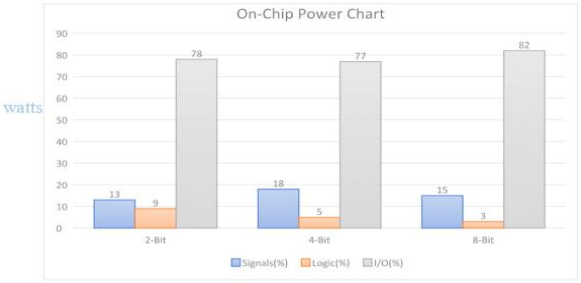

Figure 11: Power consumption comparison.

The implemented result shows that power reduction can be done upto maximum of 15-40%.

VII. Conclusion

The proposed design is to minimize the number of flip flops using multi-bit flip-flops. Multibit flops offer a smart way to lowers the overall power of the design without affecting the timing[16]. Usage of multibit flops lowers the leakage power and the dynamic power by decreasing the clock tree cells and holding the buffers required in the design. It also helps in improving the density of the design by decreasing the standard cell area, and thereby enhancing the block size. The work has proceeded with a Verilog based code for constructing combination table of flip flops compared power with the clock gating fused flipflops. We here conclude the design and implementation of 2-bit, 4-bit and 8-bit flip flops with ICG and compared with MBFF. Next process to implement MBFF in applications like Reversable counter, Johnson counter or Modulo counter.

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