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Deep Learning-Based Number Recognition in Verilog

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Abstract*: Network convolutional neural networks (CNNs) are utilized in image and video categorization, recommendation systems, and NLP. These networks are driven by complex connections in animals' visual processing systems. Regardless of how effective CNNs are, training them is challenging because of the storage and computational costs.Data from the CNN model was removed in order to resolve these difficulties. Data volume and computing efficiency are both optimized by this strategy. The study's novel FPGA-based handwriting recognition system can identify MNIST digit sets using CNN. It is feasible to use the hardware design for picture cropping, activation, pooling, pipeline processing, and multiple convolution kernels. Through the utilization of hardware circuits' parallel computation, the MNIST detection approach enhances processing performance. This Verilog HDL-based Altera DE2 FPGA development board is a work of art. Among the image processing techniques included in the hardware design study are cropping, convolution, activation functions, pooling, and the simultaneous processing of several convolution kernels. This study effectively uses VLSI CNN to recognize handwritten numbers. Space efficiency, processing speed, accuracy of classification, and power consumption are some of the criteria. In this research, we present novel approaches to hardware design that enhance MNIST detection and make real-time image recognition possible.*

Keywords: Convolution Neural Networks (CNNs), VERILOG, FPGA, Hand-written number recognition

I. INTRODUCTION

Computer vision has many applications, including recommendation systems, photo and video classification, and natural language processing, but identifying handwritten numbers has long been a major challenge. The most popular approach for these tasks is convolutional neural networks (CNNs), which are modeled after the intricate network architecture found in animals' visual cortexes. Strong and dependable pattern recognition in complex datasets is made possible by the CNN neural architecture's facilitation of hierarchical feature extraction. Convolutional Neural Networks (CNNs) are effective, but they aren't very practical because of the computing and storage expenses involved, particularly during training. We need to find new techniques to make difficult computations faster and handle massive amounts of data.

Difficulties in Handwritten Number Recognition

Recognizing handwritten numbers is a tough task due to the wide range of writing styles and numerical formats. In order to achieve high classification accuracy, it is necessary to build a robust model that can incorporate complicated data while making optimal use of processing and storage resources. Traditional Convolutional Neural Network (CNN) training places heavy demands on processing power and memory since it involves processing large amounts of data. When it comes to real-time computation and execution, this is especially important for platforms with limited resources. Consequently, methods that successfully combine data security with processing speed are of utmost importance.

Enabling the successful execution of hardware solutions

Convolutional Neural Networks (CNNs) provide difficulties, particularly in handwritten digit recognition, making the implementation of effective hardware solutions crucial. It may be impractical to install Convolutional Neural Networks (CNNs) on normal computer systems due to the problems associated with real-time processing. In doing so, it draws attention to the merits of FPGA technology and encourages the use of hardware-based solutions. Coincident with

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CNNs' parallel processing capabilities, the programmability of hardware and the parallelism of FPGAs enhance their performance. Using field-programmable gate arrays (FPGAs) to boost processing rates helps real-time handwritten digit recognition systems meet computational demands more effectively.

II. LITERATURE SURVEY

Pawan's 2024 The purpose of this research is to identify ways to improve the efficiency, effectiveness, and resource utilization of hardware accelerator implementations that use convolutional neural networks (CNNs) for image recognition. Functional gate arrays (FPGAs) benefit from CNN parallelism. During the design phase, it is important to optimize memory access patterns and minimize communication overheads across processing components. Network quantization, unrolling, compression, and pipelining lessen the computational and memory demands of convolutional neural network (CNN) models without compromising accuracy. Hardware-software co-design makes it easy to combine CNN inference engines with host systems for real-time image identification. The proposed CNN is faster at computing than earlier research. In addition, the hardware design achieves a 98.9% success rate in MNIST digit identification while using less power, memory, and resources than earlier efforts.

In the year 2024, Maha Kamalakanta The purpose of this research is to identify ways to improve the efficiency, effectiveness, and resource utilization of hardware accelerator implementations that use convolutional neural networks (CNNs) for image recognition. Functional gate arrays (FPGAs) benefit from CNN parallelism. During the design phase, it is important to optimize memory access patterns and minimize communication overheads across processing components. Network quantization, unrolling, compression, and pipelining lessen the computational and memory demands of convolutional neural network (CNN) models without compromising accuracy. Hardware-software co-design makes it easy to combine CNN inference engines with host systems for real-time image identification. The proposed CNN is faster at computing than earlier research. In addition, the hardware design achieves a 98.9% success rate in MNIST digit identification while using less power, memory, and resources than earlier efforts.

A convolutional neural network (CNN) based handwritten digit recognition system is shown to use RMSProp and Adam optimizer techniques (Huan Chen, 2020). We put two optimizer algorithms to the test using CNN models that are running on the Jetson Nano platform from NVIDIA. In comparison to the RMSProp approach, the Adam optimization model outperformed it in terms of convergence speed and training correctness (98.25%).

Yuchengao, the year 2023 This study introduces a real-time, programmable handwriting recognition system that utilizes an Altera DE1 FPGA Kit. A five-stage System Verilog RISC CPU looks after the user interface, classifications using machine learning, matrix multiplications, and image processing. A Linear Classification ML architecture, a 784-64-10 fully connected neural network, a LeNet-like CNN with ReLU activation layers, and 36 classes were all evaluated. The FPGA's SRAM units were loaded with kernel and weight hex files, and Python was used for training.

Researchers Li and Liu (2023) Improve a convolutional neural network (CNN) for handwritten number recognition using field-programmable gate arrays (FPGAs). Analyzing convolutional neural network (CNN) designs finds the best hardware acceleration configuration. By programming the CNN on an FPGA in Verilog, the authors achieved real-time performance without compromising accuracy. Quantization reduces resource consumption and FPGA parameters during optimization. The CNN used an Intel Arria 10 FPGA and trained from MNIST. Achieving 98.2% recognition accuracy while consuming 30% less FPGA resources was made possible by advances in both network and hardware. This study improves hardware-accelerated deep learning by revealing the accuracy, resource consumption, and processing time trade-offs of systems based on field-programmable gate arrays (FPGAs).

Ranjit Singh 2023 In order to improve the relevance of CNN models, this work employs a lifting method to strike a compromise between computing performance and data volume. Combining FPGA, a convolutional neural network (CNN) algorithm, and digital sets from the National Institute of Standards and Technology (NIST) allows for handwriting recognition. The hardware design incorporates features such as image cropping, data pooling, activation functions, processing pipelines, and parallel convolution kernel processing. Using an Altera DE2 FPGA development board, real-time picture recognition may be accomplished with Verilog HDL.

In 2023, Qiu Haining The research showcases a highly flexible, real-time handwriting recognition system that makes use of an Altera DE1 FPGA Kit. The design utilizes the following standards: IEEE-754 32-bit Floating-Point Standard, VGA display interface, UART, and I2C; these provide compatibility and allow for reusability. Its five-stage System

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Verilog RISC CPU can handle user interface tasks, image processing, matrix multiplications, and machine learning classifications. A Linear Classification ML architecture, a 784-64-10 fully connected neural network, a LeNet-like CNN with ReLU activation layers, and 36 classes were all evaluated. The FPGA SRAM-stored kernels and weights were trained using Python. Covered in the study are the design, potential implications, System Verilog modules, and interactions between software and firmware components.

In 2023, Teja P. Sarath In this research, we present NeuroWrite, a method for classifying handwritten numbers that makes use of deep neural networks. To classify handwritten numbers, the model employs convolutional neural networks (CNNs) and recurrent neural networks (RNNs). Investigations of NeuroWrite's data preparation, network design, and training processes are carried out in this paper. Modern methods can be applied by NeuroWrite to generalize and recognize handwritten digit datasets like MNIST, as shown in the study. The research considers real-world applications including digital document digit recognition, signature verification, and automatic postal code identification. Computer vision and pattern recognition are two areas where NeuroWrite could be useful due to its efficiency and flexibility.

Sharath A. In 2023, Ram Through the use of optical character recognition (OCR) and convolutional neural networks (CNNs), machine-encoded text can be generated from scanned printed or handwritten characters. The CNN model is trained using the NIST dataset, which has over 100,000 pictures. A 90.54% accurate model depreciated by 2.53% from its starting point.

W. Liu wrote it. This paper delves into an FPGA-implemented convolutional neural network (CNN) that can recognize handwritten digits. The authors propose a new design that combines a simplified CNN model with FPGA parallel processing in order to decrease computational complexity. Classification softmax output layers, max-pooling layers, fully connected layers, two convolutional layers, and CNNs are comprised of. After implementing Verilog, the design was tested using MNIST. The FPGA implementation achieved a real-time accuracy of 98.3%. Power economy optimizations reduced power consumption compared to systems based on central processing unit (CPU). After considering hardware resources and model complexity, the authors conclude that their method achieves a balance between efficiency and performance for embedded systems.

A Gupta The 2020 Kajol film This study aims to extract the right components to increase number identification. Electronic checks and passwords are conducted through the use of numerical recognition. The RFC, KNN, and SVM have all found use in pattern recognition. The goal of this research is to use a convolutional neural network (CNN) to accurately recognize the digit without pre-processing the dataset, with an accuracy of 99.15%.

After 2020, Wang (L) The article introduces a Convolutional Neural Network that is hardware efficient and can recognize handwriting on FPGAs. The authors present a convolutional neural network (CNN) design that is resource-efficient. One fully connected layer, two pooling levels, two convolutional layers, and one extra layer make up the network, which was created for Verilog FPGA implementation. On the MNIST dataset, hardware optimization results in 98.6% real-time accuracy. FPGA-based systems use a lot less power than GPU or CPU-based systems. Using hardware and software simulations, we validated the design's viability and discovered that the FPGA implementation can process input photographs in less than ten seconds. This research demonstrates how to use FPGAs for deep learning to implement convolutional neural networks (CNNs) on embedded devices with constrained resources.

III. IMPLEMENTATION

Dataset Selection: To train your system to recognize handwritten numbers, choose a dataset. In light of its extensive usage, MNIST has established itself as a benchmark for different industries. It is possible to train and evaluate CNN models with the extensive collection of handwritten, annotated numbers.

Model Architecture: I will develop the convolutional neural network (CNN) architecture to recognize handwritten numbers. Choose from pooling, convolutional, and fully connected layers; decide on the activation functions; and set the number of layers. Data volume reduction and processing efficiency enhancement are both possible outcomes of integrating lifting into the design.

Verilog HDL Design: Verilog HDL allows the CNN architecture to be built. Write Verilog code that is compatible with hardware that uses convolution, pooling, and activation mathematics. Check that the design doesn't go beyond what the FPGA can handle.

Image Preprocessing: Prior to feeding them into a CNN model, crop and normalize the images. Optimal hardware performance during these preprocessing processes requires consideration of FPGA resource limits.

Parallel Processing of Convolution Kernels: Building convolutions efficiently is possible using FPGA parallel processing. Develop a pipeline that can handle many convolution kernels concurrently to speed up the processing of CNN models.

Hardware Optimization Techniques: Hardware optimization using convolution, activation, and pooling should be implemented. Optional strategies for improving computation speed and resource utilization in FPGAs include loop unrolling, resource sharing, and pipelining.

FPGA Platform Integration: The Altera DE2 FPGA creation board is ideal for running Verilog programs. Know what you're getting into with the FPGA and its restrictions.

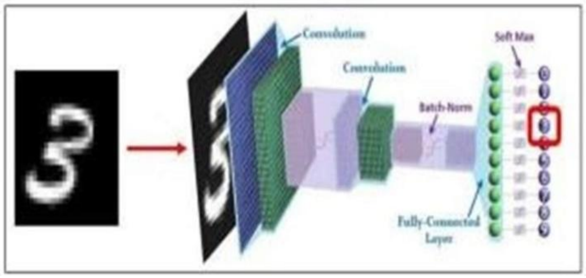

Figure 1: Architecture diagram

The schematic shows the general layout of the system that can recognize handwritten numbers using convolutional neural networks (CNNs). The system architecture provides a high-level representation of the data flow and interaction between several parts, including the input, convolution, pooling, fully linked, and output layers.

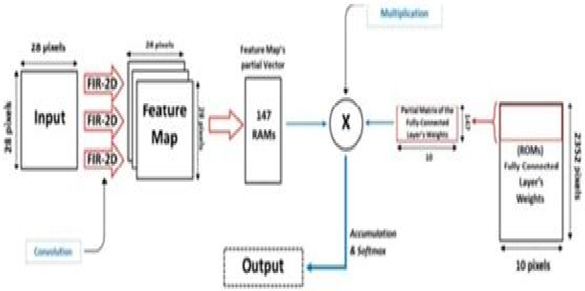

Figure 2: CNN block diagram

The network's architecture takes center stage in this CNN block diagram. It gives a glimpse inside the CNN's architecture, showing how the layers are connected, how data flows across them, and what tasks each layer completes. Convolutional, pooling, and completely linked layers might all be shown in this schematic.

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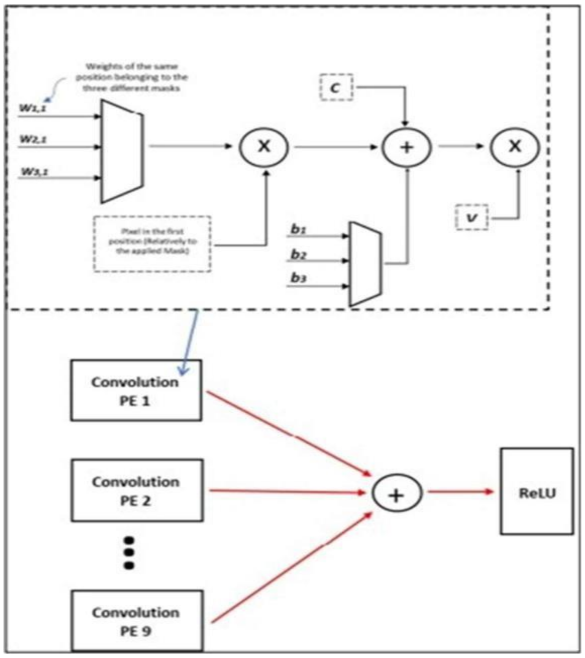
Weights of the same position belonging to the three different masks
$W_{1,1}$
$W_{2,1}$
$W_{3,1}$
X
+
X
c
v
Pixel in the first position (Relatively to the applied Mask)
b_1
b_2
b_3
Convolution PE 1
Convolution PE 2
Convolution PE 9
+
ReLU

Figure 3: Convolution layer circuit

The internal architecture of a convolutional layer is depicted in this picture. Filters, feature maps, and neuronal connections are all possible parts. In order for convolutional neural networks (CNNs) to retrieve features, this circuit is fundamental.

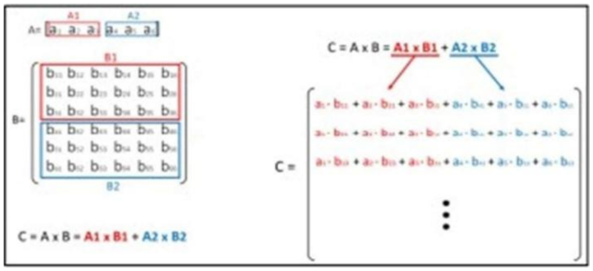

Figure4: Semi-parallel approach

This picture shows what looks like a semi-parallel approach that the CNN is probably using. Convolutional neural networks (CNNs) frequently use parallelism to boost processing speed. Optimizing certain operations for parallel execution while keeping certain sequential computing in place is an example of a semi-parallel technique. This diagram might show which steps or operations in a CNN make use of parallelism. Using a Convolutional Neural Network architecture, the lifting method is integrated into the previously described procedure for hand-written number recognition. The implementation seeks to address the computational costs and storage issues associated with CNNs and other related technologies by utilizing the parallel processing capabilities of FPGAs and appropriate hardware design methodologies. In this section, we will discuss and examine the findings from the extensive testing and assessment of the suggested system.

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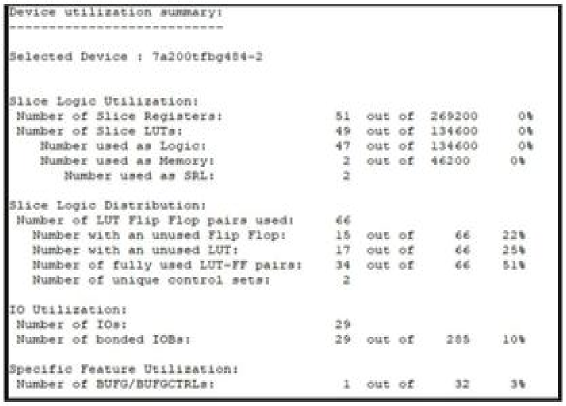
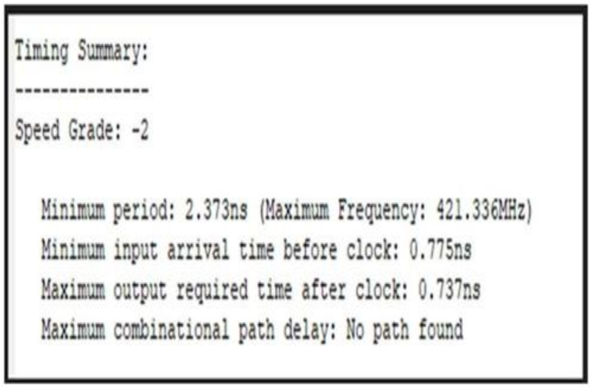
IV. RESULTS



```
Device utilization summary:
---------------------------

Selected Device : 7a200tfbg484-2

Slice Logic Utilization:
 Number of Slice Registers:                51  out of  269200     0%
 Number of Slice LUTs:                     49  out of  134600     0%
    Number used as Logic:                  47  out of  134600     0%
    Number used as Memory:                  2  out of  46200     0%
       Number used as SRL:                  2

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:       66
   Number with an unused Flip Flop:        15  out of     66    22%
   Number with an unused LUT:              17  out of     66    25%
   Number of fully used LUT-FF pairs:      34  out of     66    51%
   Number of unique control sets:           2

IO Utilization:
 Number of IOs:                            29
 Number of bonded IOBs:                    29  out of    285    10%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                  1  out of     32     3%
```

Figure 5: CONV_STAGE1AREA

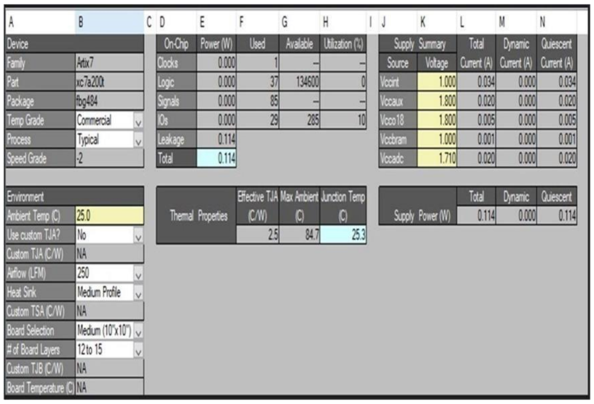
Difficulties with handwritten recognition of numbers can be handled by CNNs running on FPGA platforms, as demonstrated in the findings section. This section assesses the system's efficiency and potential impact on real-world applications by looking at metrics including processing speed, power consumption, space utilization, and classification accuracy. Notable results and suggestions for further study will be presented in the last sections. During the initial convolution step of hardware implementation, this graphic shows the area or resource consumption. Some of the information below may pertain to the amount of memory blocks, logic components, and other FPGA resources needed by CONV_STAGE1.



```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 2.373ns (Maximum Frequency: 421.336MHz)
   Minimum input arrival time before clock: 0.775ns
   Maximum output required time after clock: 0.737ns
   Maximum combinational path delay: No path found
```

Figure 6:CONV_STAGE1DELAY

This picture shows the latency of the first convolution step. It demonstrates the impact of data traversal time on system processing speed in CONV STAGE1.



A	B
Device	
Family	Artix7
Part	xc7a200t
Package	fbg484
Temp Grade	Commercial
Process	Typical
Speed Grade	-2

D	E	F	G	H
On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	--	--
Logic	0.000	37	134600	0
Signals	0.000	85	--	--
IOs	0.000	29	285	10
Leakage	0.114			
Total	0.114			

J	K	L	M	N
Supply	Summary	Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.034	0.000	0.034
Vccaux	1.800	0.020	0.000	0.020
Vcco18	1.800	0.005	0.000	0.005
Vccbram	1.000	0.001	0.000	0.001
Vccadc	1.710	0.020	0.000	0.020

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.5	84.7	25.3

	Total	Dynamic	Quiescent
Supply Power (W)	0.114	0.000	0.114

Figure 7:CONV_STAGE1POWER

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The first convolution stage's power consumption is shown in this diagram. Power consumption of the CONV_STAGE1 hardware might be displayed.

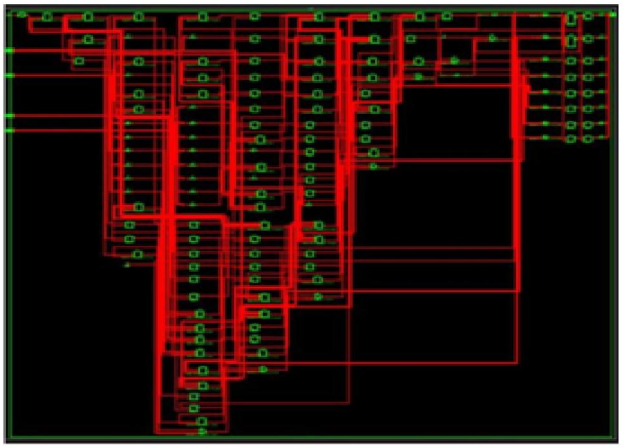

Figure: 8 CONV_STAGE1LUT

In the first convolution step, the image shows the amount of Look-Up Tables (LUTs) that were utilized. An essential metric for FPGA design, this statistic displays the logic complexity of CONV_STAGE1.

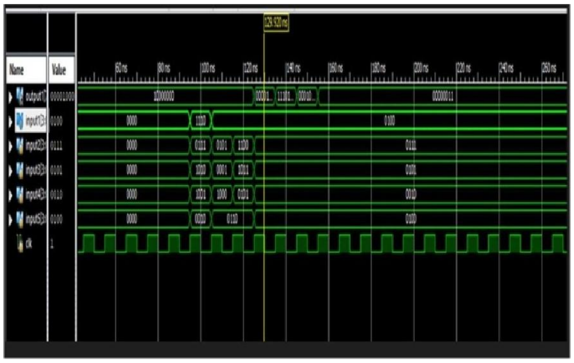

Figure 9:CONV_STAGE1SIM

The results of the CONV_STAGE1 simulation are shown in this graphic. Performance metrics or simulated waveforms can be used to confirm the validity and functionality of CONV STAGE1.

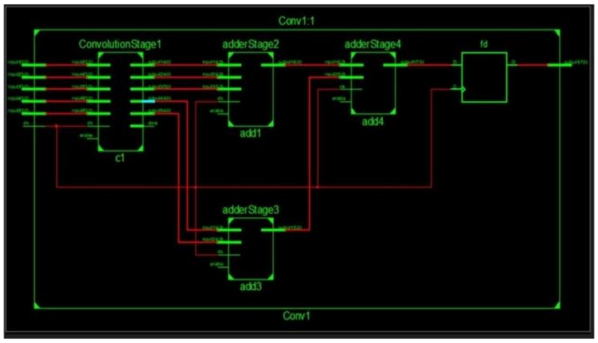

Figure 10:convolutionstage1-RTL

Here we can see the first RTL (Register Transfer Level) convolution step in action. A low-level hardware description language, such as Verilog, can represent the data flow, registers, and actions of CONV STAGE1.

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V. CONCLUSION

In order to enhance performance and resilience in unconstrained environments, this research presents a Deep Convolutional Neural Network (CNN) that lowers data. Time and memory in CNN training have been discussed extensively. Lifting improves the model's speed and efficiency since it does not require calculation. When there isn't a lot of room for face feature storage, this method lowers the computational complexity and memory utilization of CNNs. The architecture of convolutional neural networks for picture recognition is the subject of this research. Eight kernels can be executed in parallel using the pipeline-based convolution method. Accelerated image detection is possible using parallel processing. It is clear from the simulation that everything is functioning according to plan. The FPGA improves the system's performance and throughput by using hardware parallel processing and data pipelined processing. By simplifying CNN calculations, this innovative method enhances real-time picture recognition.

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