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RTL-Oriented Design and Verification of a Three-Channel Package-Scale Galvanic Isolation Interface for Wide-Bandgap Gate Drivers

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Abstract: *Wide-bandgap semiconductor switches based on silicon carbide (SiC) and gallium nitride (GaN) enable high switching frequency and power density, but they impose stringent requirements on isolated gate-driver communication. This paper presents an RTL-oriented design and verification framework for a three-channel package-scale galvanic isolation interface in which a low-voltage controller domain and a high-voltage driver domain exchange information through RF-coupled microantenna links. The architecture assigns a communication method to each function: direct on-off keying (OOK) for latency-sensitive PWM gate commands, guarded half-duplex communication for diagnostic and configuration exchange, and short/long edge-coded pulses for low-activity reverse power-control signalling. Carrier planning and package placement separate the outer 1.5-GHz links from a 0.5-GHz central diagnostic link, while receiver offset self-calibration, invalid-pulse rejection, mutual exclusion, timeout recovery, programmable channel delay and safe-state forcing improve fault tolerance. The digital architecture was developed and evaluated in Xilinx Vivado 2025.1 for a Spartan-7 xc7s100fgga676-2 target. The supplied verification results show successful elaboration and synthesis with zero errors and zero critical warnings, an elaborated structure containing 11 cells and 36 nets, stable behavioural operation of the diagnostic direction controller, and a preliminary synthesized-netlist on-chip power estimate of 0.089 W. The reported power is static-dominated because representative switching activity was not supplied; therefore, it is not treated as final system power. The work provides a synthesizable verification foundation for subsequent transistor-level RF, electromagnetic, package-parasitic, PVT, CMTI and surge-isolation validation.*

Keywords: galvanic isolation, wide-bandgap devices, SiC, GaN, gate driver, RF microantenna, on-off keying, half-duplex diagnostics, edge coding, RTL verification, Vivado.

I. INTRODUCTION

The rapid adoption of SiC MOSFETs and GaN transistors in traction inverters, renewable-energy converters, high-frequency chargers, industrial motor drives and data-centre power supplies is driven by their high blocking-voltage capability, low switching loss and ability to operate at high junction temperature. These advantages allow converters to switch faster and reduce passive-component size. The same fast voltage transitions, however, increase common-mode disturbance, electromagnetic interference and sensitivity to gate-loop parasitics. The gate driver must therefore reproduce the controller command with small and predictable delay while maintaining electrical separation between low-voltage control electronics and a power stage that can operate at hundreds or thousands of volts [1], [6], [8].

Conventional isolated interfaces employ optocouplers, pulse transformers, capacitive isolators or discrete magnetic/digital isolators. Although mature, these approaches may require several independent devices when gate-

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control, fault reporting, configuration and reverse regulation signals must cross the same barrier. Additional packages and interconnects increase board area and parasitic inductance and may introduce channel-to-channel delay mismatch. Optocouplers also exhibit ageing and temperature dependence, while capacitive barriers must reject displacement current caused by high dV/dt [7]–[10].

Package-scale RF isolation offers an alternative in which two electrically independent dice are co-packaged and communicate by near-field coupling through integrated microantennas [1]–[6]. A high-frequency carrier permits compact resonant coupling structures, and OOK permits simple burst generation and envelope detection. However, a practical intelligent gate driver does not require the same communication behaviour on every signal. The gate command is latency critical, diagnostic traffic is intermittent and bidirectional, and power-control feedback can trade bandwidth for reduced transmitter activity. This motivates a channel-specific architecture rather than a uniform isolator for every function.

The contribution of this work is an RTL-oriented adaptation and verification framework for such a three-channel package-scale isolator. The work focuses on the synthesizable digital-control layer and a configurable behavioural representation of the physical isolation channels. The architecture integrates (i) a direct low-delay driver-control path, (ii) a guarded half-duplex diagnostic path, (iii) an edge-coded reverse power-control path, (iv) receiver offset-calibration control and (v) fault-management logic. The validation is intentionally limited to RTL elaboration, synthesis and behavioural simulation; transistor-level RF performance, electromagnetic antenna coupling and certified isolation ratings remain future sign-off stages.

II. RELATED WORK AND RESEARCH GAP

Integrated galvanic isolation has progressed from discrete optical and magnetic components toward chip-scale and package-scale coupling structures. RF planar coupling can provide reinforced isolation while supporting high common-mode transient immunity, and integrated GaN/CMOS links have demonstrated the feasibility of high-speed data transfer through resonant magnetic structures [2], [3], [6]. Microantenna geometry, mutual coupling, quality factor and the dielectric environment are important because greater lateral separation improves insulation but weakens signal coupling [5].

For wide-bandgap gate drivers, literature identifies propagation delay, delay asymmetry, pulse-width distortion, CMTI and fail-safe behaviour as critical design metrics [1], [8], [9]. Pulse-transformer solutions can combine signal and power transfer [7], while low-jitter isolated drivers target strong transient immunity [8]. Resonant inductive links have also been demonstrated for bidirectional die-to-die communication with high surge isolation [12]. These studies show the benefits of integrated isolation, but the communication requirements of an intelligent gate driver remain heterogeneous.

The research gap addressed here is not the invention of RF microantenna isolation itself, which is established in prior work [1]–[6], but the verification-oriented integration of three tailored communication modes in one synthesizable control architecture. The challenge is to keep the gate-command path simple and fast, allow diagnostics to reverse direction without collision, reduce reverse-channel activity, compensate receiver offset, and ensure deterministic safe states when communication is missing or corrupted.

Isolation approach	Typical strengths	Limitations for multi-function WBG gate drivers
Optocoupler	High electrical separation; mature technology	Ageing, temperature drift, limited bandwidth and delay spread
Pulse transformer / magnetic isolator	High speed and good common-mode immunity	Encoding needed for static states; leakage/parasitic coupling; extra area in discrete form
Capacitive isolator	High integration density and high	Barrier displacement current under high dV/dt;

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	data rate	strong filtering/threshold design required
Package-scale RF microantenna	Co-design of package and communication; short interconnects; frequency-selective reception	Requires EM/package co-design, sensitive RF receiver and careful crosstalk planning
Proposed RTL-oriented three-channel framework	Channel-specific signalling, fault containment, half-duplex diagnostics, edge-coded reverse link	Current validation is digital/behavioural; RF, CMTI, surge and silicon measurements are future work

Table 1. Qualitative comparison of isolation approaches and the scope of the proposed framework.

III. PROPOSED THREE-CHANNEL PACKAGE-SCALE ARCHITECTURE

The proposed system is partitioned into a low-voltage controller chip and a high-voltage driver chip mounted side-by-side on separate conductive frames in a common package. No direct metal connection crosses the isolation barrier. Data is transferred by differential microantennas through narrowband RF coupling. The driver-control and power-control links are positioned toward opposite package edges, while the diagnostic link is centrally located. Nominal carrier planning assigns approximately 1.5 GHz to the two outer links and 0.5 GHz to the central diagnostic link, giving adjacent channels a 1-GHz carrier separation.

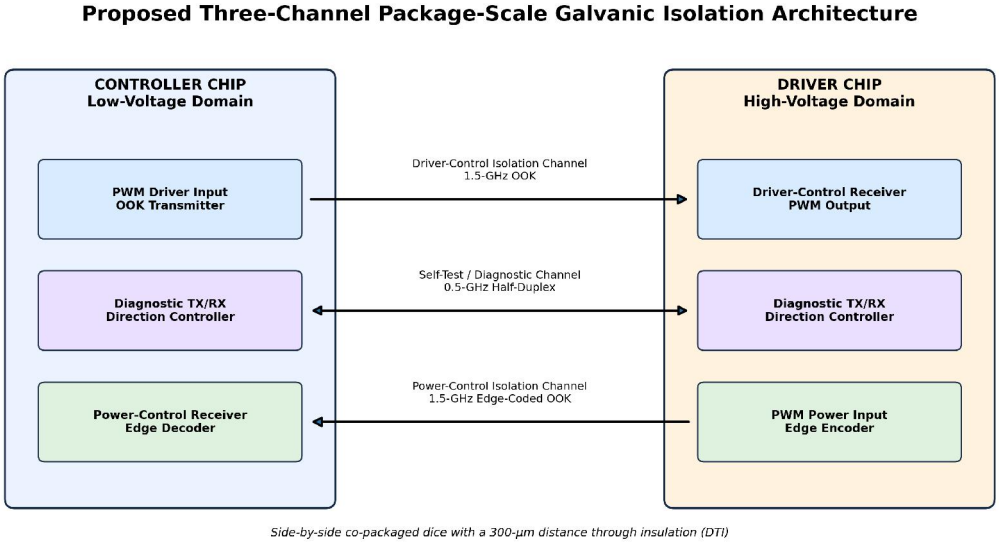

Figure 1. Proposed three-channel package-scale galvanic isolation architecture (adapted from the supplied project design).

3.1 Channel Assignment

Channel	Direction	Signalling method	Primary objective	Protection / control
Driver-control	Controller → Driver	Direct OOK, nominal 1.5 GHz	Minimum latency and low PWM distortion	Missing-carrier timeout; safe off-state
Diagnostic	Bidirectional, half-duplex	OOK, nominal 0.5 GHz	Configuration, self-test and fault reporting	Mutual exclusion, guard interval, timeout recovery

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Power-control	Driver → Controller	Edge-coded OOK, nominal 1.5 GHz	Reduced RF activity for reverse PWM information	Busy protection, width validation, invalid-pulse rejection

Table 2. Functional assignment of the three isolated communication channels.

3.2 Isolation Barrier and RF Coupling

A first-order estimate of dielectric withstand can be obtained from the material dielectric strength E_d and the minimum distance through insulation d_DTI. For the indicative values used in the project, Ed = 50 V/µm and dDTI = 300 µm, the idealized product gives 15 kV. This value is only a design estimate; it is not a certified isolation rating because real qualification depends on electric-field concentration, creepage, package geometry, humidity, ageing, manufacturing tolerance and surge-test conditions.

$$V_{ISO,ideal} = Ed \cdot dDTI \quad (1)$$

Each RF channel employs a resonant antenna/tank. The carrier frequency is approximated by the LC resonance. The antenna shape, metal thickness, spacing, number of turns, quality factor and mutual coupling must subsequently be optimized by electromagnetic extraction.

$$f_{RF} = 1 / (2\pi \sqrt{(L_{ANT} \cdot C_{TANK})}) \quad (2)$$

3.3 OOK Transmitter and Receiver

The transmitter gates a class-D RF oscillator using the digital information signal. When the input is high, an RF burst excites the resonant transmit antenna; when the input is low, the oscillator is disabled. OOK is attractive because it removes a complex line encoder from the latency-sensitive path and allows transmitter activity to follow data activity. In the idealized representation,

$$s_{TX}(t) = A_c\, m(t) \cos(2\pi f_{RF} t + \varphi), \quad m(t) \in \{0,1\} \quad (3)$$

The average transmitter power is approximately proportional to the fraction of time for which the oscillator is enabled. This relationship motivates edge coding for the lower-bandwidth reverse path.

$$P_{TX,avg} \approx D \cdot P_{TX,on} \quad (4)$$

At the receiver, the weak coupled RF voltage is rectified, low-pass filtered, amplified, offset-corrected and passed to a hysteresis comparator. Differential reception and narrowband tuning improve rejection of common-mode and adjacent-channel disturbances. The RTL prototype does not directly implement the GHz oscillator or analog envelope detector; instead, it represents their functional delay, enable, fault and pulse-transfer behaviour with configurable digital models.

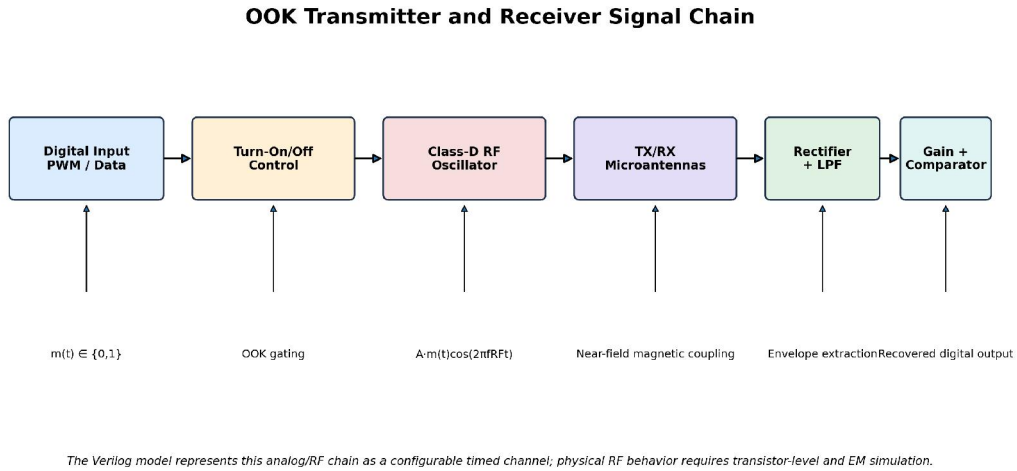

Figure 2. OOK transmitter, package coupling and receiver signal-processing chain used as the mixed-signal reference model.

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IV. CHANNEL LOGIC AND RELIABILITY MECHANISMS

4.1 Low-Latency Driver-Control Path

The driver-control input directly enables the 1.5-GHz OOK transmitter in the physical architecture. Avoiding additional coding minimizes logic-induced latency. The receiver reconstructs the PWM state from the detected carrier envelope. For verification, rising- and falling-edge propagation delays are defined relative to the corresponding input transition, and PWM fidelity is assessed using delay mismatch and pulse-width distortion.

$$t_{PD,r} = t_{OUT,r} - t_{IN,r}, \quad t_{PD,f} = t_{OUT,f} - t_{IN,f} \tag{5}$$

$$t_{PD,avg} = (t_{PD,r} + t_{PD,f})/2, \quad \Delta t_{PD} = |t_{PD,r} - t_{PD,f}| \tag{6}$$

$$PWD = |T_{HIGH,out} - T_{HIGH,in}| \tag{7}$$

The design is intended to be tested across low, medium and high duty ratios because a small rising/falling asymmetry becomes a larger percentage error for narrow pulses. A missing-carrier timeout forces the isolated gate-command output to a predetermined safe state, normally the switch-off state.

4.2 Low-Activity Reverse Power-Control Path

The reverse channel sends events rather than continuously representing the PWM level. A rising input edge generates a short coded pulse T_SHORT, whereas a falling edge generates a longer pulse T_LONG. The receiver measures pulse width and restores the persistent PWM state. A decision threshold is placed midway between the nominal widths.

$$T_{TH} = (T_{SHORT} + T_{LONG})/2 \tag{8}$$

An encoder busy condition prevents overlapping code pulses. The decoder contains pulse-width measurement, end-of-pulse detection and validity checking. Pulses shorter than a minimum valid width are rejected as noise or crosstalk, improving robustness without requiring the RF transmitter to remain continuously active.

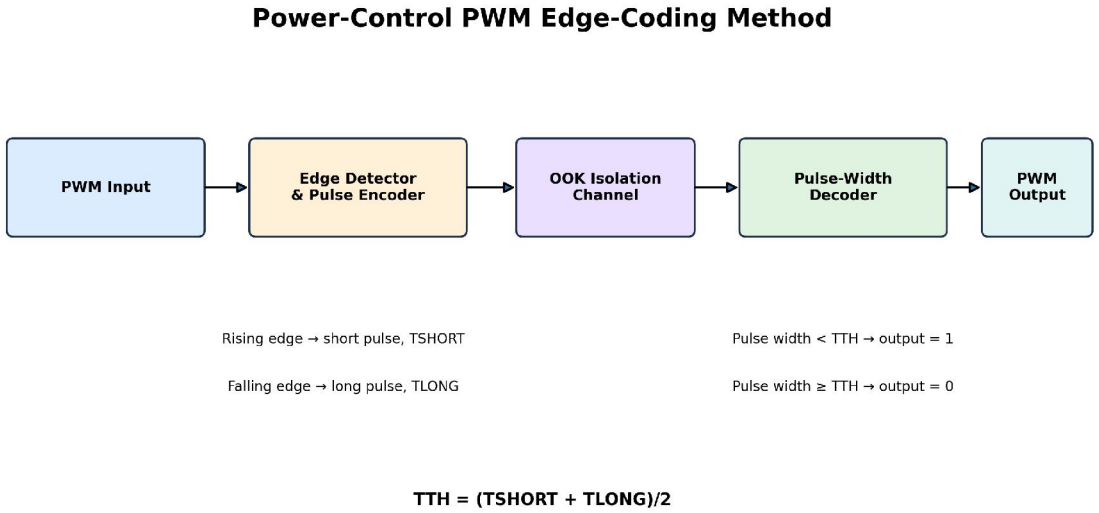

Figure 3. Edge-coding and reconstruction method for the reverse power-control channel.

4.3 Half-Duplex Diagnostic Channel

The central channel shares the coupling structure between transmit and receive functions and therefore operates half duplex. The default state assigns the controller as transmitter and the driver as receiver. After a query or configuration word is sent, both transmitters are disabled for a turnaround guard interval before the driver is allowed to respond. Completion of the response, or expiration of the timeout, returns the channel to the default orientation.

$$T_{XEN,CTRL} \cdot T_{XEN,DRV} = 0 \tag{9}$$

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$$T_{GUARD} \geq T_{DISABLE,max} + T_{SETTLE} + T_{SYNC} + T_{MARGIN} \quad (10)$$

The mutual-exclusion condition prevents transmitter collision and receiver saturation. The guard interval accounts for disable delay, resonant/receiver settling, synchronization uncertainty and design margin. A timeout path prevents the system from remaining indefinitely in the reverse direction when the remote side does not respond.

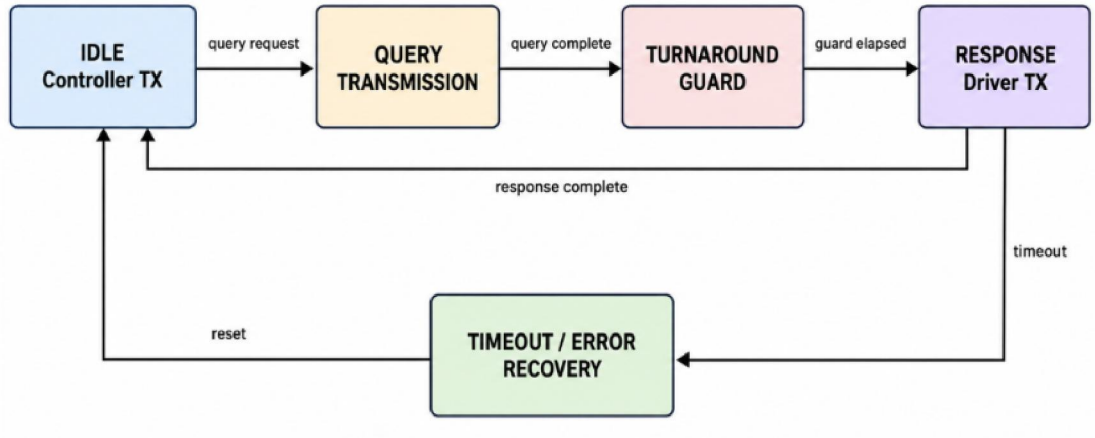

Figure 4. Diagnostic half-duplex direction-control sequence with guard interval and timeout/error recovery.

4.4 Receiver Offset Self-Calibration and Fault Handling

Analog receiver mismatch can shift the effective comparator threshold and reduce sensitivity. The proposed digital calibration controller stores the initial comparator sign and adjusts an N-bit compensation code one step per calibration clock until the comparator output changes sign. Saturation protection terminates the search if an endpoint is reached. The worst-case digital search time is bounded by

$$T_{CAL,max} = (2^N - 1) / f_{CAL} \quad (11)$$

Fault management operates independently on the three channels. The driver-control path detects loss of valid carrier activity, the power-control decoder rejects invalid widths and prevents overlap, and the diagnostic controller recovers from missing responses. The behavioural channel models can inject blockage or spurious pulses so that the testbench can verify safe-state forcing and protocol assertions before analog/RF models are available.

V. RTL IMPLEMENTATION AND VERIFICATION METHOD

The digital prototype is implemented as a modular top-level design containing programmable delay models, an edge encoder, edge decoder, half-duplex data path, diagnostic-control finite-state machine, offset-calibration controller, timeout/error logic and safe-state outputs. The physical RF channel is represented by a configurable behavioural block that can transfer a digital event after a defined delay, block the channel, or inject a short disturbance. This abstraction allows functional verification of control interactions while explicitly avoiding claims about transistor-level RF amplitude, antenna coupling or CMTI.

Verification is organized around self-checking scenarios. The driver-control path is exercised with multiple PWM frequencies and duty cycles; the reverse path is tested for rising/falling code generation and reconstruction; and the diagnostic channel is exercised through query, turnaround, response and timeout states. Assertions are used to check diagnostic transmitter mutual exclusion, prevention of a second edge-coded pulse while the encoder is busy, completion of calibration within the allowed number of cycles, and deterministic recovery after a timeout.

A digital crosstalk margin can be defined by comparing the shortest accepted valid pulse with the longest spurious pulse that the receiver is allowed to accept. A positive margin indicates that the validity filter can separate the modeled disturbance from intentional coded events.

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$$MXT = TVALID,min - TSPURIOUS,max \quad (12)$$

The RTL was evaluated in Xilinx Vivado 2025.1 using a Spartan-7 device identified as xc7s100fgga676-2. The supplied output captures include the synthesized-device view, synthesis status, early power estimate, elaborated schematic and behavioural waveform. These artefacts form the basis of the results reported in the following section.

VI. RESULTS AND DISCUSSION

6.1 Elaboration and Synthesis

Vivado successfully elaborated and synthesized the design with zero errors and zero critical warnings. The supplied synthesis log also reports 23 warnings; because the warning details are not fully visible in the source capture, they should be reviewed before hardware deployment. The elaborated schematic identifies the major proposed modules and reports 11 cells and 36 nets. This confirms structural connectivity of the calibration controller, diagnostic-control logic, half-duplex channel, edge encoder/decoder and programmable delay paths.

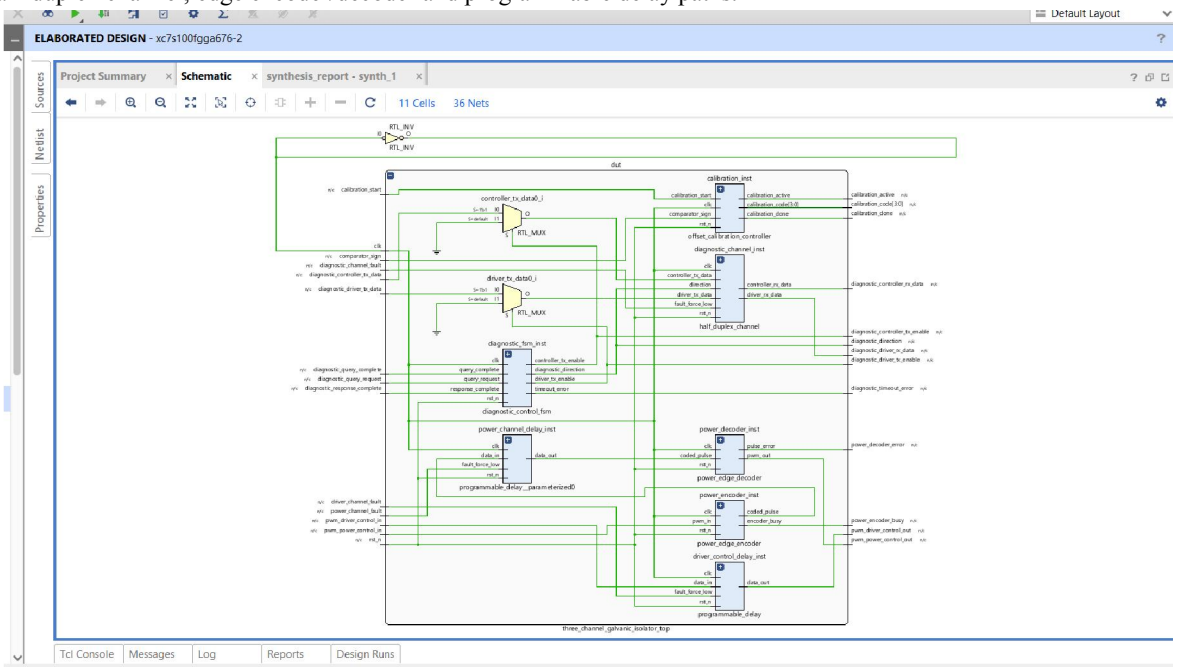

Figure 5. Cropped Vivado elaborated RTL schematic showing the integrated isolation-control modules and top-level interconnection.

6.2 Preliminary Power and Thermal Estimate

The early synthesized-netlist report gives a total on-chip power estimate of 0.089 W. The report attributes the value to device static power and shows dynamic power as 0.000 W. This must not be interpreted as zero switching consumption; instead, it indicates that representative clocks, toggle rates or post-implementation switching activity were not available to the estimator. The source also reports a junction temperature of approximately 25.2 °C for a 25.0 °C ambient condition. A meaningful operating-power result requires implementation-derived capacitances and realistic activity information. In addition, the FPGA report excludes the physical class-D oscillators, antennas, rectifiers, amplifiers and comparators that would dominate parts of a real RF isolation implementation.

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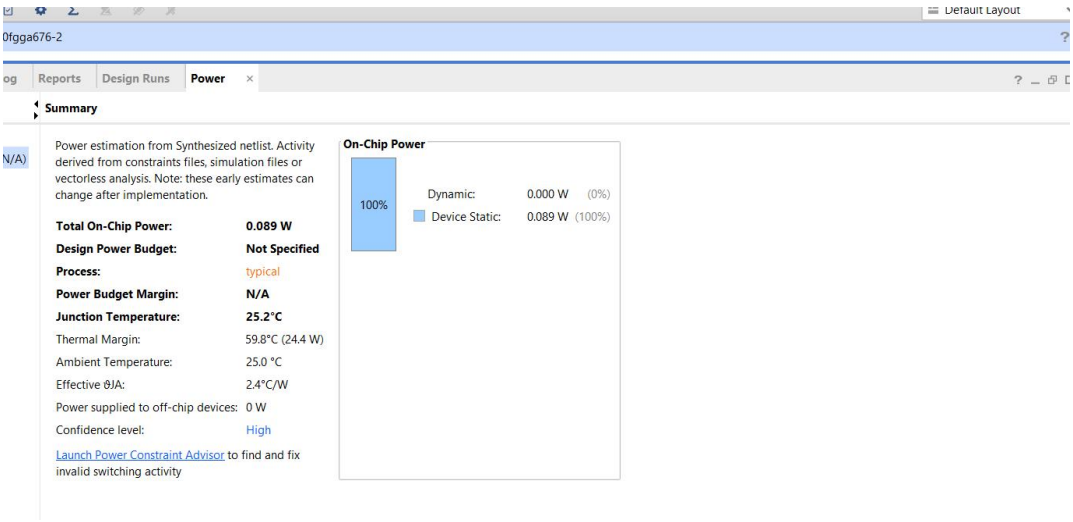

Figure 6. Cropped preliminary Vivado power-estimation view. The 0.089-W value is a static-dominated early estimate, not final mixed-signal system power.

6.3 Behavioural Simulation

The supplied behavioural waveform shows a stable operating interval near 4.889 ms. Reset is deasserted, the driver-control and power-control signals are low at the selected cursor, and the diagnostic request/completion signals are inactive. The controller-side diagnostic transmitter enable is high while the driver-side transmitter enable is low, which is consistent with the defined default direction and verifies transmitter mutual exclusion at the observed instant. The timeout-error indication is low. The displayed calibration code is 4 while calibration_start is inactive, indicating that the controller is retaining a settled code in the captured interval.

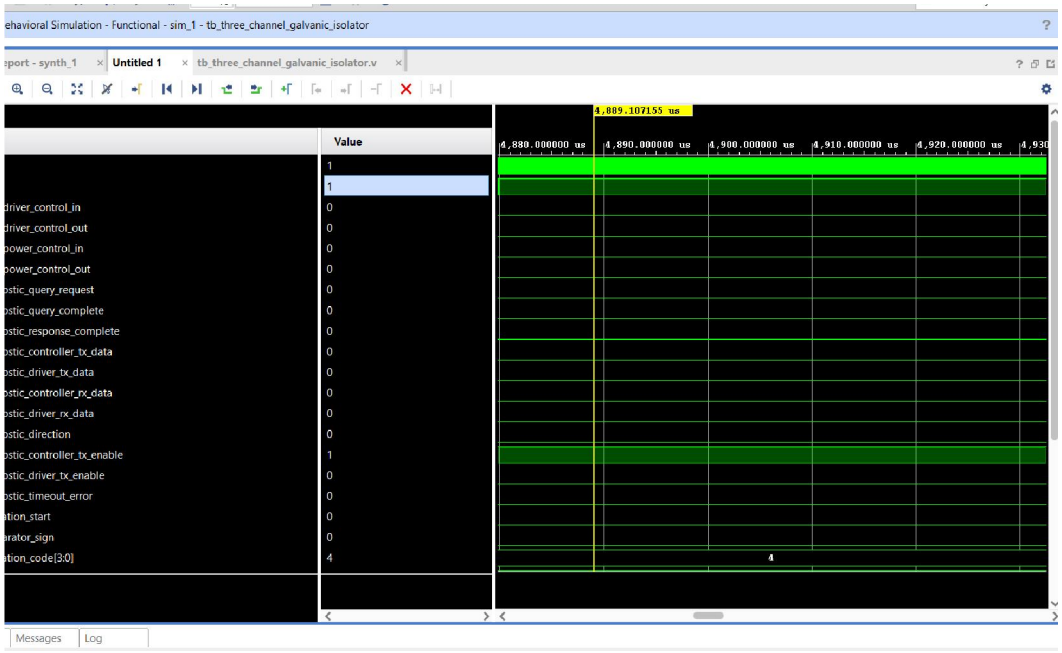

Figure 7. Cropped behavioural simulation waveform showing stable default direction, inactive timeout and retained calibration code in the observed interval.

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The captured waveform is primarily an idle/stable interval, so it does not by itself quantify all active timing metrics. Publication-quality physical performance claims still require zoomed waveforms and markers for rising/falling propagation delay, edge-code widths, diagnostic guard timing, timeout recovery and calibration convergence. The present results therefore establish functional and structural feasibility rather than complete mixed-signal performance sign-off.

6.4 Consolidated Verification Summary

Item	Observed result from supplied outputs	Interpretation / remaining action
Tool / target	Xilinx Vivado 2025.1; Spartan-7 xc7s100fgga676-2	RTL prototype successfully targeted to the selected FPGA family
Synthesis status	0 errors; 0 critical warnings; 23 warnings	RTL accepted; individual warnings should be reviewed before hardware programming
Elaborated structure	11 cells; 36 nets	Major digital modules are integrated at top level
Diagnostic state at capture	Controller TX enable = 1; driver TX enable = 0; timeout = 0	Default direction and mutual exclusion are consistent with the specification
Calibration at capture	Calibration code = 4; calibration_start inactive	A retained code is visible; full convergence interval still needs timing measurement
Preliminary on-chip power	0.089 W; dynamic component shown as 0.000 W	Static-dominated estimate; realistic activity and post-route analysis required
Physical RF/isolation metrics	Not measured in RTL/FPGA results	Need transistor-level, EM, package, PVT, CMTI and surge validation

Table 3. Summary of verified results and the limits of the present validation stage.

6.5 Discussion

The main value of the proposed digital architecture is functional separation. The gate-command path remains free of additional line coding, the diagnostic protocol is isolated from the timing-critical PWM path, and the reverse link reduces RF activity by encoding only transitions. Independent channel enables and state machines also localize failures. From a system-design perspective, this is preferable to treating isolation as one generic serial link whose protocol overhead must satisfy every function.

The design also demonstrates how package-level decisions and digital validation can be co-ordinated. Frequency separation and physical placement are expected to reduce adjacent-channel interference, while digital validity thresholds reject disturbances that survive the analog front end. Nevertheless, the positive impact of these measures on actual crosstalk and CMTI cannot be quantified from the RTL results. Electromagnetic coupling, package capacitance, resonant detuning and common-mode displacement current must be extracted and simulated before a measured robustness claim can be made.

Similarly, the 15-kV ideal dielectric estimate and the 0.089-W FPGA estimate should be interpreted only within their stated models. The former is a simple material-strength product, not a reinforced-isolation certification; the latter excludes RF/analog circuitry and lacks realistic switching activity. Preserving these distinctions strengthens the technical validity of the paper and defines a clear path from digital feasibility to mixed-signal and package-level qualification.

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VII. APPLICATIONS, ADVANTAGES AND LIMITATIONS

Potential applications include electric-vehicle traction inverters, on-board and fast battery chargers, photovoltaic and wind-energy converters, industrial motor drives, uninterruptible power supplies, data-centre and telecommunication supplies, solid-state circuit breakers, railway traction, aerospace power systems, robotics, medical power electronics and high-frequency DC–DC conversion. In these systems, reducing external isolator count and shortening the path between isolation receiver and gate-drive stage can improve integration and reduce board-level parasitics.

Architectural advantages include three function-specific channels, bidirectional diagnostics, low-activity reverse communication, offset-calibration control, timeout-based fail-safe behaviour, transmitter collision prevention and modular RTL verification. These are architecture-level benefits. The current study does not yet provide fabricated-silicon propagation delay, pulse-width distortion, CMTI, surge withstand, microantenna coupling loss, receiver sensitivity, post-layout area or full mixed-signal power. These limitations must be addressed before the design is compared quantitatively with commercial or published isolator ICs.

VIII. CONCLUSION

This paper presented an RTL-oriented design and verification framework for a three-channel package-scale galvanic isolation interface intended for SiC- and GaN-based gate-driver systems. The interface separates a low-voltage controller domain from a high-voltage driver domain and assigns direct OOK, guarded half-duplex OOK and edge-coded OOK to the driver-control, diagnostic and reverse power-control functions, respectively. Frequency planning, receiver offset calibration, timeout recovery, invalid-pulse rejection, programmable channel delay and safe-state forcing are integrated into one modular control architecture.

The supplied Vivado results establish structural and functional feasibility at the digital level. The design elaborated and synthesized without errors or critical warnings, the schematic shows the intended functional modules connected at top level, and the behavioural waveform is consistent with stable default diagnostic direction and no timeout in the observed interval. The preliminary 0.089-W power figure is appropriately treated as an early static-dominated FPGA estimate rather than final system power. The work therefore provides a credible RTL foundation for a subsequent mixed-signal implementation without overstating results that have not yet been measured.

IX. FUTURE WORK

The next stage should replace behavioural channel abstractions with transistor-level class-D oscillators, rectifiers, gain stages, hysteresis comparators and the actual offset-compensation network. Electromagnetic extraction should optimize microantenna geometry, mutual coupling, self-resonance, carrier separation and channel placement while including lead-frame, bond-wire, mould-compound and metal-fill parasitics. Mixed-signal simulation should then measure propagation delay, delay mismatch, pulse-width distortion, receiver sensitivity, coded-pulse margin and energy per transferred event across process, voltage and temperature corners.

Post-layout analysis should be followed by Monte Carlo mismatch evaluation, common-mode transient testing, surge and insulation withstand testing, thermal/humidity ageing and hardware experiments with real SiC/GaN converters. Further digital enhancements can include error-detection coding, adaptive thresholds, automatic carrier tuning, built-in self-test, multi-channel scaling and intelligent fault prediction. A final fabricated prototype would allow the proposed architecture to be benchmarked quantitatively against published isolated gate-driver interfaces.

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