IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

Resource-Efficient VHDL UART Soft Core with 16× Oversampling, Configurable Parity and Double-Buffered Data Paths for Spartan-3E FPGA

Dr. Radha Krishna A.N[1], Vasikarla Renuka[2], Vemula Vinayak[3]
Associate Professor, Dept. of ECE[1]
Assistant Professor, Dept. of ECE[2]
Dept. of ECE[3]
Brilliant Grammar School Educational Society's Group of Institutions - Integrated Campus, Hyderabad, India.
dr.radhakrishnaece@gmail.com, vasikarlarenuka1@gmail.com, vinayakvemula9133@gmail.com

Abstract: *Universal Asynchronous Receiver/Transmitter (UART) remains one of the most widely used low-complexity interfaces for communication between processors, embedded controllers and external peripherals. This paper presents a modular VHDL implementation of a UART soft core intended for FPGA-based embedded systems. The architecture integrates a host-visible register block, baud/clock divider, parity generation and checking, a finite-state-machine-based transmitter, a receiver employing 16× oversampling and center-bit sampling, and buffered data paths for decoupling the processor interface from serial transfer. The transmitter converts an 8-bit parallel word into an asynchronous frame with start, data, optional parity and stop bits, while the receiver validates the start bit, samples the data stream near the center of each bit interval and reconstructs the parallel byte. Functional verification was carried out in ModelSim and synthesis was performed using Xilinx ISE for a Spartan-3E XC3S500E device in the FG320 package with speed grade -4. The reported implementation uses 51 of 4,656 slices, 54 slice registers, 76 four-input LUTs, 22 bonded I/O blocks and one BUFGMUX. The synthesis timing report gives a minimum period of 5.953 ns, corresponding to a maximum frequency of 167.983 MHz, with all timing constraints reported as met. The results demonstrate that the architecture provides correct serial-to-parallel and parallel-to-serial operation with low FPGA resource occupation, making it suitable as an embedded communication peripheral and as a reusable teaching or prototyping IP core.*

Keywords: UART, VHDL, FPGA, Spartan-3E, asynchronous serial communication, 16× oversampling, parity, ModelSim, Xilinx ISE, soft core

I. INTRODUCTION

Asynchronous serial communication continues to be a practical interface in embedded and digital systems because it uses a small number of physical connections, does not require a shared clock line and can be integrated with modest logic resources. A UART performs the conversion between a parallel data representation used by a processor or digital subsystem and the serial bit stream required by a communication link. At the transmitter, the data word is framed by control bits and shifted out one bit at a time. At the receiver, the incoming frame is detected, sampled, checked and reconstructed as a parallel word. The source design considers UART operation as a reusable digital soft core rather than as a fixed external communication device, allowing the serial interface to be embedded directly into a larger FPGA-based system [1]–[4].

The central challenge in an asynchronous link is timing recovery. Because the transmitter and receiver do not share the same bit clock, both endpoints must agree on the baud rate and frame format. The receiver must detect the transition that

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

marks the start bit and then sample each following bit sufficiently close to the center of its bit interval. The supplied design addresses this requirement with a local clock running at sixteen times the data rate. A valid start is accepted only after the input remains low for a substantial portion of the start interval, and the remaining data and parity bits are then sampled at 16-clock intervals. This structure improves tolerance to phase uncertainty at the instant the start edge is detected. The transmitter and receiver also employ holding/buffer registers so that host-side transfers are partially decoupled from the serial shift operation.

The work reported here reformulates the supplied UART project as a publication-oriented FPGA design study. The contribution is a compact, modular VHDL architecture combining a programmable timing block, configurable parity logic, register-based control, a deterministic transmitter state sequence, center-sampled reception and buffered data movement. Functional behavior is demonstrated through ModelSim waveforms, while Xilinx ISE synthesis results provide a concrete measure of logic utilization and achievable clock speed on the Spartan-3E target device. The measured results are taken directly from the supplied project material; no unsupported silicon-area or power claims are introduced.

II. BACKGROUND AND DESIGN REQUIREMENTS

2.1 Asynchronous Frame Structure

A conventional UART line remains at logic high when idle. Transmission begins with a logic-low start bit, followed by a configurable number of data bits transmitted least-significant bit first. An optional parity bit provides simple error detection, and one or more logic-high stop bits terminate the frame. Since no clock is sent with the data, the receiver uses the start edge as a timing reference and advances according to its local baud-rate clock. The design material supports 5-, 6-, 7- or 8-bit character formats in the broader UART description, with even, odd or disabled parity and one, one-and-a-half or two stop-bit options in the referenced UART family. The implemented soft-core datapath shown in the simulation and RTL material is centered on an 8-bit data path.

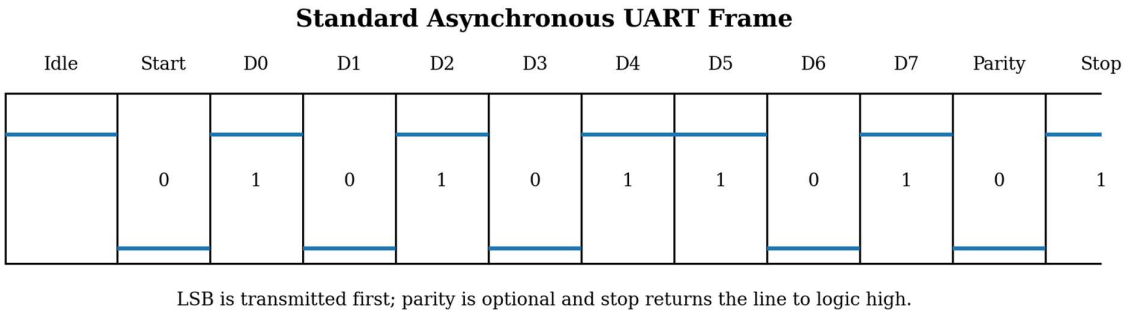


Fig. 1. Generic asynchronous UART frame used as the timing basis of the soft core.

2.2 Design Objectives

The design objectives are: (i) provide a simple 8-bit host interface for transmit and receive data; (ii) generate and check parity under configuration control; (iii) create the timing required for the selected baud rate; (iv) serialize parallel transmit data and reconstruct serial receive data; (v) reduce host timing pressure through buffering; (vi) reject short false-start activity and sample received bits near their centers; and (vii) realize the complete interface with a small logic footprint on an FPGA. These objectives are aligned with the source project's emphasis on reliable high-speed serial communication and a reusable VHDL implementation.

III. PROPOSED UART SOFT-CORE ARCHITECTURE

The architecture is partitioned into a host/register interface, clock divider, parity logic, transmitter and receiver. This modular organization maps naturally to VHDL entities or processes and allows each block to be verified separately before system-level integration. The register block carries transmit data, receive data, configuration information and the clock-division value. The timing block derives the internal clock used by the serial state machines. The transmitter consumes a

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

parallel byte and produces the SOUT bit stream, whereas the receiver monitors SIN and produces a recovered parallel byte together with status information.

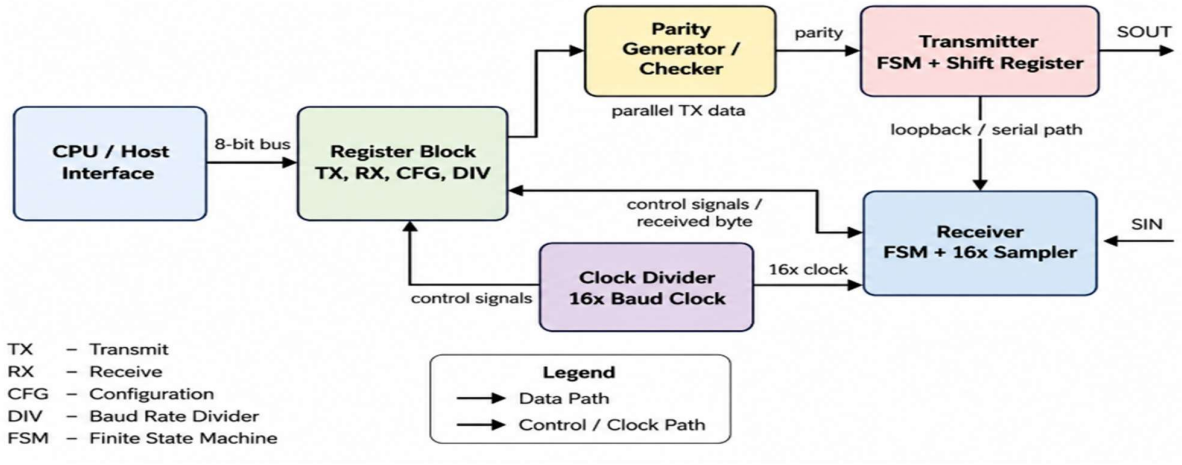


Fig. 2. Modular architecture of the VHDL UART soft core.

3.1 Register Interface and Control

The source architecture describes four primary registers: transmit data, receive data, configuration and clock division. In the shown register map, transmit data is associated with address 0x00, receive data with 0x01, configuration with 0x10 and the clock-division value with 0x11. Configuration bits enable the transmitter and receiver, select parity behavior and expose receive-complete information. This compact address map is appropriate for memory-mapped attachment to a processor or to a simple bus bridge.

Compact Register Interface Used by the UART Core

Address	Register	Access	Function
0x00	Transmit Data	Write	8-bit data
0x01	Receive Data	Read	8-bit data
0x10	Configuration	R/W	TX enable, RX enable, parity enable, odd/even select, RX done
0x11	Clock Division	R/W	Baud / sampling-clock divisor

Fig. 3. Register organization reconstructed from the supplied UART design.

3.2 Baud-Rate and Sampling-Clock Generation

The clock divider establishes the serial timing reference. The source material states that the internal UART clock is operated at sixteen times the desired baud rate. Therefore, when a system clock f_SYS is divided by an integer N to generate the 16× sampling clock, the relationship can be written as

$$B = \frac{f_{SYS}}{(16N)}$$

where B is the desired baud rate. This formulation separates the fast FPGA system clock from the slower serial timing domain and allows multiple common baud rates to be produced by changing only the divisor. The waveform supplied

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

with the project shows the counter progressing while the divided baud clock toggles, confirming the expected clock-generation behavior.

3.3 Transmitter Operation

The transmitter uses a holding/buffer register and a shift register. When the transmitter buffer is available, the host can write the next data byte without directly controlling individual serial bit times. Once transmission is enabled, the transmitter forces the line low for the start bit, then shifts the eight data bits from least significant to most significant. If parity is enabled, the computed parity bit follows the data field. A logic-high stop bit completes the frame, after which the state machine returns to the idle state. The source description notes that double buffering permits a second word to be placed in the holding register while the current word is being shifted, supporting back-to-back frames and improving throughput.

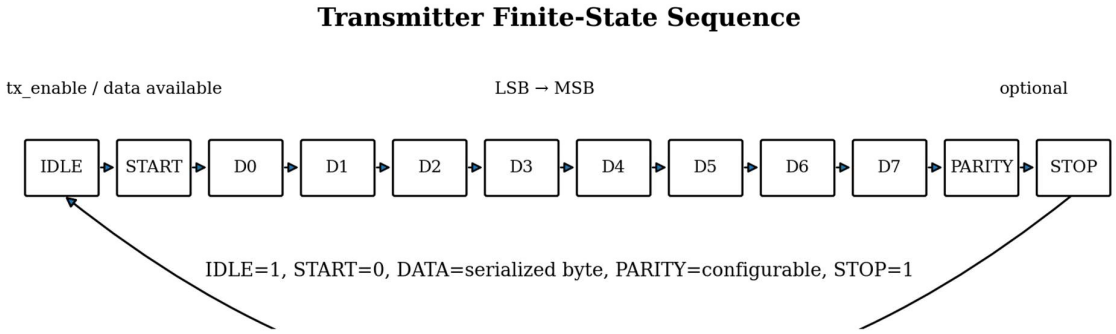


Fig. 4. Transmitter state sequence for an 8-bit UART frame.

3.4 Receiver Operation and 16× Oversampling

The receiver detects a high-to-low transition on SIN as a candidate start bit. To reduce the probability that a short noise pulse is accepted as a real frame, the design requires the start condition to remain low for at least eight cycles of the 16× receive clock before it is treated as valid. After this validation, the data and parity positions are sampled at intervals of sixteen local clock cycles so that the sample point lies close to the center of each bit cell. The source material reports that the center of the start bit is approximately at count 7.5; with a symmetric 16× clock, the phase uncertainty is about ±1/2 clock, equivalent to 1/32 of a bit interval. This center-sampling strategy provides substantial timing margin without requiring a transmitted clock.

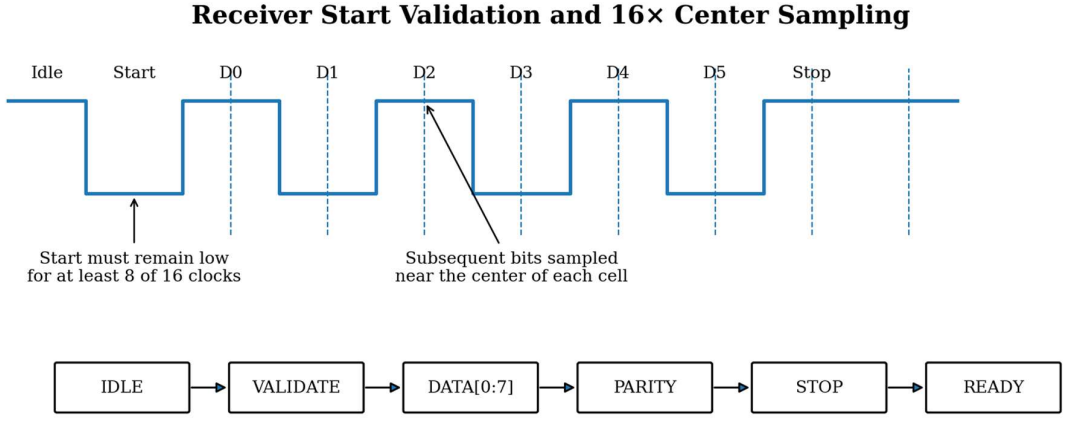


Fig. 5. Receiver start validation, center sampling and simplified receive sequence.

DOI: 10.48175/IJARSCT-38271

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

The receiver shift register captures data from LSB to MSB. If parity is enabled, the received parity is compared with the parity recomputed from the data. A valid stop interval completes the frame, after which the reconstructed byte is transferred into the receiver buffer and the data-ready status is asserted. The source conclusion also notes that overrun-error signaling was not implemented in the VHDL source, which is an important limitation and a clear opportunity for future refinement.

3.5 Parity Generation and Error Checking

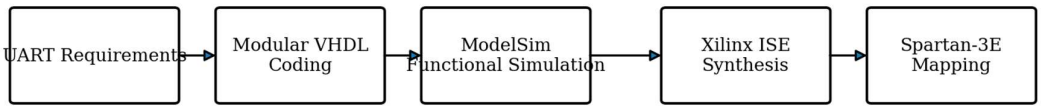
Parity is generated by evaluating the number of logic-one bits in the data word. For even parity, the parity bit is chosen so that the total number of ones in the data plus parity field is even. For odd parity, the total is forced to an odd value. The source project uses even parity as the default and enables odd parity through the configuration register. On reception, a mismatch between the expected and received parity value is reported as a parity error. Parity is intentionally a lightweight error-detection mechanism; it detects many single-bit disturbances but is not a substitute for a stronger end-to-end checksum or cyclic-redundancy check when a higher level of integrity is required.

3.6 Buffering and Data-Flow Decoupling

The source project describes double-buffered transmit and receive paths and also includes a FIFO simulation waveform. In the receive direction, the receiver shift register accumulates the serial frame while the receiver buffer preserves the previously completed byte for host access. In the transmit direction, the transmit buffer can accept the next byte while the shift register serializes the current one. This decoupling reduces the requirement for the host processor to respond at exact bit boundaries. The FIFO waveform further demonstrates write, read, full/empty control behavior in the project's verification environment, illustrating how a deeper queue can be incorporated when burst tolerance beyond double buffering is required.

IV. VHDL IMPLEMENTATION AND VERIFICATION METHODOLOGY

The design flow used in the supplied project follows the standard RTL path: architectural partitioning, VHDL coding, behavioral simulation, synthesis, mapping and timing analysis. The design was simulated with ModelSim and synthesized using Xilinx ISE. The final target reported in the synthesis section is the Spartan-3E XC3S500E device in the FG320 package with speed grade -4. The project status indicates successful routing and that all timing constraints were met, while the synthesis flow also produced a programming file.



Clock-divider, buffer, transmitter and receiver waveforms are verified before synthesis; post-synthesis reports are then used to assess logic cost and timing.

Fig. 6. RTL design, simulation and synthesis flow used for the UART implementation.

Item	Configuration / Evidence
HDL	VHDL
Functional simulator	ModelSim 6.4b (as reported in the results chapter)
Synthesis environment	Xilinx ISE / XST
FPGA family	Spartan-3E
Target device	XC3S500E
Package	FG320
Speed grade	-4
Receive timing	16× local clock with center sampling

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 6, Issue 1, September 2026 Impact Factor: 8.2

Data path	8-bit transmit and receive datapaths
Buffering	Double-buffered TX/RX; FIFO activity also simulated

Verification was performed at block and top level. The clock-divider test confirms generation of the slower timing reference from the input clock. Buffer/FIFO testing exercises write, read, full and empty behavior. Transmitter testing verifies start generation, bit sequencing and serial output progression. Receiver testing verifies serial input capture, receive-clock operation and parallel-word reconstruction. Because the supplied source does not provide a formal assertion set or coverage report, the paper treats the presented simulation waveforms and synthesis reports as the primary evidence of correctness.

V. RESULTS AND DISCUSSION

5.1 Functional Simulation

The ModelSim results demonstrate the intended behavior of the principal submodules. In the clock-divider waveform, the internal counter advances while the derived baud clock toggles at the divided rate. The buffer/FIFO waveform shows data being written and later read while the status signals track occupancy. In the receiver waveform, the serial input changes in time with the local receive clock and the parallel output eventually resolves to the received byte. In the transmitter waveform, the 8-bit input value is converted into a serial output sequence under baud-clock control. Together, these tests provide functional evidence for the data-path and timing blocks before synthesis.

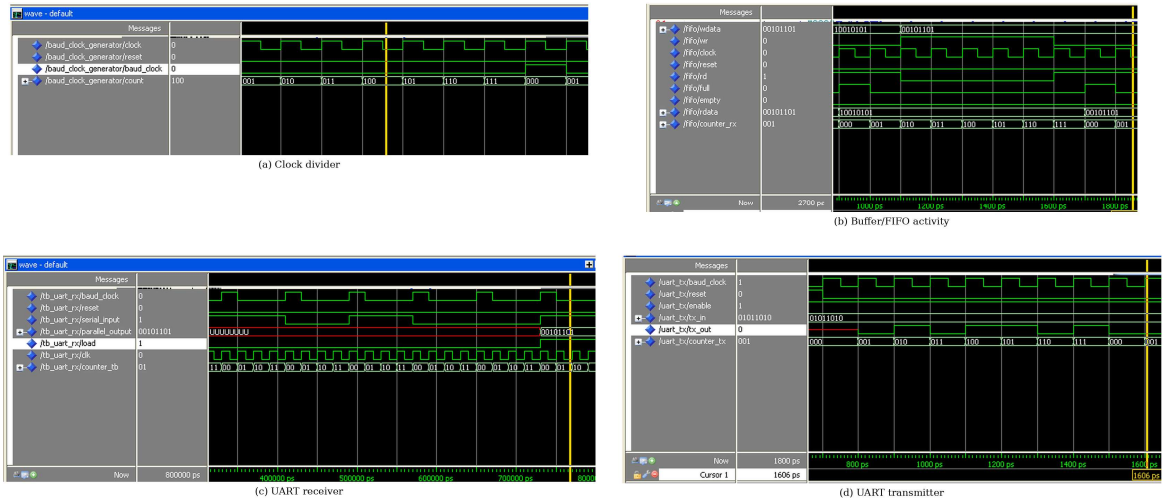


Fig. 7. Functional ModelSim results supplied with the UART project: clock divider, buffering, receiver and transmitter.

5.2 FPGA Resource Utilization

After functional simulation, the VHDL design was synthesized for the XC3S500E-4FG320 target. The project summary reports no errors, successful complete routing and all timing constraints met. Twenty-seven warnings are reported at project level; the supplied material does not list their detailed causes, so they should be reviewed before treating the implementation as production-ready. The resource report indicates very low use of the available Spartan-3E logic fabric.

FPGA Resource	Used	Available	Reported Utilization
Slice registers	54	9312	1%
- flip-flops	45	—	—
- latches	9	—	—
4-input LUTs	76	9312	1%
Occupied slices	51	4656	1%
Bonded I/Os	22	232	9%

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 6, Issue 1, September 2026 Impact Factor: 8.2

BUFGMUXs	1	24	4%

The logic cost is modest: only 51 occupied slices and 76 LUTs are required, while 54 slice registers implement the sequential state and data storage. This leaves substantial headroom for integrating the UART alongside application logic in the same device. The higher percentage for bonded I/O relative to logic is expected for a communication peripheral because external pins are consumed even when the internal datapath is small.

UART Project Status (04/24/2010 - 11:13:18)

Project File:	UART.ise	**Current State:**	Programming File Generated
Module Name:	uart	**• Errors:**	No Errors
Target Device:	xc3s500e-4fg320	**• Warnings:**	27 Warnings
Product Version:	ISE 10.1 - Foundation Simulator	**• Routing Results:**	All Signals Completely Routed
Design Goal:	Balanced	**• Timing Constraints:**	All Constraints Met
Design Strategy:	Xilinx Default (unlocked)	**• Final Timing Score:**	0 (Timing Report)

UART Partition Summary [-]

No partition information was found.

Device Utilization Summary [-]

Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	54	9,312	1%	
Number used as Flip Flops	45			
Number used as Latches	9			
Number of 4 input LUTs	76	9,312	1%	
Logic Distribution				
Number of occupied Slices	51	4,656	1%	
Number of Slices containing only related logic	51	51	100%	
Number of Slices containing unrelated logic	0	51	0%	
Total Number of 4 input LUTs	76	9,312	1%	
Number of bonded IOBs	22	232	9%	
Number of BUFGMUXs	1	24	4%	

Performance Summary [-]

Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports [-]

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat Apr 24 11:08:43 2010	0	18 Warnings	13 Infos
Translation Report	Current	Sat Apr 24 11:11:49 2010	0	0	0
Map Report	Current	Sat Apr 24 11:12:02 2010	0	9 Warnings	2 Infos
Place and Route Report	Current	Sat Apr 24 11:12:35 2010	0	0	2 Infos
Static Timing Report	Current	Sat Apr 24 11:12:45 2010	0	0	3 Infos
Bitgen Report	Current	Sat Apr 24 11:13:14 2010	0	9 Warnings	0

Date Generated: 04/24/2010 - 11:13:18

Fig. 8. Xilinx ISE project-status and device-utilization report from the supplied implementation.

5.3 Timing Performance

Timing Metric	Reported Value
Speed grade	-4
Minimum period	5.953 ns
Maximum frequency	167.983 MHz
Minimum input arrival before clock	4.537 ns

DOI: 10.48175/IJARSCT-38271

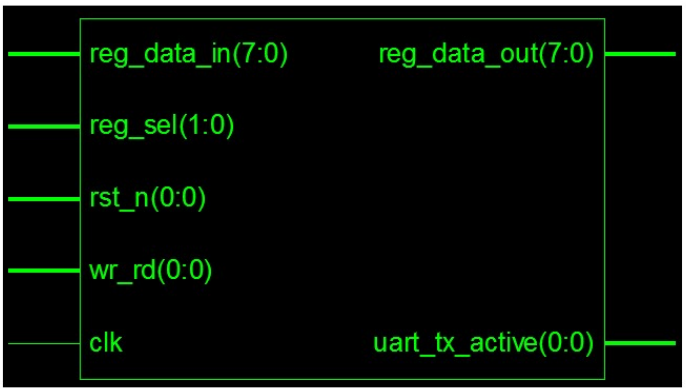
IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

Maximum output required after clock	5.919 ns
Maximum combinational path delay	No path found in the reported summary

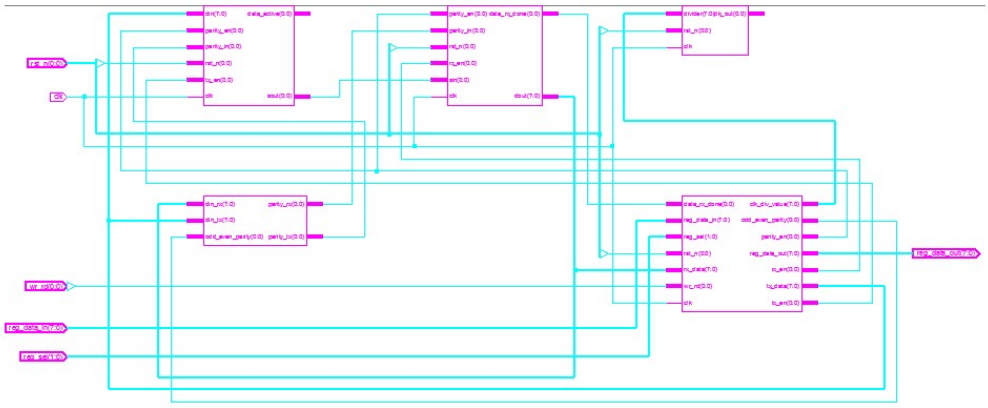
The synthesis timing summary reports a minimum clock period of 5.953 ns, corresponding to a maximum frequency of 167.983 MHz. This is the internal design timing limit reported by synthesis; it should not be confused with the serial baud rate, which is lower because the UART derives a 16× sampling clock and then a one-bit-per-baud data stream. The timing result nevertheless indicates that the RTL control and datapath can operate comfortably above typical UART sampling-clock requirements on the selected Spartan-3E device.

5.4 RTL Structure and Integration

The synthesized RTL view confirms that the design is composed of distinct functional blocks rather than a monolithic process. The supplied schematic identifies the top-level host-facing inputs and outputs, while the expanded view shows the internal register, clock, parity, transmitter and receiver modules. This structure is advantageous for reuse because an integrator can replace or extend a block—such as the buffer depth or bus interface—without redesigning the complete serial engine.



(a) Synthesized top-level interface



(b) Internal module connectivity

Fig. 9. Synthesized top-level UART interface and internal module connectivity from the supplied project.

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

5.5 Requirement-to-Evidence Assessment

Requirement	Implementation Mechanism	Evidence in Supplied Results
Parallel-to-serial conversion	TX FSM + shift register	Transmitter waveform and RTL schematic
Serial-to-parallel conversion	RX FSM + receive shift register	Receiver waveform and parallel-output reconstruction
Baud timing	Programmable clock divider	Clock-divider waveform
Noise-resistant start detection	8-of-16 start validation	Receiver methodology in source design
Parity support	Configurable parity generator/checker	Architecture and configuration description
Host decoupling	Double buffers / FIFO test	Buffer/FIFO waveform and conclusion
Low FPGA cost	Small LUT/register/slice count	Xilinx device-utilization report
High internal timing margin	5.953 ns minimum period	Xilinx timing summary

The evaluation shows that the strongest evidence is available for functional transmission/reception, timing generation and synthesis cost. The main limitations of the evidence are the absence of post-layout waveform measurements, hardware oscilloscope captures, a detailed warning audit, formal verification coverage, and measured power. Therefore, the reported results support the RTL and FPGA-synthesis claims but should not be extended to unmeasured electrical or power-performance claims.

VI. APPLICATIONS, ADVANTAGES AND LIMITATIONS

The core is appropriate for embedded processor peripherals, FPGA-based instrumentation, educational digital-design platforms, industrial control links, debug interfaces, sensor gateways and prototype systems that require a straightforward asynchronous serial port. Its modular VHDL description allows the interface to be instantiated as reusable IP and adapted to a larger logic design. Low LUT and slice use are particularly useful when the UART is only one peripheral among several functions on a resource-constrained device.

Aspect	Implication
Modular VHDL organization	Facilitates reuse, debugging and block-level verification.
16× receiver clock	Provides deterministic center sampling without a shared serial clock.
Double-buffered data paths	Reduces processor response pressure and supports continuous transfers.
Configurable parity	Adds lightweight transmission-error detection.
Low slice/LUT occupancy	Leaves most FPGA resources available for application logic.
Source limitation: overrun error not implemented	Host or future FIFO logic must prevent receive-buffer overwrite.
No measured power data	Power efficiency cannot be quantified from the supplied results.
Legacy Spartan-3E toolchain	Modern FPGA retargeting requires renewed synthesis and timing validation.

VII. CONCLUSION

A complete VHDL UART soft core has been organized and evaluated from the supplied project material. The design combines an 8-bit register interface, programmable timing, parity processing, a serial transmitter, a 16× oversampling receiver and buffered data movement. Functional simulation demonstrates clock division, buffer activity, serial transmission and serial reception. Xilinx ISE synthesis for the Spartan-3E XC3S500E-4FG320 reports 51 occupied slices, 54 slice registers, 76 four-input LUTs, 22 bonded I/Os and one BUFGMUX. The timing summary reports a 5.953 ns minimum period and 167.983 MHz maximum frequency, with routing complete and timing constraints met. These results indicate that the design is a compact FPGA communication peripheral with significant remaining logic capacity for

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

integration into larger embedded systems. The interpretation is deliberately limited to the supplied RTL simulation and synthesis evidence; no unmeasured power, silicon or analog link performance is claimed.

VIII. FUTURE SCOPE

Future development can strengthen both the implementation and its validation. The receive path can be extended with explicit overrun-error handling and a parameterized multi-byte FIFO. Interrupt generation can be added for receive-ready, transmit-empty and error events, or alternatively a lightweight bus protocol such as AXI4-Lite, Wishbone or APB can be introduced for SoC integration. A fractional or numerically controlled baud-rate generator would improve baud accuracy when the system clock is not an integer multiple of 16 times the target rate. The receiver can be enhanced with majority voting across multiple oversamples rather than a single center sample. Additional verification should include randomized frame testing, parity and framing faults, baud mismatch, back-to-back traffic, buffer overflow, reset during transfer, assertions and functional coverage. Finally, retargeting the design to a current FPGA family and collecting post-place-and-route timing, resource, power and on-board serial-loopback measurements would provide a stronger basis for modern comparative evaluation.

REFERENCES

1. M. Y. I. Idris, M. Yaacob, and Z. Razak, “A VHDL Implementation of UART Design with BIST Capability,” reference cited in the supplied project document.
2. Z. Navabi, VHDL: Analysis and Modeling of Digital Systems. New York, NY, USA: McGraw-Hill, 1991.
3. MD. Javeed and F. Jabeen, “FPGA Implementation for the Linking of Cell Tracks Using New Structure Algorithm,” *International Journal of Engineering and Advanced Technology (IJEAT)*, vol. 9, no. 1, pp. 6773–6778, Oct. 2019.
4. C. H. Roth, Digital System Design Using VHDL. Boston, MA, USA: PWS Publishing, 1998.
5. M. S. Michael, “A Comparison of the INS8250, NS16450 and NS16550AF Series of UARTs,” National Semiconductor Application Note 493, Apr. 1989.
6. National Semiconductor, “PC16550D Universal Asynchronous Receiver/Transmitter with FIFOs,” application documentation, Jun. 1995.
7. M. S. Harvey, Generic UART Manual, Silicon Valley, Dec. 1999.
8. MD. Javeed and C. F. Jabeen, “Linking of Cell Tracks Using Segmentation,” *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*, vol. 9, no. 1, pp. 3020–3026, Nov. 2019. Google Scholar
9. S. Wang, “Generation of low power dissipation and high fault coverage patterns for scan-based BIST,” in Proc. International Test Conference, 2002, pp. 834–843.
10. A P. Stroele and H. J. Wunderlich, “Hardware-optimal test register insertion,” IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 17, no. 6, pp. 531–539, Jun. 1998.
11. M. Javeed, T. Srujana, and M. Senthil Kumar, “Design of a Clock Distribution Network Using Low Power Prescaler and Fused P & S Counters,” International Journal of Innovation in Engineering Research & Management (IJIERM), vol. 6, Special Issue 6, pp. 1–8, Oct. 2019. Google Scholar
12. O. A. Petlin and S. B. Furber, “Built-in-self-testing of micropipelines,” in Proc. Advanced Research in Asynchronous Circuits and Systems, IEEE, 1997, pp. 22–29.
13. J. Turino, “RTL DFT Rule Checking—The Circuit Designer’s Secret Weapon,” Integrated System Design Magazine, 2000.
14. S. A. Pasha, M. Javeed, and B. Laxman, “Detection Disease and Automatic Medication Composition on Plant Leafs Using Structure Algorithm,” *International Journal of Innovation in Engineering Research & Management (IJIERM)*, vol. 6, Special Issue 6, pp. 1–8, Oct. 2019. Google Scholar