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Area–Delay–Power Efficient FPGA Architecture for Real-Time Impulse Noise Removal Using Decision-Based Multiplexers and Adaptive Neighborhood Median Filtering

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Abstract: *Real-time image denoising requires a filtering architecture that simultaneously preserves image structure and satisfies strict hardware constraints on area, latency, and power. This paper presents an FPGA-oriented real-time impulse noise removal (RTINR) architecture built around a decision-based multiplexer and an adaptive-neighborhood median-selection network. The decision-based multiplexer compares two 8-bit pixel values and directly produces high and low outputs through comparator-controlled 2:1 multiplexers. These primitive cells are organized into multi-level adaptive-neighborhood blocks so that the median of a 3×3 processing window can be obtained without a conventional full sorting network. The architecture was modeled in Verilog HDL, simulated and synthesized using Xilinx ISE, while image-level denoising quality was assessed in MATLAB R2020a. Reported synthesis results show 437 slice LUTs, a total path delay of 20.375 ns, and on-chip power consumption of 32.83 mW. For the evaluated image case, the method achieves 54.53 dB PSNR and 0.992 SSIM. Relative to the compared standard, decision, and adaptive median filters, the RTINR architecture reduces LUT count, delay, and power while improving image-quality measures. The results indicate that comparator/multiplexer-centric median selection is a practical design strategy for low-resource, real-time FPGA image preprocessing in embedded vision systems.*

Keywords: FPGA, impulse noise, median filter, decision-based multiplexer, adaptive neighborhood, image denoising, VLSI, real-time image processing

I. INTRODUCTION

Noise introduced during image acquisition, sensor readout, storage, or communication can seriously degrade the reliability of subsequent image-processing operations. Impulse noise is especially disruptive because it replaces isolated pixels with extreme or arbitrary intensity values. In an 8-bit gray-scale image, fixed-valued impulse noise commonly appears as salt-and-pepper samples at or near 0 and 255. When such corrupted images are used by surveillance, medical-imaging, machine-vision, or robotics systems, the denoising stage must suppress corrupted pixels without destroying edges and fine structures.

Median filtering is one of the most widely used nonlinear techniques for impulse-noise suppression because it is inherently more resistant to outliers than linear averaging filters. The major implementation challenge is that the median of a local window normally requires repeated comparisons and data ordering. A direct software realization is flexible, but real-time embedded applications often require deterministic throughput and lower latency than a processor-only

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solution can provide. Field-programmable gate arrays (FPGAs) are therefore attractive because the comparison, selection, and neighborhood operations can be parallelized and mapped directly to logic resources [1], [12], [14].

However, a hardware median filter is not automatically efficient. Conventional comparator trees and sorting networks may consume substantial LUT resources, incur long routing paths, and increase dynamic power. Approximate and low-cost sorting approaches have been investigated to reduce these costs [13], [20], [24], [25], while hybrid and adaptive median strategies have been developed to improve robustness under mixed or high-density noise [4]–[9], [17]. The design problem is therefore a joint hardware–algorithm optimization problem: the filter must be accurate enough to restore image detail while remaining compact and fast enough for real-time deployment.

This work develops an RTINR architecture in which a decision-based multiplexer is used as the fundamental compare-and-select element. Instead of constructing a large generic sorter, the design organizes low-cost high/low selectors into adaptive-neighborhood modules and then into a 3×3 median-selection network. The architecture targets reduction of LUT usage, path delay, and power while retaining high denoising quality.

The main contributions of the paper are:

A compact decision-based multiplexer that maps two-pixel comparison directly to high and low data outputs.

An adaptive-neighborhood three-input block that produces high, median, and low values from local pixel groups using cascaded decision modules.

A multi-level 3×3 RTINR median network that avoids a full nine-element sort and is suitable for RTL implementation and FPGA synthesis.

A joint hardware and image-quality evaluation using LUT count, timing, power, PSNR, and SSIM, together with comparison against SMF, DMF, and AMF baselines reported in the supplied study.

II. RELATED WORK

Research on hardware-efficient image filtering has followed three closely related directions: high-throughput median architectures, adaptive or hybrid denoising algorithms, and low-cost comparison/sorting circuits. Goel et al. presented a high-throughput FPGA implementation of a two-dimensional median filter [1], [12]. Srinu et al. used compare-and-exchange elements to obtain a hardware-oriented median filter with emphasis on processing speed [14]. These works demonstrate the value of mapping rank-order operations directly to hardware, but the number and arrangement of comparison stages remain critical determinants of area and delay.

Several studies have combined median operations with adaptive or hybrid filtering. Sambamurthy and Kamaraju investigated power-optimized hybrid sorting-based median filtering [4], while Arnal and Súcar developed a fuzzy hybrid approach for mixed-noise reduction [5]. Other studies applied hybrid median concepts to rain-streak elimination, medical images, ultrasound, and review frameworks [6]–[9]. Sindhana Devi and Soranamageswari combined impulse-noise removal with neuro-fuzzy processing [17]. Such methods can improve restoration quality, but complex decision rules may be costly when translated directly to hardware.

Low-cost arithmetic and ordering circuits provide another route to efficient filtering. Approximate arithmetic has been proposed for DSP and image-processing workloads [13], [16], [20]. Chen et al. reported a low-cost two-dimensional median filter [21], and Lin et al. proposed a comparison-free one-dimensional median filter [24]. Najafi et al. introduced unary-processing-based sorting networks for area- and power-efficient hardware [25]. These methods show that the structure of the comparison network has a strong influence on the final hardware cost.

FPGA image-processing research has also addressed haze removal, depth estimation, feature extraction, demosaicing, FIR filtering, polarization denoising, and bilateral filtering [2], [3], [10], [11], [15], [18], [19], [22], [23]. Collectively, these studies reinforce a general requirement: real-time vision pipelines benefit from algorithmic forms that are naturally compatible with parallel logic and predictable memory access. The present work applies this principle specifically to impulse-noise removal by making the decision-based multiplexer the basic hardware primitive.

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III. PROBLEM FORMULATION AND DESIGN OBJECTIVES

Let the input be an 8-bit gray-scale image. For each processing location, the filter considers a 3×3 neighborhood containing nine pixel values P0 through P8. The desired output is a representative local value that rejects impulse outliers while preserving the local edge structure. A conventional median implementation would order all nine samples and select the fifth-ranked value. In hardware, this can require a large number of compare-and-swap operations and may introduce unnecessary switching activity.

The proposed design adopts a structured median-selection strategy. Groups of three pixels are first reduced to local high, median, and low values. Selected local extrema and medians are then compared in subsequent stages until a single median output is produced. The design objectives are: (i) deterministic real-time operation; (ii) reduced LUT count; (iii) reduced critical-path delay; (iv) low on-chip power; and (v) preservation of denoised image quality as reflected by PSNR and SSIM.

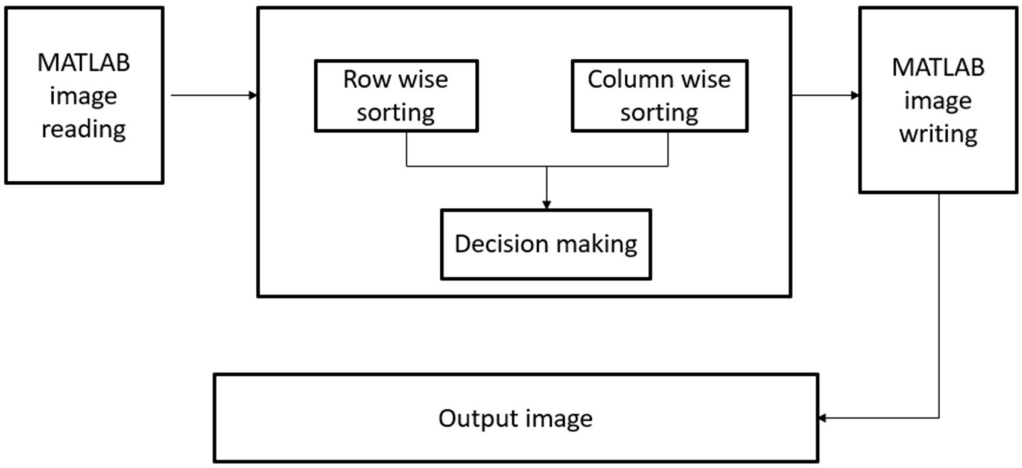

Fig. 1. System-level workflow used in the supplied RTINR study: image input, row/column neighborhood processing, decision logic, and restored image output.

IV. PROPOSED RTINR ARCHITECTURE

4.1 Decision-Based Multiplexer

The decision-based multiplexer is the fundamental two-input processing element. It receives pixel values A and B and generates two outputs: High (H) and Low (L). A comparison condition A < B produces the select signal. The same select signal is applied to two 2:1 multiplexers whose data inputs are arranged in complementary order. Consequently, one multiplexer forwards the larger sample while the other forwards the smaller sample.

This structure is hardware-efficient because the comparison result is reused directly for data routing. The design does not require a separate arithmetic sorting stage followed by a second selection stage; comparison and selection are combined in one compact unit. For 8-bit pixels, the operation is replicated at word level while the select path determines which complete byte is routed to each output.

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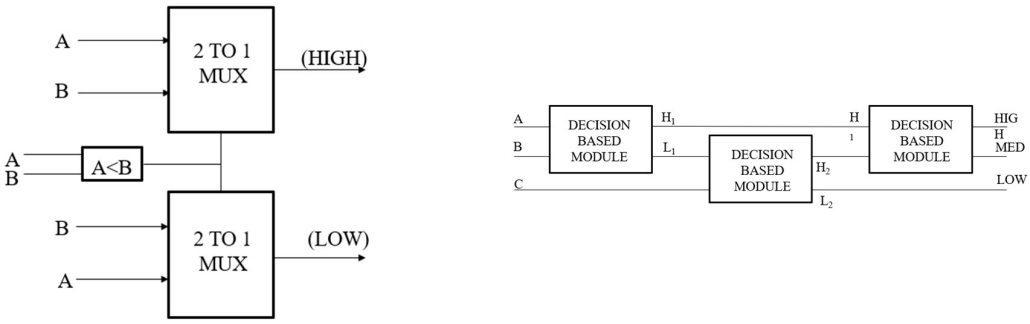

Fig. 2. Core submodules: (a) decision-based two-input high/low selector and (b) adaptive-neighborhood three-input high/median/low selector.

4.2 Adaptive-Neighborhood Three-Input Module

A three-input adaptive-neighborhood module is created by cascading decision-based modules. The first stage compares two values and produces intermediate high and low outputs. A subsequent decision block compares the remaining input against these intermediate values so that the final outputs are organized as High, Median, and Low. This module therefore behaves as a compact three-cell sorter and becomes the basic building block of the 3×3 median network.

The advantage of the three-input reduction is architectural regularity. Each local row or neighborhood can be reduced in parallel, and only the required high, median, and low candidates need to propagate to later stages. This limits the amount of data participating in downstream comparisons and avoids a complete nine-element ordering operation.

4.3 Multi-Level 3×3 Median Network

The complete RTINR datapath accepts nine pixels P0–P8. Three adaptive-neighborhood blocks process three local groups and produce H1/M1/L1, H2/M2/L2, and H3/M3/L3. Intermediate decision blocks then select candidates from the local high and low groups, while a further adaptive-neighborhood block processes the local medians. The final stage combines the surviving candidates and generates the median output MOUT.

The network is deliberately asymmetric: only values that can still become the global median are forwarded. Extremely high and extremely low candidates are progressively eliminated. This candidate-pruning view explains why the design can use fewer resources than a generic full sorting network while still obtaining the required central order statistic for the evaluated 3×3 window.

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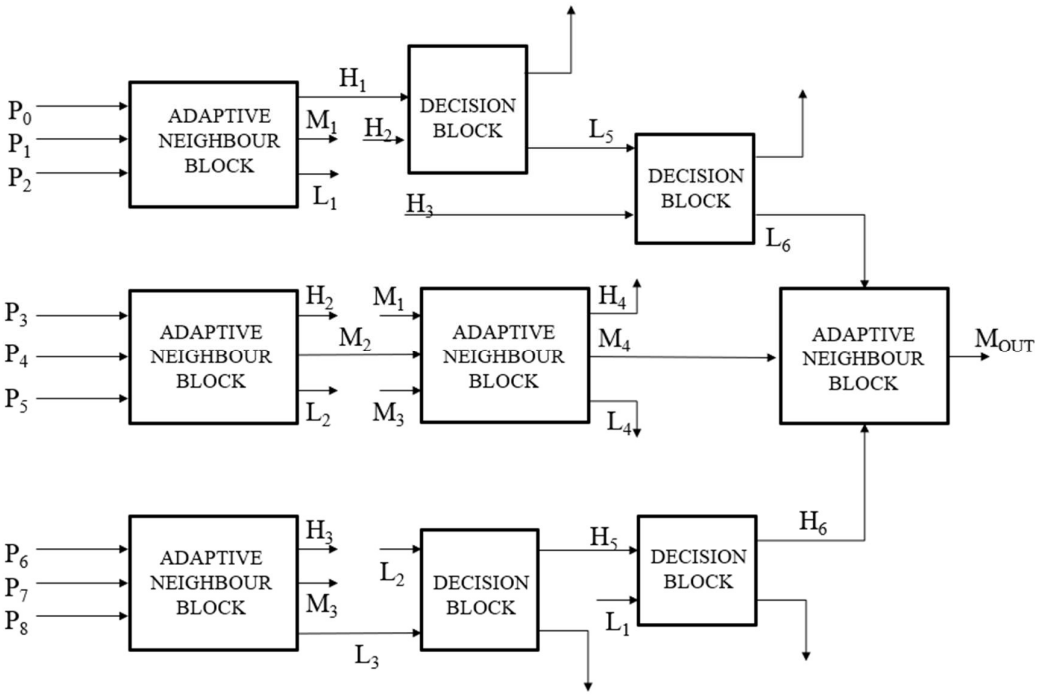

Fig. 3. Hardware architecture of the RTINR median-selection network for nine input pixels P0–P8.

4.4 Numerical Operation Example

The supplied design includes a numerical example that traces the progression of sample values through the comparison network. The local high, median, and low candidates are successively narrowed until the median is obtained. This example is useful for hardware verification because the value on each internal branch can be checked against the expected ordering relation, making it easier to validate RTL behavior before synthesis.

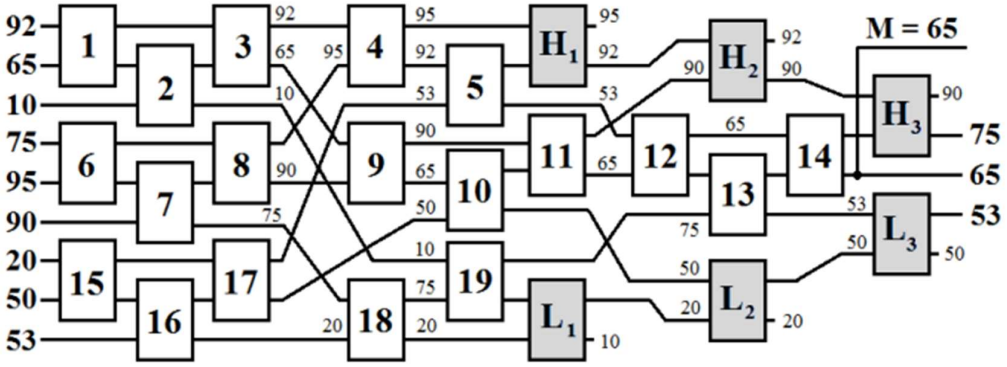

Fig. 4. Example of RTINR median selection through the cascaded decision network.

4.5 RTL Realization and Dataflow

The architecture is suitable for Verilog RTL because each decision block can be described with combinational comparison and multiplexing logic. The 3×3 pixel values are presented as 8-bit words, and intermediate signals carry the

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corresponding local extrema and medians. Since the filter is composed of repeated modules, the RTL can be developed hierarchically: a two-input decision cell, a three-input adaptive-neighborhood cell, and the top-level nine-pixel median module.

For streaming image processing, the median core would normally be combined with line buffers and a sliding-window generator so that a new 3×3 neighborhood is supplied as the image raster advances. The supplied study focuses on the median-selection core and reports the synthesis, timing, power, and image-quality results of that core. Therefore, system-level line-buffer cost is not included in the reported LUT and power figures and should be considered separately when integrating the filter into a complete camera pipeline.

V. EXPERIMENTAL METHODOLOGY

5.1 Hardware Evaluation

The RTL design was simulated and synthesized using Xilinx ISE. Functional simulation was used to verify that the nine input bytes produced the expected median output. Synthesis reports were then used to obtain LUT utilization, path delay, and power. The design summary reports 437 slice LUTs used out of 303,600 available resources on the selected device. Timing analysis reports a total path delay of 20.375 ns, consisting of 1.726 ns logic delay and 18.649 ns routing delay. The corresponding on-chip power report gives a total of 32.83 mW.

5.2 Image-Quality Evaluation

MATLAB R2020a was used for image-level evaluation. The supplied experiment compares the proposed RTINR output with standard median filtering (SMF), decision median filtering (DMF), and adaptive median filtering (AMF). The reported objective metrics are peak signal-to-noise ratio (PSNR) and structural similarity index (SSIM), while qualitative assessment is performed by visual comparison of the original, noisy, and filtered images.

5.3 Evaluation Metrics

Hardware efficiency is evaluated using three direct implementation metrics: LUT count as a proxy for area, worst-case path delay as a measure of speed, and total on-chip power as a measure of energy demand. Image restoration quality is evaluated using PSNR and SSIM. Higher PSNR generally indicates lower reconstruction error, while SSIM measures preservation of structural information and approaches 1 for high similarity to the reference image.

VI. RESULTS AND DISCUSSION

6.1 Functional Simulation

The functional simulation waveform confirms the operation of the nine-input median core. In the reported test case, P0–P8 are applied as 8-bit input values and the median output stabilizes at the expected byte value. The waveform provides a direct RTL-level check that the hierarchy of decision blocks produces the correct central order statistic for the applied neighborhood.

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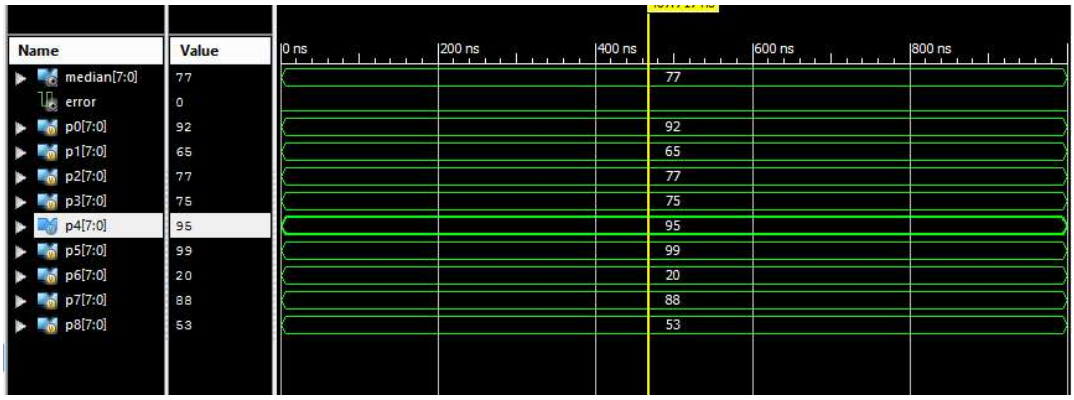

Fig. 5. Functional simulation result of the RTINR hardware core.

6.2 Area Utilization

The synthesis summary reports 437 slice LUTs. Compared with the baseline values given in the supplied study—767 LUTs for SMF, 655 for DMF, and 542 for AMF—the proposed RTINR reduces LUT usage by approximately 43.0%, 33.3%, and 19.4%, respectively. These reductions are consistent with the design strategy of forwarding only median-relevant candidates instead of fully sorting all nine samples.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	437	303600	0%
Number of fully used LUT-FF pairs	0	437	0%
Number of bonded IOBs	81	700	11%

Fig. 6. FPGA design-utilization summary reported for the proposed RTINR architecture.

6.3 Timing Performance

The reported total path delay is 20.375 ns. Of this, 1.726 ns is attributed to logic and 18.649 ns to routing, meaning that routing contributes about 91.5% of the critical path. This observation is important: the logical depth of the decision network is relatively small, but placement and interconnect dominate the final delay. Therefore, floorplanning, pipelining, or implementation on a newer FPGA family could potentially yield additional speed improvement without changing the filtering algorithm.

Relative to the baseline delays of 51.927 ns (SMF), 43.837 ns (DMF), and 32.735 ns (AMF), the RTINR delay is lower by approximately 60.8%, 53.5%, and 37.8%, respectively. The design is therefore favorable for real-time pipelines where the filter must operate as an early preprocessing stage before feature extraction or classification.

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```
LUT6:I0->O            1    0.043   0.350  c14/a[7]_b[7]_LessThan_1_o22
LUT6:I5->O           14    0.043   0.422  c14/a[7]_b[7]_LessThan_1_o24
LUT4:I3->O            3    0.043   0.507  c14/a[7]_b[7]_LessThan_1_o25
LUT6:I3->O            1    0.043   0.613  H3/a[7]_b[7]_LessThan_1_o3 (H
LUT6:I0->O            1    0.043   0.405  H3/a[7]_b[7]_LessThan_1_o4 (H
LUT3:I1->O            2    0.043   0.410  H3/a[7]_b[7]_LessThan_1_o1_SW
LUT5:I3->O            1    0.043   0.000  H3/a[7]_b[7]_LessThan_1_o1_G
MUXF7:I1->O           1    0.178   0.405  H3/a[7]_b[7]_LessThan_1_o1 (H
LUT5:I3->O            6    0.043   0.631  H3/a[7]_b[7]_LessThan_1_o21 (
LUT5:I0->O            1    0.043   0.613  H3/Mmux_13 (h31<2>)
LUT6:I0->O            1    0.043   0.405  median[7]_h31[7]_LessThan_1_o
LUT5:I3->O            1    0.043   0.613  median[7]_h31[7]_LessThan_1_o
LUT6:I0->O            1    0.043   0.339  error5 (error_OBUF)
OBUF:I->O                  0.000          error_OBUF (error)
----------------------------------------
Total                     20.375ns (1.726ns logic, 18.649ns route)
                                   (8.5% logic, 91.5% route)
```

Fig. 7. Timing report showing the 20.375 ns total path delay of the proposed design.

6.4 Power Consumption

The on-chip power report gives 32.83 mW total power. The majority is reported as quiescent power, while the design-related clock, logic, signal, and I/O components form a smaller portion of the total. Against the baseline power values of 82.61 mW, 73.41 mW, and 58.26 mW for SMF, DMF, and AMF, respectively, the reported RTINR value corresponds to reductions of about 60.3%, 55.3%, and 43.7%.

```
2.  Summary
2.1.  On-Chip Power Summary
+-------------------------------------------------------------------------------+
|                          On-Chip Power Summary                                |
+-------------------------------------------------------------------------------+
|        On-Chip        | Power (mW) |  Used  | Available | Utilization (%) |
+-------------------------------------------------------------------------------+
| Clocks                |       1.30 |      3 |    ---    |       ---       |
| Logic                 |       0.00 |     10 |     11776 |               0 |
| Signals               |       0.00 |     20 |    ---    |       ---       |
| IOs                   |       0.00 |     20 |       372 |               5 |
| Quiescent             |      31.52 |        |           |                 |
| Total                 |      32.83 |        |           |                 |
+-------------------------------------------------------------------------------+
```

Fig. 8. On-chip power summary reported for the proposed RTINR design.

6.5 Image Restoration Quality

Visual results show that the proposed RTINR output is closer to the original image than the compared baseline outputs in the reported test. The SMF and AMF examples retain more visible residual noise, while the DMF result improves the image but still shows greater degradation than RTINR. The proposed output preserves the main facial and edge structures with substantially reduced impulse noise.

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Fig. 9. Visual comparison from the supplied study: (a) original image, (b) noisy image, (c) SMF, (d) DMF, (e) AMF, and (f) proposed RTINR.

TABLE I. PERFORMANCE COMPARISON REPORTED IN THE SUPPLIED STUDY

Metric	SMF	DMF	AMF	Proposed RTINR
LUTs	767	655	542	437
Time delay (ns)	51.927	43.837	32.735	20.375
Power consumption (mW)	82.61	73.41	58.26	32.83
PSNR (dB)	37.34	42.45	48.38	54.53
SSIM	0.827	0.893	0.927	0.992

The objective image metrics reinforce the visual observation. The proposed RTINR records 54.53 dB PSNR and 0.992 SSIM, compared with 48.38 dB and 0.927 for AMF, 42.45 dB and 0.893 for DMF, and 37.34 dB and 0.827 for SMF. The PSNR gain over the strongest baseline in the table (AMF) is 6.15 dB, while the SSIM increases by 0.065. These values suggest that the resource reductions are not obtained by sacrificing the reported restoration quality.

6.6 Area–Speed–Power–Quality Trade-Off

The most significant result is the simultaneous improvement across both hardware and image-quality metrics. In many approximate-hardware designs, area or power savings are achieved by allowing a measurable loss in numerical accuracy. Here, the proposed decision-network organization reduces the reported LUT, delay, and power figures while the image-quality metrics increase. This behavior indicates that the principal efficiency gain comes from architectural restructuring rather than from intentionally approximating the median value.

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The delay report also reveals the next optimization opportunity. Because routing accounts for more than ninety percent of the reported critical path, further gains are likely to depend more on physical implementation than on Boolean simplification. Register insertion between candidate-reduction stages could shorten combinational paths and enable a higher clock frequency at the cost of additional latency and registers. Such pipelining would be particularly suitable for streaming video, where throughput is more important than single-window latency.

VII. PRACTICAL APPLICABILITY AND LIMITATIONS

The proposed architecture is well suited to FPGA-based preprocessing in systems that receive noisy gray-scale image streams and require a compact impulse-noise-removal stage. Potential applications include embedded surveillance, machine vision, portable medical-imaging front ends, robotics, industrial inspection, and sensor nodes. The repeated decision-block structure also makes the design amenable to parameterized RTL reuse.

Several limitations should be recognized when interpreting the reported results. First, the supplied hardware results correspond to the median-selection core and do not explicitly include a complete line-buffer/window-generation subsystem. Second, the image-quality table is based on the evaluated image case reported in the supplied document; a publication-grade validation should include multiple standard test images, multiple impulse-noise densities, and statistical aggregation of PSNR and SSIM. Third, the study reports Xilinx ISE synthesis results on one target configuration; portability should be verified on modern FPGA families and, where possible, ASIC technology. Finally, robustness against random-valued impulse noise, Gaussian noise, and mixed-noise conditions should be evaluated separately because the optimal detection and restoration strategy can differ from fixed-valued salt-and-pepper noise.

VIII. FUTURE WORK

Future development can proceed in four directions. A streaming implementation can integrate dual-line buffers and a sliding 3×3 window generator so that one filtered pixel is produced per clock after pipeline filling. The median network can be pipelined at stage boundaries to reduce routing-dominated timing. An adaptive corruption detector can be added so that clean center pixels bypass the median network, reducing unnecessary modification of uncorrupted image detail. Finally, the architecture can be evaluated across a broader benchmark set and synthesized on newer FPGA devices to characterize frame rate, energy per pixel, and scalability to higher image resolutions.

IX. CONCLUSION

This paper presents a hardware-oriented RTINR architecture based on decision-based multiplexers and adaptive-neighborhood median selection. The design transforms the 3×3 median operation into a hierarchy of compact high/low and high/median/low selector blocks, thereby avoiding a full nine-element sorting network. The supplied synthesis results report 437 LUTs, 20.375 ns total path delay, and 32.83 mW on-chip power. The image experiment reports 54.53 dB PSNR and 0.992 SSIM, exceeding the corresponding SMF, DMF, and AMF values in the supplied comparison. These results support the use of comparator/multiplexer-centric candidate reduction as an effective strategy for low-resource, real-time FPGA image denoising. Broader multi-image and multi-noise-density evaluation, together with streaming line-buffer integration and pipelining, will further strengthen the architecture for deployment in practical embedded vision systems.

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