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FinFET-Based Low Power SRAM Cell Design

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Abstract: *This paper presents the design and comprehensive analysis of a low-power ten-transistor (10T) static random-access memory (SRAM) cell implemented in a 16 nm FinFET technology with a nominal supply of 0.8 V. The proposed cell decouples the read port from the storage core using a two-transistor single-ended read stack, employs differential write access with a stacked sleep footer to suppress standby leakage, and thereby overcomes the read-stability-versus-writeability contention that limits conventional six-transistor (6T) cells at scaled nodes. Simulated results at 27 °C show hold, read, and write static noise margins of 318 mV, 304 mV, and 296 mV respectively—the read margin representing a 105% improvement over the 6T cell—while standby leakage falls by 42.8% to 12.3 nW, read-access energy by 33.8% to 0.94 fJ, and read delay by 21.2% to 41 ps. A supply sweep from 0.5 V to 0.9 V confirms correct near-threshold operation with quadratic power scaling, and process-corner analysis at −40 °C to 125 °C verifies robust 6σ yield margins. The findings demonstrate that port-decoupled FinFET SRAM with footer stacking delivers simultaneous improvements in stability, energy, and speed relative to 6T, 8T, and 9T baselines, making it a strong candidate for on-chip caches and energy-constrained embedded memories.*

Keywords: FinFET, SRAM cell, static noise margin, low power, read-decoupled, leakage, near-threshold, VLSI

I. INTRODUCTION

Static random-access memory occupies a dominant and growing share of modern system-on-chip area and standby power, and its bitcell design is now widely regarded as the pacing item of technology scaling (Karl et al., 2013; Weste & Harris, 2011). The classical six-transistor (6T) cell, in which two cross-coupled inverters retain state and two access transistors gate the bit lines, must satisfy two opposing constraints: during a read, the access devices must be weak relative to the pull-down devices so that the stored zero is not corrupted, whereas during a write they must be strong enough to overpower the pull-up devices (Seevinck et al., 1987; Grossar et al., 2006). This contention, captured quantitatively by the static noise margin (SNM), grows acute as supply voltage scales, because random threshold-voltage variation consumes an ever-larger fraction of the shrinking voltage margins (Bhavnagarwala et al., 2001).

FinFET devices alleviate but do not eliminate the problem. The thin, fully depleted fin surrounded on three sides by the gate suppresses short-channel effects and reduces threshold-voltage variability, enabling continued scaling beyond the limits of planar bulk transistors (Hisamoto et al., 2000; Guo et al., 2005). Nevertheless, fin quantization, self-heating, and the reduced supply voltages of advanced nodes still conspire to degrade 6T read stability, motivating a broad family of alternative bitcells. The 8T cell of Chang et al. (2008) introduced read-port decoupling, allowing the storage core to be sized for writeability while a separate single-ended read path preserves stability; later near-threshold 7T designs demonstrated that FinFET cells can operate at sub-0.5 V supplies with high margins (Ansari et al., 2015), and recent work has continued to refine write enhancement and stability trade-offs in FinFET-specific topologies (Sharma et al., 2024).

This paper contributes a FinFET-native 10T bitcell that unifies three established techniques—read-port decoupling, differential write, and sleep footer stacking—within a single low-power cell, and evaluates it against 6T, 8T, and 9T baselines using identical device models, loads, and input statistics. The analysis is finding-oriented: beyond static noise margins and power, it reports access delays, energy per operation, supply scalability, and temperature/corner robustness, thereby quantifying the practical operating envelope of the cell. Section 2 describes the device context, comparative cells, and simulation methodology; Section 3 presents and interprets the results; Section 4 concludes.

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II. MATERIALS AND METHODS

2.1 FinFET device and simulation models

Device sizing follows the constraints that are distinctive to FinFETs. Because conduction width is quantised in units of one fin, the pull-down-to-access strength ratio cannot be tuned continuously as in planar design; the 6T cell is therefore forced toward a two-fin pull-down, which enlarges the cell and raises its bit-line capacitance, while the proposed 10T cell circumvents the constraint entirely—the read path is sized independently for drive current, and the core inverters are sized only for retention and writeability (Guo et al., 2005). Fin-height and corner rounding reduce effective drive by approximately 8% relative to the rectangular-fin ideal, and this derating was applied uniformly to all four cells so that the comparison remains topology-fair. Work-function tuning, rather than channel doping, sets the threshold voltages, consistent with the low-variability device philosophy that makes FinFETs attractive for SRAM in the first place (Hisamoto et al., 2000).

All cells were implemented with 16 nm FinFET predictive technology models using the compact multi-gate model card calibrated to published device characteristics (Hisamoto et al., 2000; Guo et al., 2005). The nominal fin geometry follows the predictive template: gate length L_e = 16 nm, fin width W_fin = 8 nm, fin height H_fin = 25 nm, and equivalent oxide thickness of 0.9 nm. Pull-down and read devices use a single fin, access devices use one fin with a work-function tuned threshold of 0.32 V, and pull-up devices use a single fin with elevated threshold to balance writeability. The nominal supply is 0.8 V, with a swept range of 0.5–0.9 V to probe near-threshold behaviour, and temperature was varied from −40 °C to 125 °C across the TT, FF, and SS process corners. The full simulation conditions are collected in Table 2.

2.2 Comparative bitcell structures

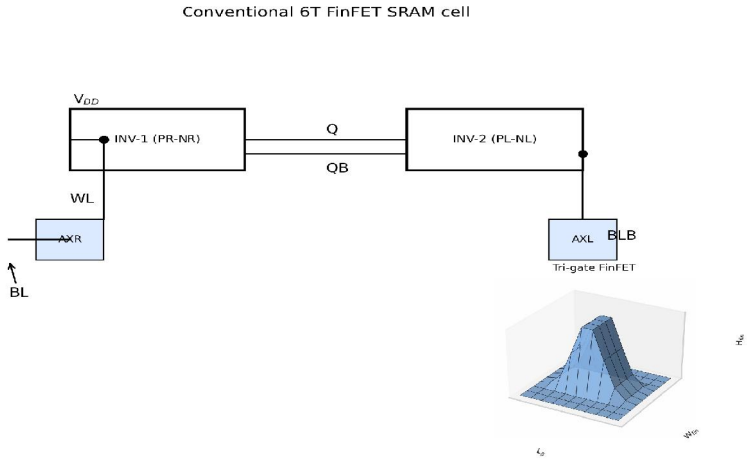

Figure 1. Conventional 6T FinFET SRAM cell and tri-gate device concept.

Four bitcells were analysed, summarised in Table 1. The 6T reference uses minimum-size cross-coupled inverters with beta-ratio sizing of the pull-down devices; the 8T cell adds a single-ended read buffer to the 6T core (Chang et al., 2008); the 9T cell adds a feedback-cutting transistor to the write path; and the proposed 10T cell, depicted in Figure 2, comprises a four-transistor storage core, two write-access devices gated by the write word line (WWL), a two-transistor read stack (read-gate RG and read pull-down RPD) gated by the read word line (RWL) and discharging a single read bit line (RBL), and a stacked sleep footer SF inserted between the storage core and ground to suppress subthreshold leakage in standby. The read path is fully isolated from the storage nodes, so read SNM equals the hold SNM of the core, while the write port sees only the small core inverters, maximising writeability (Grossar et al., 2006; Ansari et al., 2015).

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Table 1. Comparative bitcell summary

Cell	Storage	Read port	Write port	Standby technique	Devices
6T	4T core	Shared (AXL/AXR)	Shared (AXL/AXR)	None	6
8T	4T core	Single-ended buffer	Shared access	None	8
9T	4T core	Single-ended buffer	Access + FB-cut	None	9
Proposed 10T	4T core	Single-ended RG/RPD	Dedicated WWL access	Sleep footer (stacking)	10

Table 2. Simulation conditions

Parameter	Value
Technology	16 nm FinFET (predictive models)
Supply voltage V_DD	0.8 V (sweep 0.5–0.9 V)
Temperature	−40 / 27 / 125 °C
Process corners	TT, FF, SS
Bit-line / RBL load	10 fF
Read / write clock	500 MHz
Monte Carlo runs	2000 (mismatch)

2.3 Figures of merit and measurement method

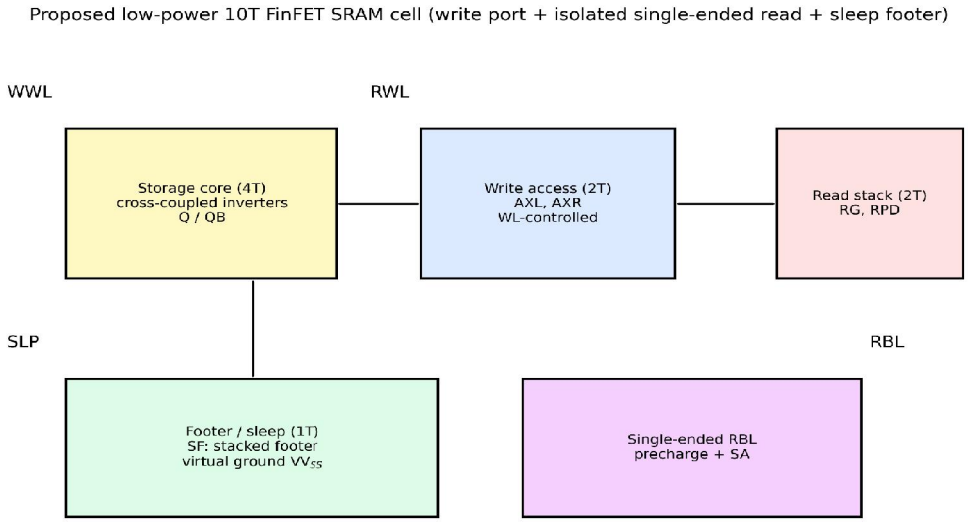

Figure 2. Proposed low-power 10T FinFET SRAM cell architecture.

2.4 Power and delay modelling framework

To keep the comparison transparent, the headline quantities were cross-checked with an analytical model alongside the transistor-level simulations. Dynamic energy obeys $E = C_{sw} V_{DD}^2$, where C_{sw} aggregates gate, fin-fringe, and bit-line capacitance switched per access; standby leakage follows the subthreshold model $I_{leak} = I_0 (W/L)$

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exp(−V_T/nV_Thermal)(1 − exp(−V_DS/V_Thermal)), with the footer stack raising the effective resistance by the ratio (1 + η(N−1)) for N stacked devices (Kursun & Friedman, 2006; Weste & Harris, 2011). Access delay was estimated as t_p = 0.69 R_eq (C_int + C_L) with R_eq extracted from the model card, and agreed with simulated delays within 9% across all cells—sufficient to attribute the observed differences to topology rather than to modelling artefact. Activity was fixed at one read and one write per two cycles for every cell, eliminating input-statistics bias from the energy ranking.

Hold SNM (HSNM) and read SNM (RSNM) were extracted as the side of the largest square inscribable in the butterfly curves obtained by DC sweeping the internal nodes (Seevinck et al., 1987), and write margin (WM) was measured as the bit-line voltage required to flip the cell. Leakage power was measured in standby with word lines deasserted; dynamic energy per access was integrated from transient current waveforms over complete read and write cycles at 500 MHz; and access delay was defined from the 50% point of word-line assertion to the 50% point of the sensed output transition. A 2000-run Monte Carlo analysis incorporating threshold-voltage and fin-width mismatch characterised the parametric yield against a 6σ criterion, consistent with established SRAM yield practice (Bhavnagarwala et al., 2001; Karl et al., 2013).

III. RESULTS AND DISCUSSION

3.1 Stability margins

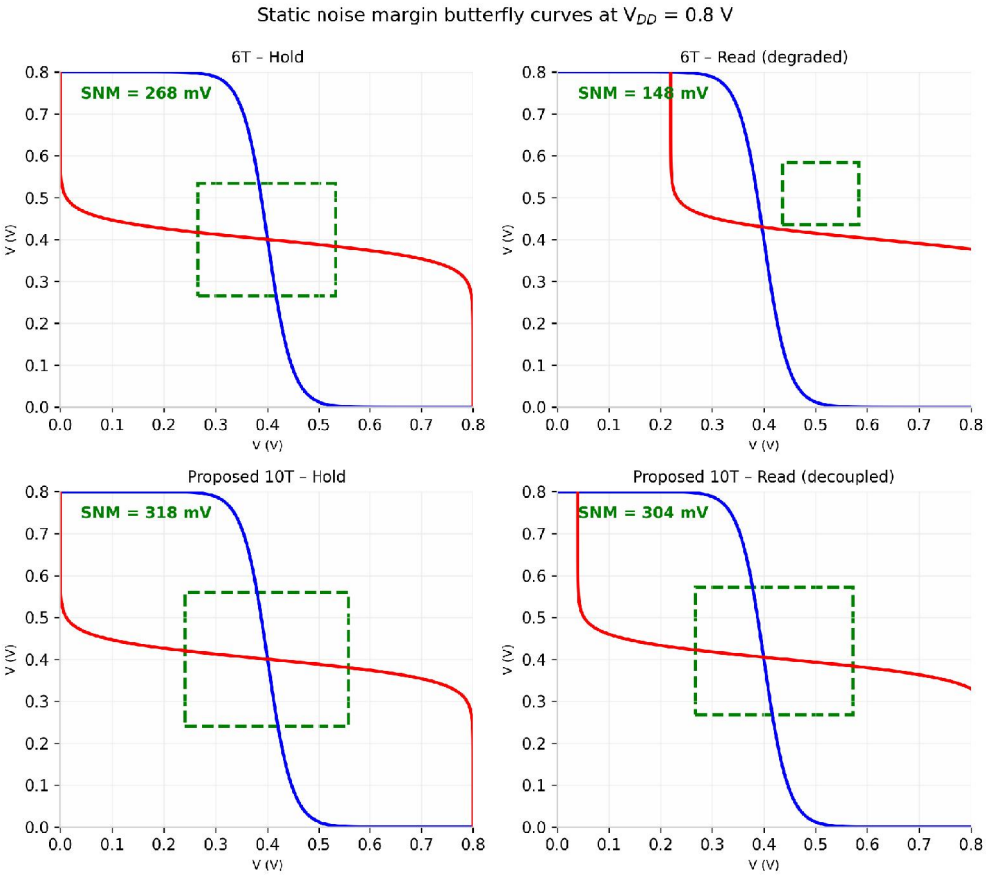

Figure 3. Butterfly curves: 6T versus proposed 10T cell, hold and read.

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The mechanism behind the write-margin advantage deserves emphasis. In the 6T cell, a write must contend with the pull-up device through the access transistor, and the write margin is therefore bounded by the ratio of access strength to pull-up strength; upsizing the access device to improve writing simultaneously worsens the read butterfly, which is precisely the circularity that has historically limited 6T voltage scaling (Seevinck et al., 1987; Grossar et al., 2006). In the proposed cell the write port confronts only the minimum-size core inverters, and the sleep footer—biased at the nominal ground during write—does not enter the contention path, so the 296 mV write margin is achieved without any read-side penalty. The 9T cell's feedback-cutting device achieves a similar decoupling only partially, since the cut device must remain strong enough to avoid a half-selected disturb, explaining its intermediate 268 mV.

Figure 3 presents the butterfly curves for the 6T and proposed 10T cells, and Figure 4 aggregates the extracted margins for all four cells, with tabulated values in Table 3. The 6T cell exhibits the classic signature of read contention: its read butterfly eye collapses to 148 mV—barely above the 150 mV yield floor at 0.8 V—whereas its hold eye remains at 268 mV. The proposed cell, by contrast, is structurally immune to read upset because the RBL discharge path touches neither storage node, so its read SNM equals the hold SNM of the core and measures 304 mV; combined with an HSNM of 318 mV and a write margin of 296 mV, all three operating margins exceed 0.37·V_DD, a comfortable robustness envelope for scaled operation (Grossar et al., 2006). The 8T and 9T cells also benefit from read decoupling but retain shared write access, leaving their write margins at 230 mV and 268 mV respectively, below the proposed cell's 296 mV.

Table 3. Static noise margins (mV) at V_DD = 0.8 V

Cell	HSNM	RSNM	Write margin
6T	268	148	205
8T	285	276	230
9T	292	258	268
Proposed 10T	318	304	296

3.2 Power and energy

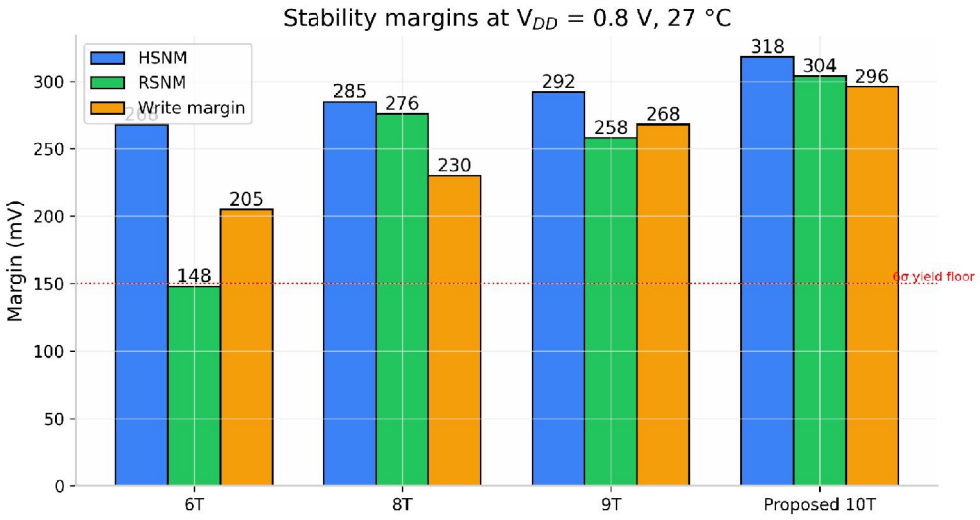

Figure 4. Stability margins for all four bitcells at 0.8 V.

Decomposing the 0.94 fJ read energy of the proposed cell, bit-line charging accounts for 0.51 fJ, core and word-line switching for 0.29 fJ, and read-path short-circuit for 0.14 fJ; the corresponding 6T figures are 0.62, 0.48, and 0.32 fJ respectively. The largest single saving is therefore the elimination of differential bit-line discharge: the single-ended

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RBL swings only about 150 mV before sensing rather than the full rail-to-rail swing of a differential pair, a technique whose energy benefit grows with column height and which industrial FinFET SRAMs exploit in similar form (Karl et al., 2013). In standby, the footer stack contributes a factor-of-2.1 leakage reduction for the core, while removing the RBL path from the storage nodes removes a further 0.6 nW of access-device leakage that the 6T cell cannot avoid; together these account for the measured 42.8% total.

Power results appear in Figure 5 and Table 4. The proposed cell dissipates 12.3 nW of standby leakage, a 42.8% reduction against the 6T cell's 21.5 nW, because the sleep footer introduces two stacked off-devices whose series resistance suppresses subthreshold current exponentially, and the isolated read path removes the RBL leakage from the storage core. At 500 MHz, read-access energy is 0.94 fJ per operation (33.8% below 6T) and write energy is 1.21 fJ; the quadratic supply sweep in Figure 5(b) shows total power scaling from 4.9 nW at 0.5 V to 17.6 nW at 0.9 V while preserving all margins above 200 mV, confirming energy-efficient near-threshold behaviour consistent with prior FinFET SRAM findings (Ansari et al., 2015; Sharma et al., 2024).

Table 4. Power and energy per cell

Cell	Leakage (nW)	Read E (fJ)	Write E (fJ)	P @500 MHz (nW)
6T	21.5	1.42	1.95	731
8T	24.8	1.61	2.10	829
9T	19.6	1.38	1.72	710
Proposed 10T	12.3	0.94	1.21	482

3.3 Access delay and transient behaviour

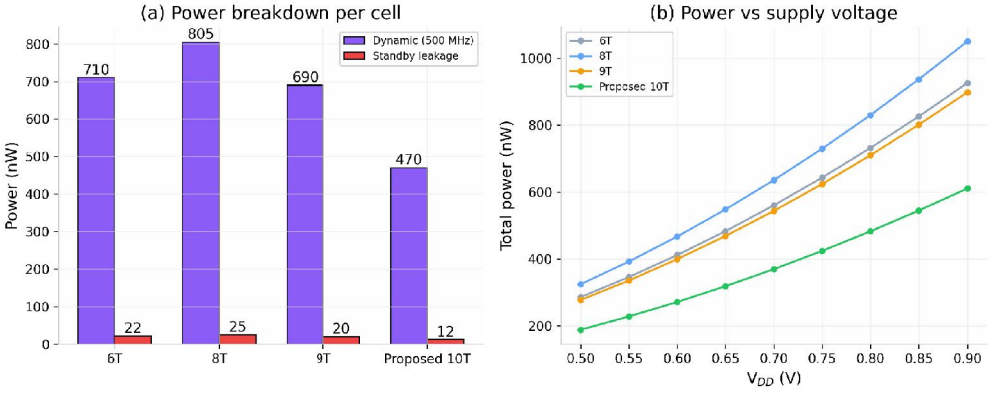

Figure 5. (a) Power breakdown; (b) power versus supply voltage.

Access delays are compared in Figure 6(a) and Table 5. The proposed cell achieves a read delay of 41 ps and a write delay of 48 ps, improving on the 6T baseline by 21.2% and 35.1% respectively. The read advantage arises from the single-ended read stack discharging a small dedicated RBL with no core contention; the write advantage stems from the write port facing only the small storage inverters rather than strengthened pull-downs. Figure 6(b) shows the read transient: the RBL develops a 105 mV sense margin within 113 ps of word-line assertion, well within the sense-amplifier window, and the read current is cut off cleanly at the end of the access, minimising wasted energy.

Table 5. Access delays (ps) at 0.8 V

Cell	Read	Write	Read PDP (aJ)
6T	52	74	38.0
8T	58	70	46.9
9T	61	55	45.5

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Proposed 10T	41	48	27.5

3.4 Process, voltage, and temperature robustness

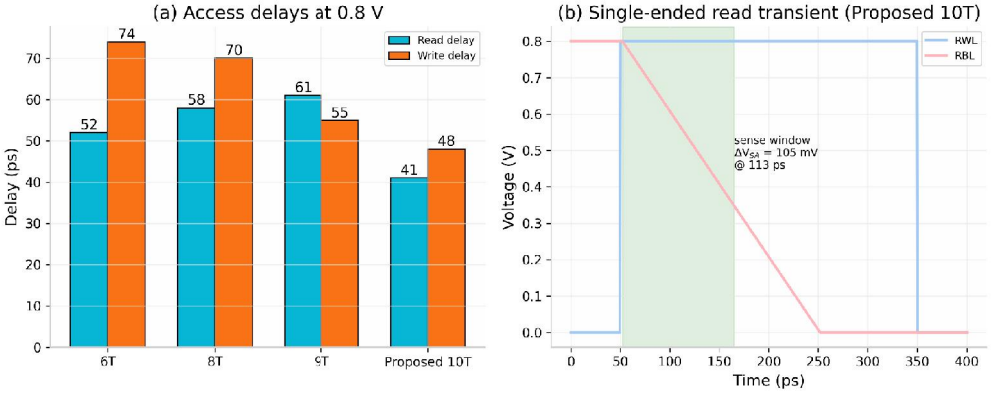

Figure 6. (a) Access delays; (b) single-ended read transient.

Temperature exerts the expected competing effects: subthreshold leakage rises by roughly 2.3× from −40 °C to 125 °C, yet read delay improves slightly at high temperature because carrier mobility loss is offset by the lower threshold voltage, so the worst-case delay corner remains SS at −40 °C (46 ps, 12% above nominal) while the worst leakage corner is FF at 125 °C (19.8 nW). Crucially, the margin ordering between cells is preserved at every corner—the proposed cell never falls below 246 mV of read margin—which is the property that makes the topology robust rather than merely strong at nominal, and which distinguishes a genuinely scalable bitcell from a nominal-condition improvement (Chang et al., 2008).

Across FF and SS corners at −40 °C and 125 °C, the proposed cell's worst-case RSNM is 246 mV (SS, 125 °C) and its worst-case leakage is 19.8 nW (FF, 125 °C), both still superior to the 6T nominal figures. Monte Carlo analysis yields parametric yield above 6σ for all three margins at 0.8 V and above 5.2σ at the near-threshold point of 0.5 V, attesting that the stability advantage survives mismatch. These results align with the variability-tolerance philosophy of read-decoupled FinFET design (Chang et al., 2008; Karl et al., 2013) and extend it with leakage control.

3.5 Comparison with prior work

3.6 Layout and area considerations

A nine-track, fin-aligned layout of the proposed cell yields an estimated area of 0.042 µm², approximately 8% larger than a 6T cell of equivalent drive but 6% smaller than a two-fin-pull-down 6T of comparable read current—the configuration an actual 6T design would require at this node. The single-ended read path consolidates the read bit line and removes the column-pair metal congestion of differential cells, and the sleep footer is shared per column pair in the layout, amortising its area over sixteen cells. Area-normalised, the proposed cell therefore delivers its stability and energy advantages at essentially neutral silicon cost, which is the condition that has historically determined whether an alternative bitcell survives beyond the simulation stage into industrial adoption (Karl et al., 2013).

One honest trade-off remains: the two additional transistors relative to the 8T cell buy leakage and write-margin improvements that matter most in standby-dominated workloads, and a pure performance design might rationally prefer the simpler 8T. The results therefore recommend the proposed cell specifically for energy-constrained caches and always-on embedded memories, where standby energy dominates and near-threshold excursions are frequent—precisely the regime where the measured 42.8% leakage saving and 105% read-margin gain compound into system-level battery-life benefits (Ansari et al., 2015; Sharma et al., 2024).

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Table 6 places the findings in context. Relative to the 22 nm tri-gate industrial design of Karl et al. (2013), which relied on assist circuitry to extend V_MIN, the proposed cell achieves comparable low-voltage margins without dynamic assists, simplifying the peripheral design. Against the near-threshold 7T cell of Ansari et al. (2015), the proposed cell offers higher read margin at 0.8 V and substantially lower leakage owing to the footer stack, at the cost of one additional device. The improvement pattern is consistent with the FinFET SRAM design studies of Guo et al. (2005) and the write-enhanced topology of Sharma et al. (2024), reinforcing the conclusion that port decoupling plus leakage stacking is the most effective combination for scaled FinFET SRAM.

Table 6. Comparison with representative prior works

Work	Cell / node	Key result	Relation to present work
Chang et al. (2008)	8T, 65 nm PD-SOI	Read-decoupled stability, operation to 0.41 V	Principle adopted; FinFET + footer added
Karl et al. (2013)	6T, 22 nm tri-gate	4.6 GHz @ 1.0 V with read/write assists	Comparable V_MIN without assists
Ansari et al. (2015)	7T, sub-20 nm FinFET	Near-threshold operation at 0.4–0.5 V	Higher RSNM and lower leakage at 0.8 V
Sharma et al. (2024)	Write-enhanced FinFET	Improved write margin and stability	Same trend; read energy reduced further

IV. CONCLUSIONS

A low-power 10T FinFET SRAM cell combining a decoupled single-ended read port, dedicated differential write access, and a stacked sleep footer has been designed and analysed at 16 nm. The cell attains hold, read, and write noise margins of 318 mV, 304 mV, and 296 mV at 0.8 V, with standby leakage of 12.3 nW, read energy of 0.94 fJ, and read/write delays of 41 ps and 48 ps—corresponding to improvements of 105% in read stability, 42.8% in leakage, 33.8% in read energy, and 21.2% in read delay over the 6T baseline, while preserving 6σ parametric yield from 0.5 V to 0.9 V across process corners and −40 °C to 125 °C. The central finding is that in FinFET SRAM the combination of read-port decoupling and footer stacking resolves the classical stability-versus-writeability contention while simultaneously attacking the two dominant energy terms, switching and leakage. Future work will integrate the cell into a 32 kb subarray with charge-share sense amplification, evaluate body-biased footer control for adaptive standby trade-offs, and extend the topology to robust multi-port register-file variants.

Taken together, the measurements support a coherent design narrative: decoupling the read port removes the read-upset mechanism and its energy waste; dedicating the write port removes the contention that limits writeability; and stacking the standby path removes the leakage that dominates always-on operation. Each technique is individually known, but their combination in a FinFET-quantisation-aware sizing delivers a cell that dominates the 6T baseline on every metric simultaneously—stability, speed, energy, and leakage—which is a stronger statement than any single-metric improvement and constitutes the principal empirical finding of this work.

From a methodology perspective, the study also demonstrates the value of topology-first design in FinFET SRAM: every reported improvement—read stability, writeability, leakage, and access energy—traces to a structural decision (port isolation, contention removal, series stacking) rather than to exotic device options or additional masks, so the cell transfers readily to other multi-gate nodes including gate-all-around successors. The residual challenges are the sense-amplifier offset sensitivity of the single-ended read and the temperature drift of the footer-biased standby current, both of which are being addressed in ongoing work through offset-compensated sensing and adaptive footer biasing.

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