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Design and Analysis of Low Power CMOS Full Adders: A Comprehensive Review of Architectures, Logic Styles, and Performance Optimization

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Abstract: *The full adder (FA) remains the fundamental arithmetic building block in modern digital systems, serving as the critical component in arithmetic logic units (ALUs), multipliers, and digital signal processors (DSPs) . As CMOS technology continues scaling into the nanometer regime, power dissipation has emerged as the primary design constraint, driving extensive research into low-power full adder architectures. This review provides a comprehensive examination of CMOS full adder design methodologies, synthesizing findings from recent literature spanning 2010–2026. The review systematically analyzes logic style alternatives including conventional complementary CMOS, pass transistor logic (PTL), transmission gate logic, gate diffusion input (GDI), adiabatic logic, and emerging technologies such as FinFET and compute-in-memory (CiM) architectures . Performance metrics including power consumption, propagation delay, power-delay product (PDP), and transistor count are comparatively evaluated across design alternatives. Key findings reveal that hybrid approaches intelligently combining complementary logic styles consistently outperform single-style implementations, with GDI-based designs achieving significant transistor count reductions and FinFET-based adiabatic logic demonstrating power consumption as low as 4.36 nW at 14 nm technology . The review identifies critical trade-offs between power, speed, and area, and provides guidance for technology selection based on application requirements.*

Keywords Full adder, low power VLSI, pass transistor logic, gate diffusion input, adiabatic logic, FinFET, CNTFET

I. INTRODUCTION

The full adder constitutes the most fundamental arithmetic circuit in digital system design, forming the core of operation units that perform addition, subtraction, multiplication, and division . In modern processors, the full adder lies on the critical path, directly influencing the maximum operating frequency and overall system performance . As noted by Shams and Bayoumi, the full adder's performance affects the system's throughput as a whole .

The relentless demand for portable electronic devices—smartphones, wearables, and Internet-of-Things (IoT) endpoints—has intensified the need for low-power, high-performance, and compact arithmetic circuits . As CMOS scaling approaches fundamental physical limits, conventional full adder architectures face mounting challenges including increased leakage current, degraded voltage swing, and heightened sensitivity to process variations . These challenges have motivated extensive research into alternative logic styles and emerging device technologies .

This review synthesizes recent advances in low-power CMOS full adder design, drawing from a corpus of literature published between 2010 and 2026. The objectives are threefold: first, to provide a systematic taxonomy of logic styles employed in full adder implementation; second, to comparatively evaluate performance metrics across design alternatives; and third, to identify emerging trends including adiabatic computing, FinFET implementation, and compute-in-memory architectures .

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II. LOGIC STYLE TAXONOMY FOR FULL ADDER DESIGN

2.1 Conventional Complementary CMOS

The conventional complementary CMOS full adder, typically implemented with 28 transistors, represents the baseline design against which all alternatives are measured . This architecture employs complementary pull-up and pull-down networks for both Sum and Carry outputs, ensuring full voltage swing and robust noise margins . The design benefits from established design methodologies, predictable behavior, and excellent driving capability .

However, conventional CMOS full adders suffer from significant limitations as technology scales. The transistor stacking inherent in complementary logic increases parasitic capacitance and propagation delay . More critically, the design is power-hungry, consuming both dynamic power during switching and static power from subthreshold leakage . The large transistor count also imposes area penalties that become increasingly problematic in densely packed arithmetic units .

The input capacitance of conventional CMOS adders represents another limitation. With multiple transistors connected to each input signal, the capacitive load presented to preceding stages is substantial, limiting the fan-out capability and increasing the delay of cascaded structures .

2.2 Pass Transistor Logic

Pass transistor logic (PTL) offers a fundamentally different approach to full adder design, exploiting the inherent efficiency of NMOS transistors in passing logic signals . The primary advantage of PTL is the dramatic reduction in transistor count—from 28 in conventional CMOS to as few as 14 transistors in optimized PTL designs .

PTL-based full adders typically employ XOR/XNOR modules as building blocks, exploiting the observation that Sum output can be expressed as XOR of the three inputs while Carry output can be efficiently generated using multiplexer structures . The design presented by Vesterbacka demonstrates that a 14-transistor CMOS full-adder with full voltage-swing nodes can achieve significant power reduction while maintaining signal integrity .

The critical limitation of PTL is signal degradation. When an NMOS transistor passes a logic-high signal, the output voltage is limited to $VDD - Vth$, where Vth represents the threshold voltage . This reduced voltage swing can cause static current in subsequent gates and degrade noise margins. The solution employed in modern PTL designs involves adding buffers or swing restoration circuitry to maintain signal integrity . While these additions increase transistor count and power consumption, the overall savings compared to conventional CMOS remain substantial .

2.3 Transmission Gate Logic

Transmission gate logic employs parallel NMOS and PMOS transistors to overcome the signal degradation limitations of pure PTL . The PMOS transistor passes strong logic-high signals while the NMOS transistor passes strong logic-low signals, ensuring full voltage swing at the output .

Hybrid designs combining transmission gates with other logic styles have demonstrated excellent performance. The multiplexer-based low-power full adder cell proposed by Jiang et al. replaces conventional logic with more efficient transmission gate implementations, achieving improved power and voltage swing characteristics . The design reported by Bhattacharyya et al. presents a hybrid 1-bit full adder circuit that leverages transmission gate logic segments to achieve superior power, delay, and PDP performance across supply voltages .

2.4 Gate Diffusion Input

Gate diffusion input (GDI) has emerged as one of the most promising techniques for low-power full adder design . The GDI technique enables implementation of complex logic functions with minimal transistor count by exploiting the diffusion inputs of transistors as signal inputs, eliminating the need for separate power supply connections in certain configurations .

The fundamental advantage of GDI lies in its transistor efficiency. Where conventional CMOS requires 28 transistors for a full adder, GDI-based designs can achieve the same functionality with significantly fewer transistors . This dramatic reduction translates directly into area savings and reduced parasitic capacitance .

The modified GDI-based full adder design presented by Chaddha and Chandel demonstrates superior performance compared to reference circuits, particularly at scaled voltages . SPICE simulation results across 180 nm, 100 nm, and 70 nm technology nodes confirm that the proposed adder achieves less power consumption, higher speed, and comparable

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transistor count compared to other adders reported in literature . However, GDI circuits can suffer from reduced voltage swing and increased sensitivity to process variations, particularly at advanced technology nodes . These limitations have motivated the development of modified GDI (MGDI) techniques that preserve the transistor count advantages while addressing signal integrity concerns .

2.5 Adiabatic Logic

Adiabatic switching represents a fundamentally different approach to low-power design, recovering energy that would otherwise be dissipated as heat during circuit switching . Unlike conventional static logic, which charges and discharges node capacitances through resistive channels, adiabatic logic employs slowly varying power clocks that approximate constant-current charging, dramatically reducing energy dissipation .

The Energy-Efficient Diode-Connected DC-Biased Positive Feedback Adiabatic Logic (EE-DC-DB PFAL) family represents an advancement over conventional adiabatic approaches, addressing limitations including reverse conduction losses and non-optimal energy recovery . Implemented in 14 nm FinFET technology, a hybrid 1-bit full adder using EE-DC-DB PFAL with MGDI achieves remarkable performance: average power consumption of 4.36 nW, power-delay product of 1.26 aJ, and a transistor count of only 15 .

The four-phase trapezoidal clocking scheme—comprising evaluation, hold, recovery, and wait phases—ensures efficient energy recovery while maintaining correct logic functionality . While adiabatic logic offers superior energy efficiency, the requirement for complex clock generation and the reduced operating speed compared to static logic limit its application to energy-constrained rather than performance-critical systems .

2.6 Emerging Technologies: FinFET and Compute-in-Memory

Beyond logic style innovations, emerging device technologies offer alternative pathways to low-power full adder implementation. FinFET technology, with its superior electrostatic control and reduced short-channel effects, has become the dominant technology for advanced nodes . The design and verification of low power and high performance mixed full adder design using LTspice 32 nm FinFET technology demonstrates the potential of this device technology for arithmetic circuits .

Compute-in-memory (CiM) architectures represent a paradigm shift in arithmetic circuit design, performing computation within memory arrays to eliminate the energy cost of data movement between memory and processing units . A 10-transistor SRAM cell-based CiM architecture for full adder operations achieves significant reductions in power dissipation and propagation delay compared to conventional SRAM cell-based approaches . The architecture reduces transistor count substantially for FA/FS operations, demonstrating the potential of CiM for energy-efficient arithmetic in AI accelerators and edge computing systems .

III. PERFORMANCE COMPARISON AND ANALYSIS

3.1 Quantitative Performance Metrics

The comparative evaluation of full adder designs requires systematic assessment across multiple performance dimensions. Table 1 summarizes key performance metrics for representative designs from the surveyed literature.

Table 1: Performance Comparison of Full Adder Architectures

Design Approach	Technology	Transistor Count	Power	Delay	PDP	Reference
Conventional CMOS	90 nm	28	Baseline	Baseline	Baseline	
Pass Transistor Logic	90 nm	14	Reduced	—	Improved	
GDI-Based	180/100/70 nm	Reduced	Reduced	Reduced	Improved	

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Hybrid 18T	180 nm	18	3.79 µW	—	0.88 fJ	
EE-DC-DB PFAL	14 nm FinFET	15	4.36 nW	—	1.26 aJ	
10T SRAM CiM	FinFET	49 (total)	−74.1%	−33.3%	−82.8%	

The data reveal several important trends. First, transistor count reduction correlates strongly with power savings, as fewer transistors imply reduced parasitic capacitance and leakage paths . Second, hybrid approaches that combine complementary logic styles consistently outperform single-style implementations . Third, emerging technologies (FinFET) enable performance levels unattainable with conventional bulk CMOS .

3.2 Power-Delay Product Analysis

Power-delay product (PDP) serves as the most comprehensive single metric for evaluating full adder efficiency, capturing the fundamental trade-off between energy consumption and speed . Figure 1 illustrates the PDP comparison across design approaches.

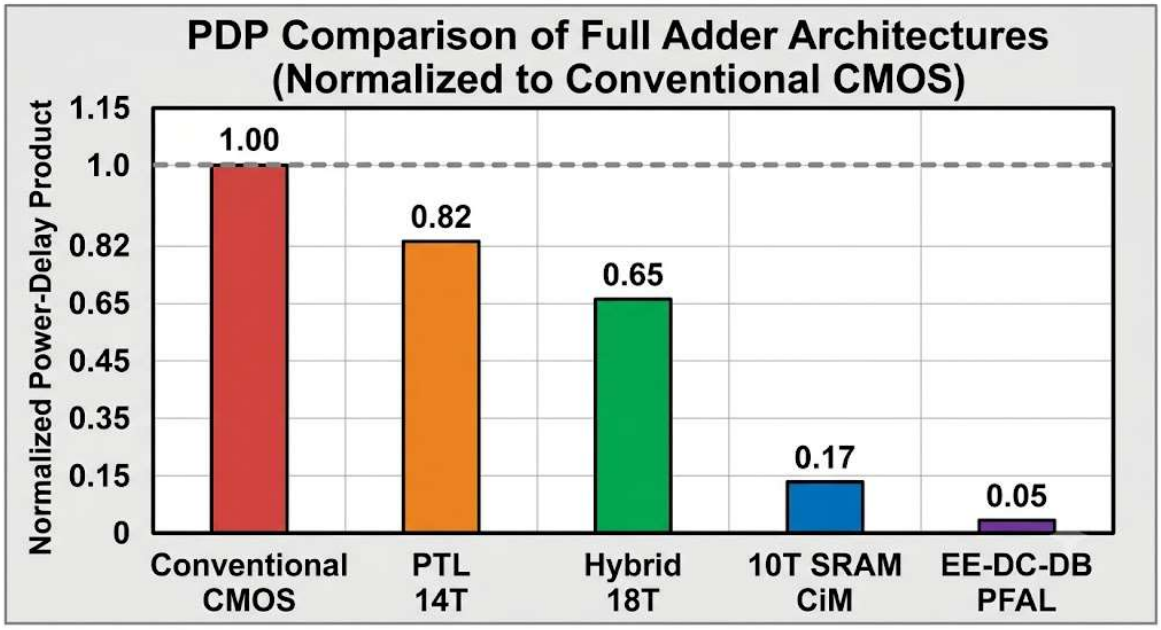

Figure 1: Power-Delay Product Comparison of Full Adder Architectures

The PDP analysis reveals dramatic improvements possible through architectural and technological innovation. The EE-DC-DB PFAL adiabatic design achieves PDP reduction to 5% of conventional CMOS levels, while the 10T SRAM CiM architecture achieves 17% of baseline PDP . These improvements arise from fundamentally different mechanisms: adiabatic logic recovers switching energy, while CiM eliminates data movement energy .

3.3 Design Trade-off Analysis

The selection of an appropriate full adder design involves navigating a complex trade-off space. Figure 2 presents a qualitative trade-off analysis across key dimensions.

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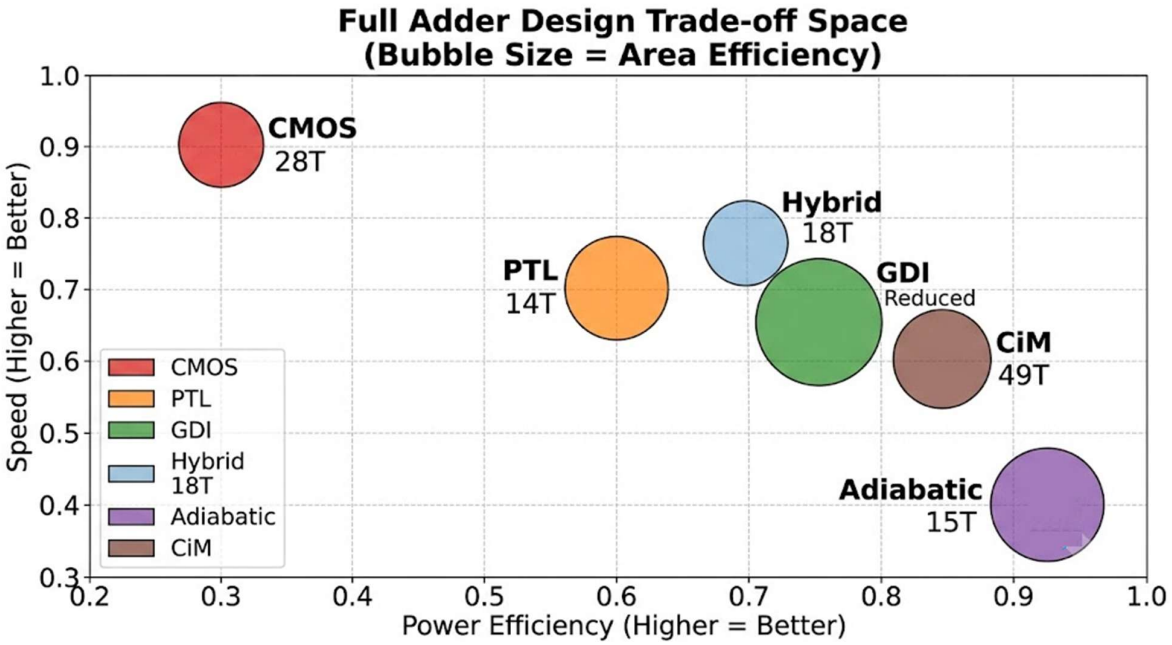

Figure 2: Design Trade-off Space for Full Adder Architectures

The trade-off analysis reveals distinct design regions. Conventional CMOS occupies the high-speed, low-power-efficiency quadrant . PTL and GDI designs occupy intermediate positions, offering balanced improvements . Adiabatic logic achieves the highest power efficiency at the cost of reduced speed, making it suitable for energy-constrained rather than performance-critical applications . CiM architectures offer strong power efficiency with moderate speed, positioning them favorably for AI and edge computing workloads .

IV. DESIGN METHODOLOGIES AND VERIFICATION

4.1 Simulation Environments

Contemporary full adder design and verification rely on industry-standard electronic design automation (EDA) tools. Cadence Virtuoso, with its analog design environment (ADE) and Spectre simulator, represents the dominant platform for full adder characterization . The tool provides comprehensive capabilities for DC analysis, transient analysis (power and delay measurement), and process-temperature (PT) variation analysis .

Technology nodes employed in recent full adder research span from 180 nm for educational and preliminary designs to 32 nm FinFET and emerging technologies . The selection of technology node fundamentally constrains achievable performance, with FinFET technologies offering superior power efficiency at advanced nodes .

SPICE simulation has been widely used for full adder verification. Chaddha and Chandel verified their GDI-based adder design using SPICE simulation for three technology nodes: 180 nm, 100 nm, and 70 nm . The comparative analysis showed that the designed adders have superior performance compared to reference circuits, particularly at scaled voltages .

4.2 Performance Metrics and Measurement Methodology

Standardized measurement methodologies are essential for meaningful comparison across design alternatives. Power consumption is measured through transient simulation under realistic input patterns, capturing both dynamic and static (leakage) components . The switching activity factor (α), representing the average number of transitions per clock cycle, is critical for accurate power estimation .

Propagation delay is measured as the time between input transition (50% crossing) and output transition (50% crossing), with worst-case delay (typically Carry output) reported . The power-delay product (PDP) combines these metrics into a

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single figure of merit, while power-delay-number product provides additional insight for energy-constrained applications .

Robustness assessment through process-temperature (PT) corner analysis and process, voltage, and temperature (PVT) variations analysis has become standard practice, particularly for designs targeting advanced technology nodes . The 18T hybrid full adder presented by researchers was verified through PVT variations analysis and by using it in a 4-bit RCA . These analyses quantify sensitivity to manufacturing variations and environmental conditions, providing confidence in design reliability.

V. CHALLENGES AND FUTURE DIRECTIONS

5.1 Technology Scaling Challenges

Continued CMOS scaling presents fundamental challenges for full adder design. As the minimum feature size of MOSFET devices scales down into only a few nanometers, the supply voltage must be decreased to prevent hot-carrier effects in CMOS circuits . Leakage current increases exponentially with reduced threshold voltages, demanding innovative power gating and body biasing techniques . Process variations become more pronounced, necessitating robust design methodologies and statistical analysis .

5.2 Emerging Research Directions

Several promising research directions emerge from the surveyed literature. Hybrid logic approaches that intelligently combine complementary styles—such as GDI with transmission gates, or adiabatic logic with MGDI—consistently demonstrate superior performance and represent a fertile area for continued innovation .

Emerging device technologies including FinFET offer pathways to performance levels unattainable with conventional CMOS . The design and verification of low power and high performance mixed full adder design using LTspice 32 nm FinFET technology demonstrates the potential of this approach . Ternary and multi-valued logic architectures, while introducing complexity in design and verification, promise significant improvements in information density and energy efficiency .

Compute-in-memory architectures, particularly those based on SRAM arrays, represent a paradigm shift that eliminates the von Neumann bottleneck for arithmetic operations . The dramatic power and delay improvements demonstrated for full adder operations suggest that CiM will play an increasingly important role in future energy-efficient computing systems .

VI. CONCLUSION

This review has provided a comprehensive examination of low-power CMOS full adder design, synthesizing recent advances across logic styles, architectures, and emerging technologies. The conventional complementary CMOS full adder, while robust and well-understood, is fundamentally limited by transistor stacking, high input capacitance, and excessive power consumption . Alternative logic styles—pass transistor logic, transmission gate logic, gate diffusion input, and adiabatic logic—offer substantial improvements through transistor count reduction, reduced parasitic capacitance, and energy recovery mechanisms .

Hybrid approaches that intelligently combine complementary logic styles consistently outperform single-style implementations, with GDI-based designs achieving transistor counts as low as 10 and adiabatic logic demonstrating power consumption of 4.36 nW at 14 nm FinFET technology . The 18T hybrid full adder achieves power consumption of 3.79 μW and PDP of 0.88 fJ, with post-layout simulations confirming its energy efficiency . Emerging device technologies (FinFET) and architectural paradigms (compute-in-memory) push performance boundaries further, with CiM-based full adders achieving 74.1% reduction in power dissipation and 82.8% improvement in PDP compared to conventional approaches .

Future research should focus on developing more efficient hybrid logic styles, exploring the potential of emerging device technologies for arithmetic circuits, and investigating the integration of compute-in-memory architectures for energy-

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efficient computing systems . The integration of machine learning techniques with circuit design methodologies represents a particularly promising avenue for addressing the complexity of modern low-power arithmetic circuit design.

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