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FinFET-Based Low Power SRAM Cell Design: A Comprehensive Review

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Abstract: *Static Random Access Memory (SRAM) remains the dominant on-chip memory technology, occupying over 50% of chip area in modern microprocessors and serving as the backbone of cache hierarchies, register files, and AI accelerators (Evolution of SRAM Architectures, 2026). As CMOS technology scaling approaches fundamental physical limits below 10 nm, conventional planar SRAM cells face critical challenges including excessive leakage power, degraded static noise margin (SNM), and heightened process variability sensitivity. FinFET technology has emerged as the dominant solution, offering superior electrostatic control through multi-gate architecture and demonstrated leakage reduction up to 40% with 10–20% SNM improvement compared to planar CMOS (Evolution of SRAM Architectures, 2026). This review provides a comprehensive examination of FinFET-based low power SRAM cell design methodologies, synthesizing findings from literature spanning 2018–2026. The review systematically analyzes architectural alternatives including conventional 6T configurations, 7T and 8T cells with decoupled read ports, 9T dual-port structures, and 10T variants optimized for stability and power. Read/write assist techniques including word-line under-drive (WLUD), transient voltage collapse (TVC), negative bit-line (NBL), and combined read-write assist strategies are comparatively evaluated. Emerging optimization approaches including metaheuristic algorithms and machine learning-informed design methodologies are examined. Key findings reveal that FinFET-based SRAM cells achieve substantial improvements across all performance metrics, with power dissipation as low as 0.985 μW, propagation delay of 0.97 ns, and PDP of 2.01×10^{-15} W-s demonstrated at advanced technology nodes (Improving FinFET Device Parameters, 2025). The review identifies critical trade-offs between stability, power, and area, providing guidance for technology selection based on application requirements.*

Keywords: FinFET, SRAM, low power VLSI, static noise margin, leakage power, read/write assist, 6T SRAM

I. INTRODUCTION

Static Random Access Memory constitutes the most widely employed on-chip memory technology in modern computing systems, providing high-speed, low-latency data storage for processor caches, register files, and AI accelerators (Evolution of SRAM Architectures, 2026). SRAM-based cache memory occupies more than 50% of chip space in contemporary microprocessors, making memory efficiency improvements directly impactful on overall system speed and energy consumption (Evolution of SRAM Architectures, 2026). The percentage die occupied by SRAM bit cells approaches 85–90% in many integrated circuits, underscoring the critical importance of efficient SRAM design (Mehra, 2018).

The relentless scaling of CMOS technology below 10 nm introduces severe challenges for conventional planar SRAM design. Process-induced unpredictability, decreased static noise margin (SNM), elevated leakage power, and instability at ultra-low supply voltages represent fundamental obstacles to continued scaling (Evolution of SRAM Architectures, 2026). Conventional MOSFETs struggle below 50 nm fabrication due to gate resistance-induced flicker noise, making 6T SRAMs under 45 nm unsuitable without architectural modification (Improving FinFET Device Parameters, 2025). These limitations have motivated extensive research into alternative device technologies and circuit topologies.

FinFET technology has emerged as the dominant solution for advanced-node SRAM design, offering superior electrostatic channel control through multi-gate architecture. Unlike planar CMOS, where the gate controls the channel from one side, FinFET employs a gate wrapped around a thin silicon “fin,” providing control from two or three sides (A

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Review on SRAM Memory Design Using FinFET Technology, 2025). This enhanced gate control enables superior suppression of short-channel effects, reduced subthreshold leakage, and improved device parameter variability tolerance. FinFET-based SRAM cells achieve up to 40% leakage reduction with 10–20% SNM improvement compared to planar counterparts (Evolution of SRAM Architectures, 2026).

This review synthesizes recent advances in FinFET-based low power SRAM cell design, drawing from a corpus of literature published between 2018 and 2026. The objectives are threefold: first, to provide a systematic taxonomy of SRAM cell architectures and their performance characteristics; second, to comparatively evaluate read/write assist techniques and optimization methodologies; and third, to identify emerging trends including dual-port architectures, machine learning-informed design, and combined read-write assist strategies.

II. FINFET DEVICE TECHNOLOGY FOR SRAM APPLICATIONS

2.1 FinFET Structure and Operating Modes

The FinFET structure comprises multiple perpendicular channels appearing similar to the “fin” of a fish, hence the nomenclature. It is classified as a Multi-Gate Device (MGD) built on a substrate, with the gate positioned on two, three, or four sides of the channel, forming a double-gate arrangement (A Review on SRAM Memory Design Using FinFET Technology, 2025). The source and drain regions form the “Fin” on the silicon surface. FinFET transistors can operate in two primary modes: Tied-Gate (TG) mode, where both front and back gates are connected to the same control signal, and Independent-Gate (IG) mode, where the gates are biased separately (A Review on SRAM Memory Design Using FinFET Technology, 2025).

In TG-mode, the design is simpler with shorted front and back gates, and short-channel effects are avoided due to greater gate-to-channel coupling. IG-FinFET combines P-type parallel FinFETs with N-type back gates tied to ground to achieve equivalent rise and fall delays. The ability to independently bias front and back gates in IG-mode enables dynamic threshold voltage control, a crucial characteristic for SRAM cells configured for low power consumption through back-gate regulation (Improving FinFET Device Parameters, 2025). FinFET devices ensure higher current density and faster switching times than CMOS technology while minimizing off-state leakage.

2.2 Advantages Over Planar CMOS for SRAM

FinFET technology addresses several fundamental limitations of planar CMOS at advanced technology nodes. The multi-gate structure provides superior electrostatic control, effectively suppressing short-channel effects that plague planar devices below 50 nm. Doping variability issues that degrade planar MOSFET performance are substantially mitigated in FinFET devices (Improving FinFET Device Parameters, 2025). Subthreshold leakage is dramatically reduced due to the improved gate control over the channel.

Comparative simulation studies at the 32 nm technology node demonstrate the superiority of FinFET over planar CMOS for SRAM applications. FinFET-based 6T SRAM cells show significantly lower average power, leakage power, and average delay compared to CMOS counterparts (The Simulation Waveform for 6-T SRAM Cell, 2010). The standby power or low leakage current property of FinFET makes it particularly appropriate for memory sub-system design (A Review on SRAM Memory Design Using FinFET Technology, 2025).

Table 1: FinFET vs. Planar CMOS Performance Comparison at 32 nm

Parameter	CMOS	FinFET	Improvement
Average Power (μW)	9.9131	Lower	Significant
Leakage Power (μW)	5.4711	Lower	Significant
Average Delay (ns)	6.1728	Lower	Significant

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SNM (mV)	113 (32 nm)	135.6 (16 nm)	10–20%

Source: The Simulation Waveform for 6-T SRAM Cell (2010); Evolution of SRAM Architectures (2026)

III. SRAM CELL ARCHITECTURES FOR LOW POWER DESIGN

3.1 Conventional 6T SRAM Cell

The conventional 6T SRAM cell consists of four NMOS transistors (two access transistors and two pull-down transistors) and two PMOS transistors (pull-up load transistors) configured as cross-coupled inverters (Design and Characterization of a Low-Leakage, 2025). The cell operates in three distinct states: hold (standby), read, and write. During hold mode, word-line is deactivated and the cross-coupled inverters maintain the stored data as long as power is supplied. During read, word-line activates the access transistors, allowing the stored value to be sensed on the bit-lines. During write, the access transistors are activated and the bit-lines force the new data into the cell.

The 6T cell faces fundamental stability trade-offs. Read stability requires a strong pull-down transistor and weak access transistor, while write ability requires a weak pull-up transistor and strong access transistor (Design and Characterization of a Low-Leakage, 2025). These conflicting requirements become increasingly difficult to satisfy at scaled supply voltages where process variations dominate. The conventional 6T SRAM cell provides poor write ability at downscaled supply voltages due to disturbance in node voltages (Design and Characterization of a Low-Leakage, 2025). These limitations motivate the exploration of alternative architectures with decoupled read/write paths.

3.2 7T and 8T SRAM Cells

The 7T and 8T SRAM architectures address the read stability limitations of the 6T cell by decoupling the read operation from the storage nodes. An additional transistor provides an isolated read path, preventing the read current from disturbing the stored data. This separation enables optimization of the pull-up/pull-down ratio for write ability without compromising read stability.

Comparative analysis of 7T SRAM implementations demonstrates the effectiveness of this approach. The proposed FinFET-based 7T design achieves propagation delay of 0.97 ns, power dissipation of 2.34 μW, and power-delay product of 2.01×10^{-15} W-s (Improving FinFET Device Parameters, 2025). The design maintains sufficient stability with write SNM of 357 mV and hold SNM of 261 mV, while delivering the fastest write access time of 0.17 ns and competitive read access time of 1.29 ns (Improving FinFET Device Parameters, 2025). These results demonstrate that the additional transistor overhead is justified by the stability and performance improvements achieved.

The 8T SRAM cell with separate read port has been extensively investigated for IoT applications where low leakage and high stability are paramount. The isolated read port enhances read stability while the negative bit-line write-aid circuit improves write capability (Design and Characterization of a Low-Leakage, 2025). Comparative analysis shows superior performance for the 8T cell compared to 6T in read, write, and hold modes, with increased static noise margins ensuring reliable bit-cell write ability.

3.3 9T Dual-Port SRAM Cell

The 9T dual-port SRAM cell represents an advanced architecture optimized for both power and stability in multi-port memory applications. A novel 9T dual-port SRAM based on 7 nm FinFET technology achieves power consumption reduction by removing the bit-line precharge circuit and introducing an innovative method to block leakage current during hold operation (Park et al., 2024).

The design achieves read static noise margin of approximately 310 mV and write static noise margin of 320 mV, with 55% improvement in read energy consumption and 69% improvement in write energy consumption compared to conventional designs (Park et al., 2024). The write SNM improvement is achieved by blocking the back-to-back loop during write operation using an additional M5 transistor. A virtual ground path is employed in the read path (M7–M9) to mitigate read current, enabling read operation without precharge circuit (Park et al., 2024). This architecture demonstrates that FinFET-based SRAM cells can be a promising solution for low-power, high-performance memory applications.

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Table 2: Performance Comparison of FinFET SRAM Cell Architectures

Architecture	Technology	Power (μW)	Delay (ns)	PDP (W-s)	SNM (mV)	Reference
6T SRAM	FinFET	0.985	0.99	2.05×10^{-15}	315 (W), 250 (H)	Improving FinFET (2025)
7T SRAM	FinFET	2.34	0.97	2.01×10^{-15}	357 (W), 261 (H)	Improving FinFET (2025)
8T AUF SRAM	16 nm FinFET	—	—	—	181.6	Fig (n.d.)
9T Dual-Port	7 nm FinFET	—	—	—	310 (R), 320 (W)	Park et al. (2024)
6T GeOI FinFET	GeOI FinFET	—	—	—	Improved with WLUD	Analysis of GeOI FinFET (n.d.)

W = Write SNM, H = Hold SNM, R = Read SNM

IV. READ AND WRITE ASSIST TECHNIQUES

4.1 Word-Line Under-Drive (WLUD) Read Assist

Word-line under-drive (WLUD) read assist is a technique that reduces the word-line voltage during read operations to weaken the access transistors, thereby improving read stability. This approach directly addresses the read disturb failure mechanism by reducing the gate-to-source voltage of access transistors.

Analysis of GeOI FinFET 6T SRAM cells with variation-tolerant WLUD read-assist demonstrates significant improvements. The WLUD read-assist is more efficient in improving read static noise margin and read V_MIN for fast-N slow-P corner GeOI FinFET SRAM cells compared to Silicon-On-Insulator counterparts (Analysis of GeOI FinFET, n.d.). GeOI FinFET SRAM cells with WLUD show less cell read access-time degradation compared to SOI counterparts at both 25 °C and 125 °C (Analysis of GeOI FinFET, n.d.). The temperature dependence of data retention time differs between GeOI and SOI FinFET SRAM cells, with important implications for assist technique selection.

4.2 Transient Voltage Collapse (TVC) Write Assist

Transient voltage collapse (TVC) write assist improves write ability by temporarily reducing the cell supply voltage during write operations, weakening the pull-up transistors and facilitating data flipping. With TVC write-assist, the write-ability and variation tolerance of both GeOI and SOI FinFET SRAM cells are improved (Analysis of GeOI FinFET, n.d.). The maximum TVC write-assist pulsewidth is constrained by data retention failure considerations. This constraint is smaller in GeOI FinFET SRAMs at 25 °C but becomes comparable at 125 °C compared with SOI FinFET SRAMs (Analysis of GeOI FinFET, n.d.). This temperature-dependent behavior must be carefully considered in assist technique design for reliable operation across the full temperature range.

4.3 Combined Read/Write Assist Techniques

While write failures initially limit minimum operating voltage (V_MIN), applying write assist alone introduces row and column half-select failures. Therefore, read and write assist must be combined to enable scaling V_MIN down to near/sub-threshold voltages (Yahya et al., 2015). Combined read/write assist techniques allow the 6T SRAM bit-cell to operate at significantly reduced V_MIN.

Research demonstrates that combining negative bit-line (BL) write assist with array VDD boosting for read assist is most effective for reducing array V_MIN and eliminating half-select failures (Yahya et al., 2015). The proposed combination

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results in the highest reduction in SRAM V_MIN, achieving 300 mV for FinFET technology and 600 mV for 130 nm CMOS (Yahya et al., 2015). Controlling the degree of applied assist based on chip corner allows further reductions in V_MIN for both FinFET and CMOS bit-cells (Yahya et al., 2015).

4.4 Negative Bit-Line (NBL) Write Assist

The negative bit-line write assist technique applies a negative voltage to the bit-lines during write operations, increasing the gate-to-source voltage of access transistors and thereby enhancing their driving capability (Design and Characterization of a Low-Leakage, 2025). This increased access transistor strength facilitates reliable write operations at reduced supply voltages.

However, the NBL technique increases bit-line capacitance through the boosted capacitor, which eventually increases access time (Design and Characterization of a Low-Leakage, 2025). This trade-off between write ability improvement and access time degradation must be carefully managed. Alternative write assist techniques including V_DD collapse and boosted word-line have been proposed, but each introduces its own limitations—V_DD collapse risks data loss during read or hold, while boosted word-line increases static power dissipation (Design and Characterization of a Low-Leakage, 2025).

Table 3: Read/Write Assist Techniques Comparison

Technique	Target	Mechanism	Key Benefit	Limitation
WLUD Read Assist	Read Stability	Reduce WL voltage	Improved RSNM and read V_MIN	Access-time degradation
TVC Write Assist	Write Ability	Reduce V_DD transiently	Improved write tolerance	Data retention constraint
NBL Write Assist	Write Ability	Negative BL voltage	Enhanced access strength	Increased BL capacitance
Combined Assist	Both	NBL + VDD boosting	V_MIN to 300 mV (FinFET)	Complex control required

V. OPTIMIZATION METHODOLOGIES FOR FINFET SRAM DESIGN

5.1 Metaheuristic Optimization Techniques

The complex, multi-dimensional trade-off space of FinFET SRAM design has motivated the application of metaheuristic optimization algorithms. Particle Swarm Optimization (PSO) and Whale Optimization Algorithm (WOA) have been integrated to optimize FinFET device parameters for improved SRAM performance. The WOA-based optimization outperforms genetic algorithms in terms of parameter optimization for predicting fin height and width based on transconductance, subthreshold swing, and other device metrics (Improving FinFET Device Parameters, 2025).

The integrated PSO-Whale methodology achieves substantial improvements in SRAM performance metrics. The proposed FinFET-based 6T SRAM design achieves power dissipation of 0.985 μW, write SNM of 315 mV, hold SNM of 250 mV, and PDP of 2.05×10^{-15} W-s, with propagation delay of 0.99 ns (Improving FinFET Device Parameters, 2025). These results demonstrate the effectiveness of metaheuristic optimization for navigating the complex FinFET SRAM design space.

5.2 Machine Learning-Informed Design Optimization

Machine learning techniques are increasingly applied to accelerate SRAM design optimization and parasitic analysis. A convolutional neural network (CNN)-informed NSGA-II methodology has been proposed for optimizing parasitic resistance in 7 nm FinFET 6T-SRAM cells (Optimization of 6T-SRAM Cell, 2025). The approach uses HSPICE

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simulation to generate datasets, trains multiple neural network models, and integrates the best-trained CNN into NSGA-II to obtain Pareto fronts with different resistance configurations (Optimization of 6T-SRAM Cell, 2025).

Parasitic resistance analysis reveals counterintuitive relationships between resistance values and performance metrics. Several types of parasitic resistance (Rbax, Roax, and Ropd) exhibit inverse relationships with power consumption—as resistance increases, power decreases (Optimization of 6T-SRAM Cell, 2025). These phenomena arise from multiple physical mechanisms, including prolonged charging and discharging times affecting transient behavior. The CNN-informed optimization framework enables rapid evaluation of design alternatives and identification of Pareto-optimal configurations.

5.3 Multi-Fin Configuration Optimization

The fin configuration represents a critical design parameter for FinFET SRAM cells. Strategic multi-fin configuration analysis at the 14 nm technology node demonstrates significant voltage-dependent stability improvements. Static noise margin increases from 190 mV to 280 mV across a VDD range of 0.5 V to 0.8 V, yielding a 47% improvement in noise tolerance capabilities (Design and Stability Optimization, 2025).

The cell maintains robust operation at VDD = 0.5 V with SNM of 190 mV and access times below 7 ps, validating its potential for low-power applications (Design and Stability Optimization, 2025). Access time characterization indicates differential sensitivity between read and write operations with respect to supply voltage modulation. These results substantiate the efficacy of FinFET technology in addressing the stability-performance trade-offs inherent in advanced node SRAM design.

VI. PERFORMANCE ANALYSIS AND COMPARATIVE EVALUATION

6.1 Technology Node Impact

Technology node selection fundamentally constrains achievable SRAM performance. Comparative analysis across 7 nm, 10 nm, 14 nm, 16 nm, and 20 nm FinFET technology nodes reveals consistent trends (Mehra, 2018). The 7 nm FinFET SRAM cells perform better in all aspects and demonstrate the most resilience under variable temperature, followed by cells at 10 nm, 14 nm, 16 nm, and 20 nm nodes (Mehra, 2018). This improvement stems from enhanced electrostatic control and reduced parasitics at advanced nodes.

Power gating techniques applied to FinFET SRAM cells reveal trade-offs between power dissipation and performance. Gated versions of SRAM cells perform poorly compared to standard counterparts but have improved PDP and lower power dissipation (Mehra, 2018). This suggests that power gating is most appropriate for applications where standby power dominates over active performance requirements.

6.2 Comparative Analysis with Alternative Technologies

While FinFET represents the dominant technology for advanced-node SRAM, emerging alternatives including CNTFET and TFET offer potential advantages for specific applications. CNTFET-based SRAM achieves static noise margin of 350.12 mV for 6T configuration and 462.21 mV for modified 10T at 32 nm technology, substantially exceeding FinFET SNM values at comparable nodes (Fig, n.d.). CNTFET and TFET architectures enable steady sub-0.3 V operation with over 60% standby-power reduction compared to conventional designs (Evolution of SRAM Architectures, 2026).

However, these emerging technologies face manufacturing maturity challenges. Planar variability in CNT diameter and doping, precise CNT placement, contact formation, interconnect parasitics, and thermal management are critical factors for reliable and scalable memory implementations (Fig, n.d.). FinFET technology, by contrast, benefits from established manufacturing infrastructure and design ecosystems, making it the pragmatic choice for near-term production.

6.3 Design Trade-off Analysis

The selection of an appropriate FinFET SRAM design involves navigating a complex trade-off space. Figure 1 presents a qualitative trade-off analysis across key dimensions.

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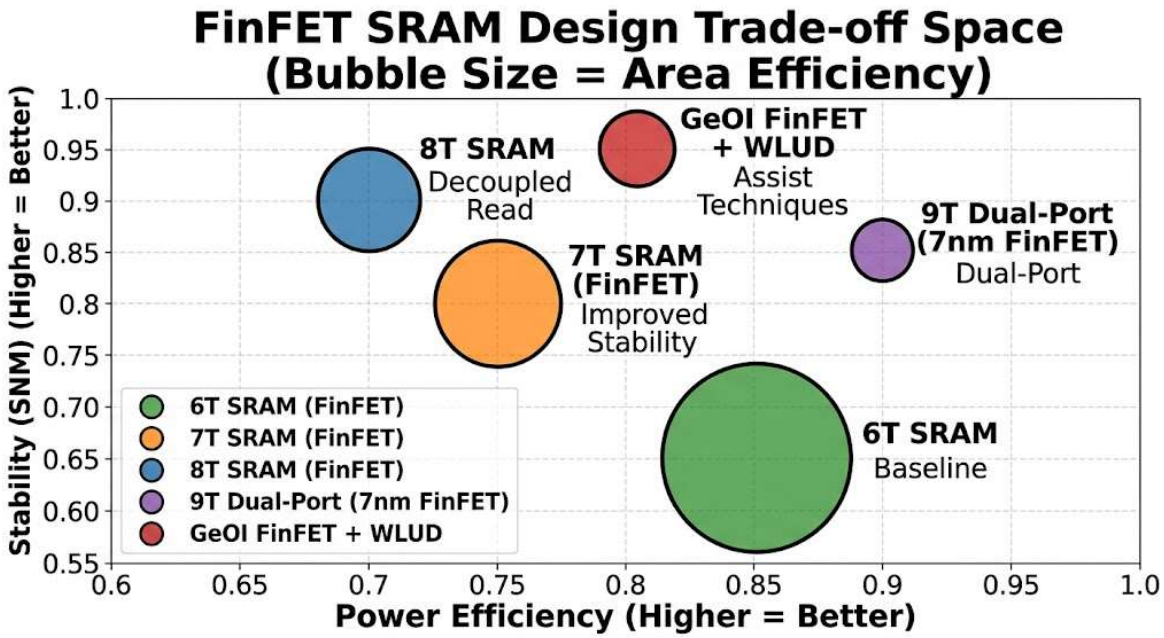

Figure 1: Design Trade-off Space for FinFET SRAM Architectures

The trade-off analysis reveals distinct design regions. The 6T FinFET SRAM achieves the highest area efficiency but with moderate stability, making it suitable for high-density cache applications. The 7T and 8T architectures improve stability at the cost of increased area, positioning them for applications where reliability is paramount. The 9T dual-port design achieves an excellent balance of power efficiency and stability, making it suitable for multi-port register files. GeOI FinFET with WLUD assist achieves the highest stability through assist techniques, appropriate for low-voltage operation.

VI. CHALLENGES AND FUTURE DIRECTIONS

7.1 Technology Scaling Challenges

Continued scaling below 7 nm presents fundamental challenges for FinFET SRAM design. As semiconductor scaling advances beyond 20 nm, maintaining robust SRAM operation becomes increasingly challenging due to enhanced short-channel effects and reduced noise margins (Design and Stability Optimization, 2025). Process variations become more pronounced, necessitating robust design methodologies and statistical analysis.

The evolution beyond FinFET toward CFET (Complementary FET), TFET, and CNFET technologies represents the next frontier in SRAM design (Evolution of SRAM Architectures, 2026). CFET-based SRAM resolves problems of scaling and efficiency by stacking complementary transistors vertically, enabling continued density scaling beyond FinFET limits. However, these technologies face significant manufacturing maturity challenges that must be overcome before production deployment.

7.2 Emerging Research Directions

Several promising research directions emerge from the surveyed literature. Advanced topologies including spintronic MTJ-based non-volatile SRAM, hybrid TFET-MOSFET 12T, Schmitt-trigger 8T, and gated-logic 10T demonstrate improved energy efficiency and robustness (Evolution of SRAM Architectures, 2026). These hybrid approaches combine the strengths of multiple device technologies to address the fundamental trade-offs in SRAM design.

Machine learning-informed design methodologies represent a particularly promising avenue for addressing the complexity of modern SRAM design. The CNN-informed NSGA-II framework demonstrates the potential of data-driven approaches to navigate the multi-dimensional trade-off space more effectively than manual optimization (Optimization

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of 6T-SRAM Cell, 2025). Future research should focus on expanding these techniques to encompass full-system considerations including array-level optimization, thermal management, and reliability analysis.

The integration of FinFET SRAM with emerging computing paradigms including compute-in-memory (CiM) and neuromorphic architectures presents both opportunities and challenges. The unique characteristics of FinFET devices—including independent gate control and back-gate biasing—may enable novel circuit topologies optimized for these applications.

VIII. CONCLUSION

This review has provided a comprehensive examination of FinFET-based low power SRAM cell design, synthesizing recent advances across architectures, assist techniques, and optimization methodologies. Conventional planar CMOS SRAM faces fundamental limitations below 10 nm including excessive leakage, degraded SNM, and process variability sensitivity (Evolution of SRAM Architectures, 2026). FinFET technology addresses these challenges through superior electrostatic control, achieving up to 40% leakage reduction with 10–20% SNM improvement compared to planar counterparts.

Architectural innovation complements device technology advancement. The 7T and 8T SRAM cells with decoupled read paths achieve superior stability by isolating read operations from storage nodes, with demonstrated write SNM of 357 mV and hold SNM of 261 mV at competitive power dissipation (Improving FinFET Device Parameters, 2025). The 9T dual-port architecture achieves 55% and 69% improvements in read and write energy consumption respectively through removal of precharge circuits and back-to-back loop blocking during write (Park et al., 2024).

Read/write assist techniques enable reliable operation at reduced supply voltages. Combined negative bit-line write assist with array VDD boosting read assist achieves V_MIN of 300 mV for FinFET technology (Yahya et al., 2015). WLUD read assist and TVC write assist provide complementary improvements for GeOI FinFET SRAM cells with temperature-dependent characteristics (Analysis of GeOI FinFET, n.d.).

Optimization methodologies including metaheuristic algorithms and machine learning-informed design frameworks enable systematic exploration of the complex SRAM design space. The integrated PSO-Whale optimization achieves power dissipation of 0.985 μW and PDP of 2.05×10^{-15} W-s for 6T SRAM (Improving FinFET Device Parameters, 2025). CNN-informed NSGA-II enables rapid evaluation of parasitic resistance configurations for Pareto-optimal design selection (Optimization of 6T-SRAM Cell, 2025).

Future research should focus on emerging device technologies including CFET, TFET, and CNTFET for continued scaling beyond FinFET limits (Evolution of SRAM Architectures, 2026). Machine learning-informed design methodologies represent a particularly promising avenue for addressing the growing complexity of SRAM design. The integration of FinFET SRAM with compute-in-memory architectures and neuromorphic computing paradigms presents opportunities for novel circuit topologies optimized for emerging applications.

REFERENCES

1. A review on SRAM memory design using FinFET technology. (2025). *IGI Global Scientific Publishing*. Retrieved from https://www.igi-global.com/gateway/article/full-text-html/302665
2. Analysis of GeOI FinFET 6T SRAM cells with variation-tolerant WLUD read-assist and TVC write-assist. (n.d.). *INFONA*. Retrieved from https://www.infona.pl/resource/bwmeta1.element.ieee-art-000007070691
3. Design and characterization of a low-leakage, high-stability SRAM cell for IoT applications. (2025). *Indian Journal of Engineering and Materials Sciences*, *31*(5). https://doi.org/10.56042/ijems.v31i5.6683
4. Design and stability optimization of 6T FinFET SRAM cell using strategic multi-fin configuration. (2025). *2025 IEEE International Conference on Emerging Trends in Engineering and Technology (ICETET)*. https://doi.org/10.1109/ICETET

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ISSN: 2581-9429
Volume 6, Issue 1, September 2026
Impact Factor: 8.2

5. Evolution of SRAM architectures: From CMOS, FinFET to CNTFET and beyond for next-generation computing systems. (2026). *2026 IEEE International Conference on Recent Trends in Engineering and Technology (ICRTET)*. https://doi.org/10.1109/ICRTET
6. Fig: Table 4 SNM comparison between different technologies SRAM. (n.d.). *Nature Scientific Reports*. Retrieved from https://www.nature.com/articles/s41598-026-47254-7
7. Improving FinFET device parameters through an integrated method of particle swarm and whale optimization techniques. (2025). *IET Circuits, Devices & Systems*, *19*(1). https://doi.org/10.1049/cds2/7035085
8. Mehra, S. S. (2018). *Performance analysis of FinFET based SRAM at nano-scaled technology nodes* [Master's thesis, Thapar Institute of Engineering and Technology]. Thapar University Repository. http://hdl.handle.net/10266/5226
9. Optimization of 6T-SRAM cell based on CNN-informed NSGA-II with consideration of parasitic resistance. (2025). *Electronics*, *14*(20), 4002. https://doi.org/10.3390/electronics14204002
10. Park, J.-Y., Choi, S.-H., & Song, H.-J. (2024). Design of a 9T dual-port SRAM based on 7nm FinFET: Power optimization and stability enhancement. *Journal of the Korean Institute of Electrical and Electronic Material Engineers*, *37*(6). https://doi.org/10.5370/JKIEEME.2024.37.6.XXX
11. The simulation waveform for 6-T SRAM cell in CMOS, FinFET and CNTFET. (2010). *International Journal of Computer Applications*, *70*(21). Retrieved from https://research.ijcaonline.org
12. Yahya, F., Patel, H., Calhoun, B., & Chandra, V. (2015). Combined SRAM read/write assist techniques for near/sub-threshold voltage operation. *2015 6th Asia Symposium on Quality Electronic Design (ASQED)*. Retrieved from http://www.asqed.com/English/Archives/2015/Technical_Papers/174.html