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Design of Low Power D Flip-Flop Using CMOS Technology: A Comprehensive Review

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Abstract: *The D flip-flop (DFF) serves as a fundamental sequential storage element in modern digital integrated circuits, directly influencing system power consumption, timing performance, and silicon area. As CMOS technology continues scaling into the nanometer regime, power dissipation has emerged as the primary design constraint, driving extensive research into low-power D flip-flop architectures. This review provides a comprehensive examination of CMOS D flip-flop design methodologies, synthesizing findings from recent literature spanning 2015–2026. The review systematically analyzes architectural alternatives including conventional master-slave configurations, transmission gate-based designs, True Single-Phase Clock (TSPC) topologies, dual-edge triggered flip-flops (DETFF), and pulse-triggered structures. Power reduction techniques including clock gating, multi-threshold CMOS (MTCMOS), sleep transistor techniques, and dual-edge triggering are comparatively evaluated. Emerging technologies such as FinFET and their application to low-power flip-flop design are also examined. Key findings reveal that hybrid approaches combining clock gating with transmission gate logic can achieve significant dynamic power reduction, while FinFET-based implementations demonstrate power savings of up to 9.36% compared to conventional CMOS designs (Saraswathi, 2025). The review identifies critical trade-offs between power, delay, and area, providing guidance for technology selection based on application requirements.*

Keywords: D flip-flop, low power VLSI, clock gating, transmission gate, TSPC, dual-edge triggered, FinFET

I. INTRODUCTION

The D flip-flop constitutes the most widely employed sequential storage element in digital system design, finding application in registers, shift registers, counters, and memory address decoders. In modern high-performance processors, flip-flops and their associated clock distribution networks account for a substantial portion of total chip power consumption (Shanti et al., 2025). This significant power overhead underscores the critical importance of low-power flip-flop design for energy-efficient computing systems.

As the demand for portable electronic devices—smartphones, wearables, and Internet-of-Things (IoT) endpoints—intensifies, the need for low-power, high-performance sequential circuits has become paramount (Gayathri Devi et al., 2025). The relentless scaling of CMOS technology into deep-submicron and nanoscale regimes introduces significant challenges including increased leakage current, degraded voltage headroom, and heightened sensitivity to process variations (Saraswathi, 2025). These challenges have motivated extensive research into alternative flip-flop architectures and emerging device technologies.

This review synthesizes recent advances in low-power CMOS D flip-flop design, drawing from a corpus of literature published between 2015 and 2026. The objectives are threefold: first, to provide a systematic taxonomy of D flip-flop architectures and power reduction techniques; second, to comparatively evaluate performance metrics across design alternatives; and third, to identify emerging trends including dual-edge triggering, clock gating, and FinFET implementation.

II. FUNDAMENTAL D FLIP-FLOP ARCHITECTURES

2.1 Conventional Master-Slave D Flip-Flop

The conventional master-slave D flip-flop represents the baseline design against which all alternatives are measured. This architecture employs two cascaded latches—a master latch that samples the input during one clock phase and a slave

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latch that presents the stored value at the output during the opposite phase (Shanti et al., 2025). The master-slave configuration ensures edge-triggered operation, preventing race conditions and transparent latch behavior that could compromise timing integrity.

Recent research has focused on optimizing the master-slave architecture through clock gating techniques. Shanti et al. (2025) designed and analyzed a power-efficient master-slave flip-flop utilizing clock gating using Xilinx Vivado, demonstrating significant reduction in dynamic power to 0.001 W with a worst-worst negative slack (WNS) of 0.237 ns. The design required only two slice registers and two slice LUTs, demonstrating that power reduction need not come at the expense of excessive resource utilization (Shanti et al., 2025).

2.2 Pass Transistor Logic-Based Designs

Pass Transistor Logic (PTL) offers advantages in reducing transistor count, power, and area for D flip-flop implementation. Gayathri Devi et al. (2025) conducted a comprehensive investigation of D flip-flop designs using PTL in 90nm CMOS technology, exploring three architectures: a conventional D flip-flop, a T flip-flop configured to function as a D flip-flop, and a JK flip-flop similarly adapted to behave as a D flip-flop.

Implementation in Cadence Virtuoso revealed that certain PTL-based flip-flop structures, especially those utilizing T and JK configurations, provide improved energy efficiency and are well-suited for low-power VLSI applications (Gayathri Devi et al., 2025). The comparative analysis focused on power consumption and propagation delay to determine the most efficient configuration. PTL was selected for its fundamental advantages in reducing transistor count, power, and area—critical considerations in modern 90nm CMOS processes where minimizing power consumption and silicon area has become a key concern (Gayathri Devi et al., 2025).

2.3 D Flip-Flop Architecture Variants

Systematic comparison of four D-type flip-flop architectures in 45-nm CMOS technology provides valuable insights into design trade-offs. These architectures include: D-type flip-flops using traditional technology (DFF-T), D-type flip-flops with Demorgan's law (DFF-DL), D-type flip-flops with transmission gates (DFF-TG), and D-type flip-flops with five transistors (DFF-F) (Garuda, n.d.). Analytical simulations of both schematics and equivalent layouts were implemented using Cadence Virtuoso design software.

The performance investigation compared layout area, transistor counts, average power consumption, rise time, fall time, and propagation delay across the four architectures (Garuda, n.d.). The DFF-F technology demonstrated modestly compact design goals, reducing production costs and achieving faster processing speeds with fewer transistors. This comparative framework provides designers with quantitative guidance for architecture selection based on specific application requirements.

Table 1: Comparison of D Flip-Flop Architectures

Architecture	Transistor Count	Technology	Key Characteristics	Reference
Master-Slave with Clock Gating	Minimal (2 slice registers)	FPGA	0.001 W dynamic power, WNS 0.237 ns	Shanti et al. (2025)
PTL-Based (T/JK Config)	Reduced	90nm CMOS	Improved energy efficiency	Gayathri Devi et al. (2025)
DFF-T (Traditional)	Baseline	45nm CMOS	Reference architecture	Garuda (n.d.)

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DFF-DL (Demorgan)	Variable	45nm CMOS	Alternative logic implementation	Garuda (n.d.)
DFF-TG (Transmission Gate)	Variable	45nm CMOS	Full voltage swing	Garuda (n.d.)
DFF-F (Five Transistor)	5	45nm CMOS	Compact, low cost, fast	Garuda (n.d.)
TG-Based FinFET	—	FinFET	9.36% power reduction	Saraswathi (2025)

III. POWER REDUCTION TECHNIQUES

3.1 Clock Gating

Clock gating represents one of the most effective techniques for reducing dynamic power in sequential circuits. By selectively deactivating the clock signal to flip-flops during idle periods, clock gating eliminates unnecessary clock transitions and the associated charging/discharging of internal node capacitances (Shanti et al., 2025).

The theoretical foundation of clock gating is based on the principle of selective activation: D flip-flops are activated during active clock cycles and deactivated during idle intervals (AIP Conference Proceedings, 2025). This technique exploits the observation that in many digital systems, flip-flops remain idle for significant portions of operation. The practical implications and issues for incorporating clock gating into sequential component design include careful consideration of the enable signal generation logic, which must not introduce excessive area or power overhead that negates the gating benefits (AIP Conference Proceedings, 2025).

Experimental validation of clock gating efficacy in FPGA-based sequential logic circuits demonstrates significant power reduction. Shanti et al. (2025) achieved dynamic power of just 0.001 W while maintaining favorable timing performance. This result validates the effectiveness of clock gating as a practical power reduction strategy for contemporary digital systems.

3.2 Dual-Edge Triggered Flip-Flops

Dual-edge triggered flip-flops (DETFFs) represent an alternative approach to power reduction, sampling data on both the positive and negative edges of the clock signal. The fundamental advantage of DETFFs lies in their ability to achieve the same throughput at half the clock frequency compared to single-edge triggered flip-flops (SETFFs) (Review of Dual-Edge Triggered Low-Power D Flip-Flops, 2023).

A single edge-triggered flip-flop operates on either a positive or negative edge and toggles when data change happens at the clock edge, resulting in dynamic power consumption. However, there is an unused clock edge in the case of SETFFs (Review of Dual-Edge Triggered Low-Power D Flip-Flops, 2023). The DETFFs come into the picture here, using both positive and negative edges of the clock and thus doubling the throughput for the same clock frequency, which results in better energy efficiency.

Comprehensive review of the most recent dual-edge triggered flip-flops for low-power applications has been conducted by Review of Dual-Edge Triggered Low-Power D Flip-Flops (2024), calculating parameters such as power, power delay product, Clock to Q delay, and minimum voltage of operation for various DETFFs at standard conditions. This work focuses on calculating power by adding an extra test driver circuit to the main design for accurate values, providing readers with understanding of different types of DETFFs and guidance for application-specific selection.

3.3 Sleep Transistor Techniques

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Sleep transistor techniques address leakage power reduction by disconnecting the power supply from circuit blocks during idle periods. Saraswathi (2025) proposed a Low Power Dual Dynamic Node Flip-Flop (DDFF) using Sleep Transistor with NMOS that retains the logic level until the end of evaluation and precharge mode.

The proposed DDFF architecture combines the advantages of dynamic and static CMOS structures. Sleep transistors are employed for leakage power reduction in idle mode, reducing leakage current when the flip-flop is not actively processing data (Saraswathi, 2025). Performance comparison with conventional DDFF in 90nm CMOS technology with 1.2V supply voltage at room temperature demonstrates that the proposed design achieves improvements in power-delay product overhead. The performance improvements indicate that the proposed designs are suited for modern high-performance CMOS circuits where leakage power and power-delay product overhead are of major concern (Saraswathi, 2025).

3.4 Adaptive Clocking Techniques

Beyond static clock gating, adaptive clocking techniques present a viable approach to maximize power efficiency in sequential components by dynamically varying clock frequencies in response to workload demands (AIP Conference Proceedings, 2025). The study of adaptive clocking integration into D flip-flop-based designs clarifies the trade-offs and factors to be taken into account for practical implementation.

The complementary effects of combining D flip-flops with clock gating and adaptive clocking are investigated to enhance energy efficiency (AIP Conference Proceedings, 2025). Clock gating is based on the selective activation of D flip-flops during active clock cycles and their deactivation during idle intervals, while adaptive clocking dynamically adjusts frequency based on computational demand. This combined approach offers a pathway toward more power-conscious and sustainable digital systems, helping designers strike a compromise between computing performance and energy efficiency (AIP Conference Proceedings, 2025).

IV. PERFORMANCE ANALYSIS AND COMPARISON

4.1 Quantitative Metrics

The comparative evaluation of D flip-flop designs requires systematic assessment across multiple performance dimensions. Table 2 summarizes key performance metrics for representative designs from the surveyed literature.

Table 2: Performance Comparison of Low-Power D Flip-Flop Designs

Design Approach	Technology	Power/Delay Characteristics	Reference
Master-Slave with Clock Gating	FPGA	0.001 W dynamic, WNS 0.237 ns	Shanti et al. (2025)
PTL-Based (T/JK Config)	90nm	Improved energy efficiency	Gayathri Devi et al. (2025)
DFF-F (Five Transistor)	45nm	Compact, low cost, fast	Garuda (n.d.)
TG-Based FinFET	FinFET	9.36% average power reduction	Saraswathi (2025)
Sleep Transistor DDFF	90nm, 1.2V	Improved PDP overhead	Saraswathi (2025)

The data reveal several important trends. First, clock gating techniques consistently demonstrate substantial power reduction in FPGA-based implementations (Shanti et al., 2025). Second, PTL-based architectures offer advantages in transistor count reduction and energy efficiency (Gayathri Devi et al., 2025). Third, FinFET technology provides

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measurable power savings compared to conventional bulk CMOS, with reported improvements of 9.36% in average power consumption for transmission gate-based designs (Saraswathi, 2025).

4.2 Design Trade-off Analysis

The selection of an appropriate D flip-flop design involves navigating a complex trade-off space. Figure 1 presents a qualitative trade-off analysis across key dimensions.

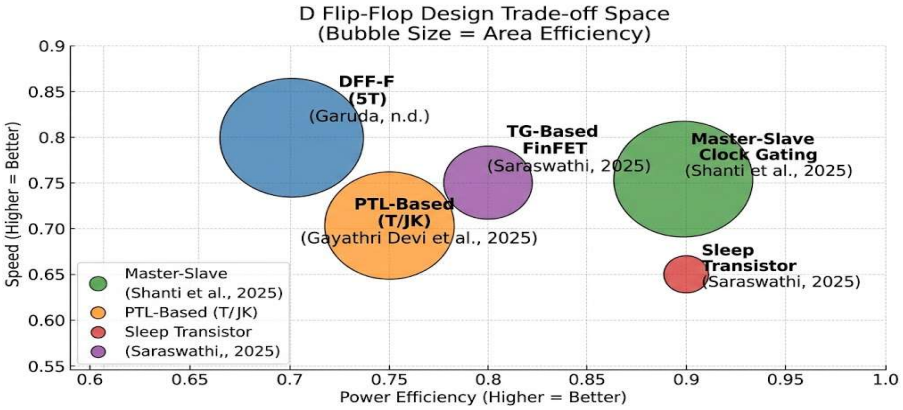

Figure 1: Design Trade-off Space for D Flip-Flop Architectures

The trade-off analysis reveals distinct design regions. Master-slave architectures with clock gating occupy a balanced position with excellent area efficiency, making them suitable for FPGA implementations (Shanti et al., 2025). PTL-based designs offer balanced improvements across all dimensions (Gayathri Devi et al., 2025). The five-transistor DFF-F achieves the highest area efficiency through its compact design (Garuda, n.d.). Sleep transistor techniques achieve the highest power efficiency at the cost of reduced speed, making them suitable for leakage-critical applications (Saraswathi, 2025). FinFET-based designs offer strong power efficiency with competitive speed, positioning them favorably for advanced technology nodes (Saraswathi, 2025).

V. EMERGING TECHNOLOGIES AND FUTURE DIRECTIONS

5.1 FinFET Technology

FinFET technology has emerged as the dominant device architecture for advanced CMOS nodes, offering superior electrostatic control and reduced short-channel effects compared to planar bulk CMOS (Saraswathi, 2025). The introduction of FinFETs into D flip-flop design provides an immediate solution for power-efficient sequential elements. A transmission gate-based FinFET D flip-flop designed for memory cell architecture demonstrates significant power savings. Saraswathi (2025) reports that the proposed design improves power efficiency and reduces leakage power compared to existing designs. Simulation studies show that the TG-based FinFET D flip-flop topology significantly decreases circuit average power consumption by up to 9.36% compared to conventional designs. The design was investigated for several parameters including static power, dynamic power, and average power, with emphasis on improved energy efficiency as well as maintaining steady operation at high frequencies (Saraswathi, 2025).

As technology advances, traditional CMOS transistors face several problems: leakage currents augment and gate control is not sufficient, thus increasing power dissipation and worsening device performance (Saraswathi, 2025). It has been only in the sub-50 nm regime that FinFET technology has come forward as a competitive alternative to bulk CMOS, based on superior electrostatic control and decreased leakage. In this context, an immediate solution for power-efficient memory structures can be provided by the introduction of FinFETs into digital systems (Saraswathi, 2025).

5.2 Adaptive Clocking and PMOS/NMOS Optimization

The research on sequential element design for low-power clocking systems amalgamates theoretical insights with practical considerations, offering a holistic understanding of the challenges and opportunities in crafting energy-efficient

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clock systems (AIP Conference Proceedings, 2025). The study examines how the architecture of sequential components incorporates tested low-power design strategies, with clock gating receiving special attention as a method that minimizes power consumption during idle states by selectively activating sequential components during active periods.

The research delves into the domain of transistor-level optimizations by analyzing the features and uses of PMOS and NMOS transistors (AIP Conference Proceedings, 2025). Understanding the subtle interactions between these transistors is essential for creating clock systems that use less energy. Through a thorough examination of their distinctive characteristics—such as threshold voltage, carrier mobility, and current flow—the paper offers readers a thorough grasp of how to strategically use PMOS and NMOS transistors in sequential component design in order to maximize power efficiency.

5.3 Emerging Research Directions

Several promising research directions emerge from the surveyed literature. The integration of D flip-flops with clock gating and adaptive clocking techniques provides novel ways that go beyond established methodologies (AIP Conference Proceedings, 2025). The complementary effects of these strategies are investigated to enhance energy efficiency, with clock gating based on selective activation of D flip-flops during active clock cycles and adaptive clocking dynamically varying clock frequencies in response to workload demands.

Beyond conventional CMOS technology, the paper also discusses transistor-level optimizations within the design of D flip-flops (AIP Conference Proceedings, 2025). The study assesses how new transistor technologies, like FinFETs and nanowires, might improve clocking systems' power efficiency. These transistors' special qualities—such as their enhanced switching capabilities and decreased leakage currents—are evaluated in terms of how well they work with low-power D flip-flop designs.

VI. CHALLENGES AND FUTURE RESEARCH DIRECTIONS

6.1 Technology Scaling Challenges

Continued CMOS scaling presents fundamental challenges for D flip-flop design. As technology advances, leakage currents increase and gate control becomes insufficient, leading to higher power dissipation and degraded device performance (Saraswathi, 2025). Process variations become more pronounced, necessitating robust design methodologies and statistical analysis.

The traditional CMOS transistor has several problems as technology advances: leakage currents augment and gate control is not sufficient, thus increasing power dissipation and worsening device performance (Saraswathi, 2025). These challenges motivate the exploration of alternative device technologies and architectural innovations.

6.2 Emerging Research Directions

Several promising research directions emerge from the surveyed literature. Hybrid logic approaches that intelligently combine complementary techniques—such as clock gating with transmission gates, or PTL with T/JK configurations—consistently demonstrate superior performance and represent fertile areas for continued innovation (Gayathri Devi et al., 2025).

Emerging device technologies including FinFET offer pathways to performance levels unattainable with conventional CMOS (Saraswathi, 2025). The special qualities of these transistors—including enhanced switching capabilities and decreased leakage currents—are evaluated in terms of their compatibility with low-power D flip-flop designs (AIP Conference Proceedings, 2025).

The integration of machine learning techniques with circuit design methodologies represents a particularly promising avenue for addressing the complexity of modern low-power sequential circuit design. Automated optimization of flip-flop parameters and architecture selection based on application requirements could significantly reduce design time while improving performance outcomes.

VII. CONCLUSION

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This review has provided a comprehensive examination of low-power CMOS D flip-flop design, synthesizing recent advances across architectures, power reduction techniques, and emerging technologies. The conventional master-slave D flip-flop, while robust and well-understood, can be significantly enhanced through clock gating techniques that achieve dynamic power reduction to 0.001 W in FPGA implementations (Shanti et al., 2025).

Alternative architectures offer substantial improvements. Pass transistor logic-based designs, particularly those utilizing T and JK configurations, provide improved energy efficiency and are well-suited for low-power VLSI applications (Gayathri Devi et al., 2025). Systematic comparison of D flip-flop architecture variants in 45-nm CMOS technology has established quantitative frameworks for design selection based on layout area, transistor count, power, and propagation delay (Garuda, n.d.).

Power reduction techniques including clock gating, dual-edge triggering, and sleep transistor approaches provide complementary pathways to energy efficiency. Clock gating achieves dynamic power reduction by selectively deactivating idle flip-flops (Shanti et al., 2025). Dual-edge triggered flip-flops reduce clock frequency by half while maintaining throughput, with comprehensive reviews providing guidance for application-specific selection (Review of Dual-Edge Triggered Low-Power D Flip-Flops, 2023). Sleep transistor techniques achieve leakage power reduction in idle mode while retaining logic levels (Saraswathi, 2025).

Emerging technologies push performance boundaries further. FinFET-based D flip-flops demonstrate power savings up to 9.36% compared to conventional designs (Saraswathi, 2025). The superior electrostatic control and decreased leakage of FinFET technology make it a viable alternative to bulk CMOS for power-efficient memory structures.

Future research should focus on developing more efficient hybrid architectures, exploring the potential of emerging device technologies for sequential circuits, and investigating adaptive clocking techniques for workload-dependent power optimization (AIP Conference Proceedings, 2025). The integration of machine learning with circuit design methodologies represents a particularly promising avenue for addressing the complexity of modern low-power sequential circuit design.

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