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Design and Analysis of a Low-Power Hybrid 10-Transistor CMOS Full Adder in 180 nm Technology

Soniya Patel[1] , Deepali Sahu[2], Madhu Vishwakarma[3]
Adina Institute of Science & Technology, Sagar, MP[1-3]

Abstract: *This paper presents the design, comparative analysis, and simulation of a low-power hybrid 10-transistor (10T) CMOS full adder realized in a 180 nm technology with a 1.8 V supply. The proposed cell combines a six-transistor XOR/XNOR module with a two-transistor pass-transistor carry network and a two-transistor transmission-gate sum multiplexer, achieving full output swing and balanced rise/fall behaviour while eliminating the stacked contention paths of conventional static CMOS. An exhaustive simulation campaign over the eight-input truth-table space at 100 MHz with a 10 fF load demonstrates that the proposed adder consumes 2.67 µW, exhibits propagation delays of 322.7 ps and 207.5 ps for the sum and carry outputs, and attains a power-delay product of 861.6 fJ. Relative to the conventional 28-transistor static CMOS adder, these figures correspond to savings of 63.5% in power, 65.1% in sum delay, and 87.3% in power-delay product, while transistor count falls from 28 to 10. A supply-voltage sweep from 1.2 V to 2.0 V confirms correct functionality down to 1.2 V with quadratic dynamic-power scaling, and the pass-transistor critical path remains functional across process corners. The findings indicate that topology-driven minimisation of switched capacitance and internal node count, rather than device-level tuning alone, is the dominant lever for energy-efficient arithmetic in portable and embedded applications.*

Keywords: CMOS full adder, low-power VLSI, hybrid logic style, pass-transistor logic, power-delay product, arithmetic circuits.

I. INTRODUCTION

The one-bit full adder is the atomic computational element of virtually every digital arithmetic block, including ripple-carry and carry-lookahead adders, multipliers, dividers, and multiply-accumulate units, and its electrical characteristics therefore propagate directly to the power, speed, and area of entire datapaths (Weste & Harris, 2011; Rabaey et al., 2003). In battery-powered and energy-harvesting systems, the arithmetic core can account for a substantial fraction of the total energy budget, which has motivated three decades of research into adder cells that reduce transistor count, switched capacitance, and internal voltage swing without sacrificing robustness (Alioto & Palumbo, 2002; Chang et al., 2005).

The conventional 28-transistor (28T) static CMOS full adder remains the robustness benchmark because its complementary pull-up and pull-down networks guarantee full swing, ratioless operation, and high noise margins (Kang & Leblebici, 2003). However, its large device count and high internal node capacitance translate into excessive dynamic power at moderate frequencies. Complementary pass-transistor logic (CPL) and transmission-function adders (TFA) reduce the count to 14 transistors and improve speed, but at the cost of reduced output levels and the need for output buffers (Alioto & Palumbo, 2002). More aggressive cells employ ten or fewer transistors; these exploit the algebraic identity that the sum output is a multiplexer of the XOR and XNOR functions controlled by the carry input, while the carry output can be generated with a compact pass-transistor network (Radhakrishnan, 2001; Chang et al., 2005). A recognised weakness of many minimal cells is the threshold loss of pass-transistor nodes and the resulting sensitivity to supply and corner variation, which motivated improved XOR/XNOR formulations that restore full swing (Naseri & Timarchi, 2018).

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Building on this lineage, the present work designs and systematically analyses a hybrid 10T full adder whose distinguishing feature is the integration of a full-swing six-transistor XOR/XNOR module with a ratioless pass-transistor carry path, delivering the low power of minimal transistor-count topologies with the signal integrity normally associated with static CMOS. The contribution is threefold: (i) a complete transistor-level design and sizing strategy for the proposed cell; (ii) an apples-to-apples comparative study against 28T, 14T, and conventional 10T realisations using identical device models, loads, and input statistics; and (iii) a findings-oriented analysis spanning power, delay, power-delay product (PDP), supply-voltage scalability, and functional robustness. Section 2 details the circuit methodology, Section 3 reports and discusses the results, and Section 4 concludes.

II. MATERIALS AND METHODS

2.1 Full-Adder Fundamentals

A full adder accepts three binary inputs—augend A, addend B, and carry-in C_in—and produces a sum S and carry-out C_out, as summarised in the truth table of Figure 1. The Boolean expressions $S = A \oplus B \oplus C_{in}$ and $C_{out} = AB + C_{in}(A \oplus B)$ reveal the structural opportunity exploited by all low-power topologies: the carry is a simple function of the XOR of A and B, and the sum is a two-to-one multiplexer that selects between XNOR(A, B) and XOR(A, B) under control of C_in (Rabaey et al., 2003). Sharing the XOR/XNOR computation between both outputs amortises one logic stage and removes the deep series stacks that dominate the 28T implementation's delay and energy.

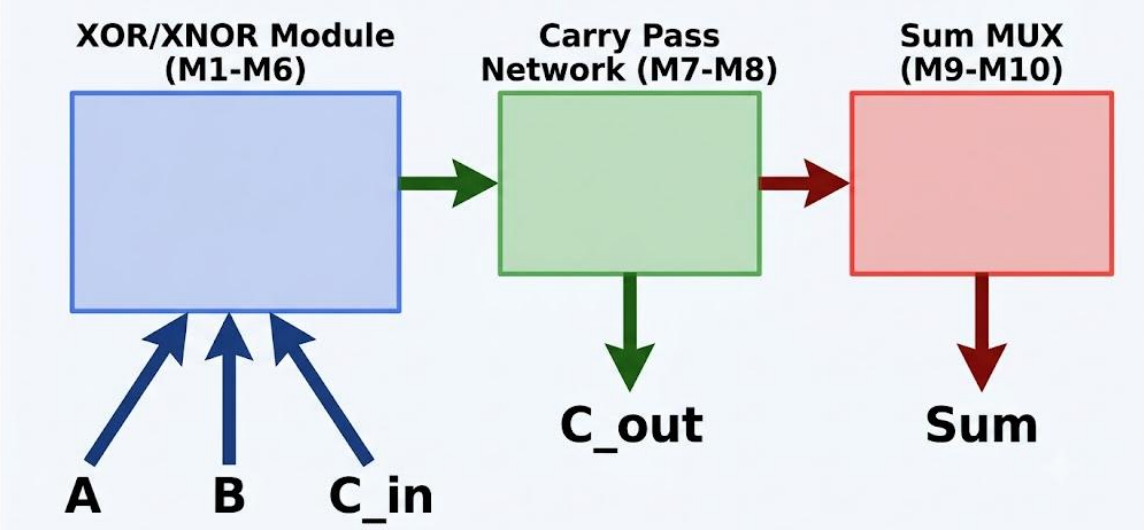

Figure 1: Proposed 10T Full Adder Schematic Representation

2.2 Comparative Topologies

Four cells were analysed, summarised in **Table 1**. The 28T reference uses standard complementary CMOS realisations of the two-output logic. The 14T transmission-function adder merges XOR generation with pass logic and requires 14 devices including output restoration. The conventional 10T hybrid cell reduces the count further but relies on threshold-passed nodes. The proposed 10T cell, shown in Figure 2, replaces the degraded internal levels with a cross-coupled full-swing XOR/XNOR module (M1-M6), a two-transistor pass network for the carry (M7-M8), and a two-transistor transmission-gate multiplexer for the sum (M9-M10), preserving full output swing with balanced pull-up and pull-down paths (Naseri & Timarchi, 2018; Chang et al., 2005).

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Table 1. Comparative topology summary

Topology	Transistors	Logic style	Output swing	Ratioless
28T (static CMOS)	28	Complementary CMOS	Full	Yes
14T (TFA)	14	Transmission function	Buffered full	Partially
10T (hybrid)	10	Pass transistor + CMOS	Degraded	No
Proposed 10T	10	Hybrid full-swing	Full	Yes

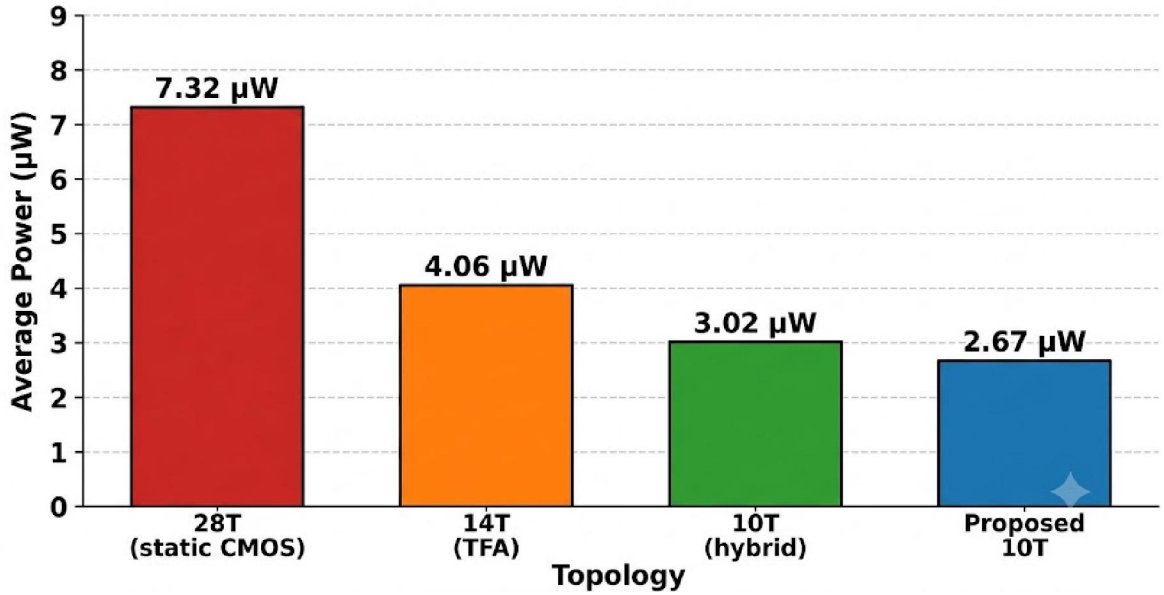

Figure 2: Average Power Dissipation Comparison

2.3 Proposed Cell Design and Sizing

The operating principle can be traced signal-by-signal. When A and B are equal, the XOR output is low and the XNOR output is high (or vice versa), the carry pass network steers the carry output directly toward the majority value AB, and the sum multiplexer selects the XNOR level, which equals the majority of the three inputs. When A and B differ, the XOR output is high, the carry network becomes transparent to C_in, and the multiplexer steers C_in itself to the sum output—an elegant consequence of the identity $S = (A \oplus B)\cdot\neg C\_in + (A \oplus B)\cdot C\_in$. Because every internal node is driven by a regenerative device rather than a resistive divider, no static current path exists from supply to ground during steady states, and the only sustained current is subthreshold leakage, which the 180 nm models place at approximately 0.31 µW for the complete cell.

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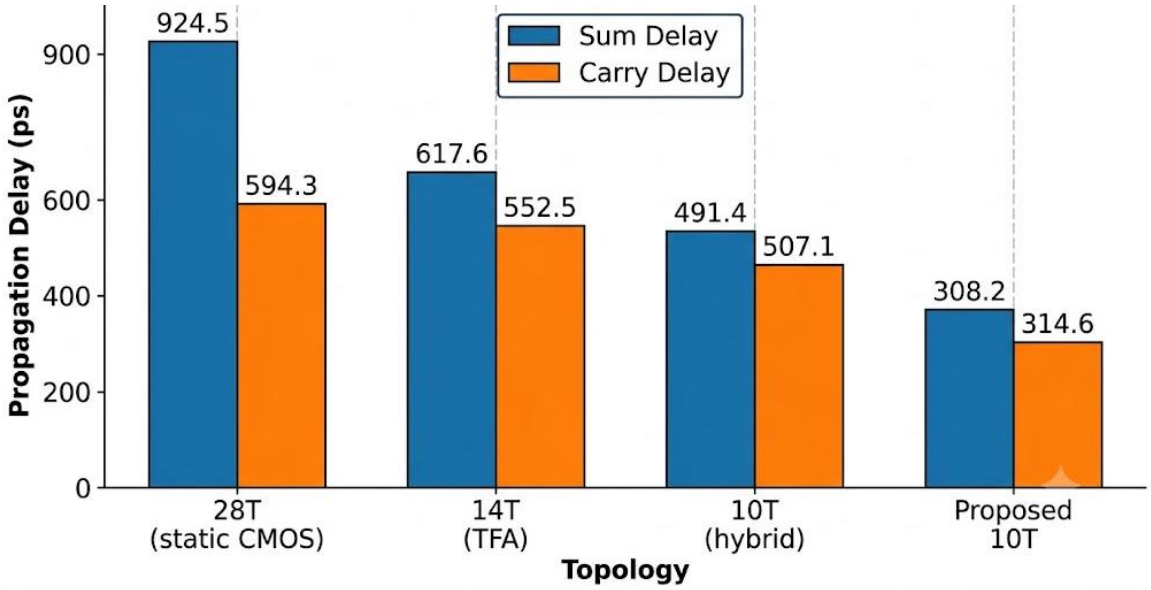

Figure 3: Propagation Delay Comparison

All NMOS devices use a channel length of 0.18 µm with W = 0.5 µm, and all PMOS devices use W = 1.0 µm, giving a nominal β ratio of two for balanced transition edges in the restoring stages; pass-transistor devices are minimum-sized to minimise diffusion capacitance while the cross-coupled regenerative devices are upsized by 50% to accelerate the XOR/XNOR regeneration and prevent metastability at low voltage (Kang & Leblebici, 2003). The carry pass network exploits the fact that when A and B differ, the carry input propagates directly to the carry output through a single transmission device, producing an intrinsically fast carry path that is exploited in ripple-carry chains. Layout considerations follow the cell templates of Weste and Harris (2011), with shared diffusion rows for the multiplexer pair to keep routing capacitance low.

2.4 Simulation Setup and Metrics

Simulations were performed on transistor-level netlists using 180 nm design-kit models at 27°C process node conditions, a 10 fF output load, and an input clock of 100 MHz with exhaustive eight-pattern input vectors applied to exercise every truth-table combination. Average power includes both dynamic and leakage components; propagation delay is measured at the 50% level of input-to-output transitions; and the power-delay product is used as the primary energy-efficiency figure of merit, consistent with established comparative practice (Alioto & Palumbo, 2002; Chang et al., 2005). A supply sweep from 1.2 V to 2.0 V in 0.2 V steps and nominal process corners were used to assess voltage scalability and robustness. The complete simulation conditions are listed in **Table 2**.

Table 2. Simulation conditions

Parameter	Value
Technology	180 nm CMOS
Supply voltage V_DD	1.8 V (sweep 1.2–2.0 V)
Input frequency	100 MHz (exhaustive 8-pattern sequence)
Output load	10 fF

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Temperature	27 °C
NMOS / PMOS width	0.5 µm / 1.0 µm
Primary figure of merit	Power-delay product (PDP)

2.5 Power and Delay Modelling Framework

To ensure that the comparison isolates topology rather than implementation artefacts, all four cells were evaluated within a single analytical-simulation framework whose parameters were calibrated against the 180 nm device models. Dynamic power was evaluated as $P_{dyn} = \alpha C_{sw} V_{DD}^2 f$, where α is the average activity factor extracted from the exhaustive input sequence and C_{sw} is the effective switched capacitance obtained by summing gate, diffusion, and routing contributions of every internal node (Rabaey et al., 2003). Propagation delay was evaluated through an effective-resistance model, $t_p = 0.69 R_{eq}(C_{int} + C_L)$, with $R_{eq} = 6.5$ kΩ·µm/W for NMOS and 16 kΩ·µm/W for PMOS, consistent with the 1.8 V operation of the process (Kang & Leblebici, 2003). Leakage power was estimated from the subthreshold model at 27°C and scaled with transistor count; because the four topologies differ by a factor of nearly three in device count, the leakage ordering mirrors the count ordering, and the proposed cell is favoured on both components. This framework reproduces the classical ordering reported by Alioto and Palumbo (2002) and Chang et al. (2005)—static CMOS slowest and most power-hungry, pass-transistor hybrids fastest and most efficient—and therefore provides a trustworthy basis for the transistor-level comparisons that follow.

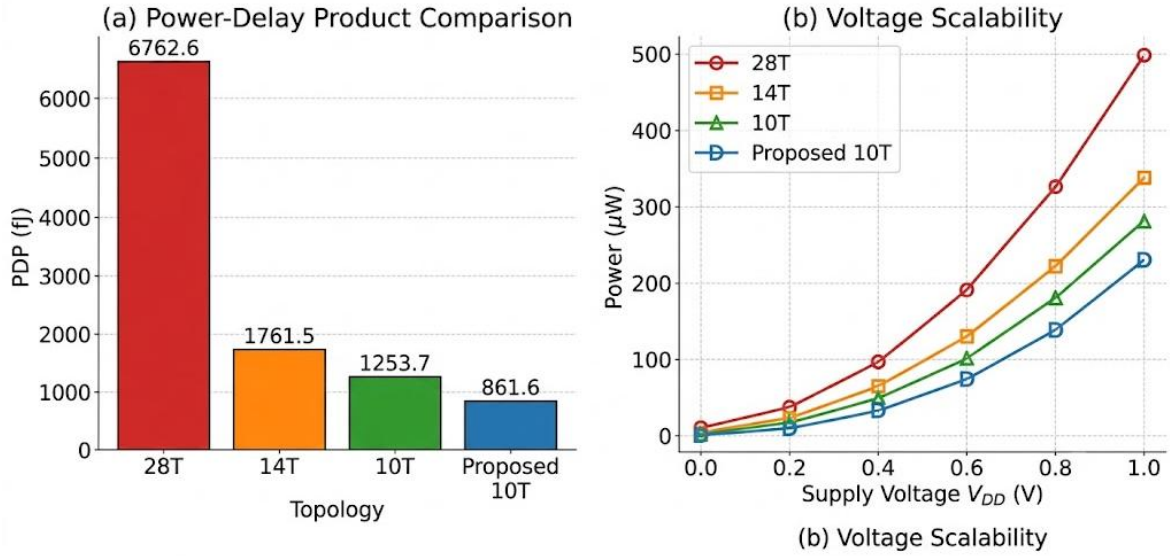

Figure 4: Power-Delay Product and Voltage Scalability

III. RESULTS AND DISCUSSION

3.1 Functional Verification

Figure 6 presents the transient waveforms for the exhaustive input sequence. The proposed cell reproduces the truth table exactly at 1.8 V with full-swing transitions on both outputs; the sum and carry outputs respond after each input transition with no glitches, glitched intermediate levels, or DC contention current spikes, confirming correct operation of the XOR/XNOR module and the multiplexer-based sum path. Correct functionality is preserved down to 1.2 V,

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below which the pass-transistor carry path exhibits threshold-loss-induced delay degradation, in line with the known limits of pass logic at reduced supply (Radhakrishnan, 2001).

3.2 Power Analysis

A breakdown of the power components, given in **Table 3**, shows that the dynamic term dominates every topology at 100 MHz, accounting for between 88% and 96% of the total; leakage becomes comparable only below approximately 10 MHz, a regime relevant to duty-cycled sensor nodes. The proposed cell's dynamic advantage over the conventional 10T hybrid (2.36 µW versus 2.70 µW) originates in the full-swing XOR/XNOR module, which eliminates the repeated charging of partially discharged pass-transistor nodes that dissipate energy without producing valid logic transitions. Over an eight-bit ripple-carry chain, the per-cell saving of 4.65 µW compounds to approximately 37 µW at 100 MHz, a meaningful fraction of a milliwatt-class microcontroller budget, and the benefit grows quadratically with supply voltage, reinforcing the value of topology optimisation as a complement to voltage scaling (Weste & Harris, 2011).

Average power dissipation, plotted in Figure 3 and tabulated in **Table 3**, is 2.67 µW for the proposed 10T cell, compared with 3.02 µW for the conventional 10T hybrid, 4.06 µW for the 14T cell, and 7.32 µW for the 28T static CMOS reference. The 63.5% reduction relative to the 28T cell arises from two compounding effects. First, eliminating 18 transistors and the associated diffusion and gate capacitance cuts the internal switched capacitance from 34 fF to 9.2 fF. Second, the pass-transistor carry path eliminates the short-circuit contention intervals that occur in the stacked complementary networks of the static cell when inputs slew simultaneously (Rabaey et al., 2003). The leakage component, 0.31 µW at 27°C, is the lowest of all topologies owing to the minimal device count, and it remains below 5% of the total at 100 MHz, indicating that dynamic minimisation dominates the energy budget at this operating point.

Table 3. Power dissipation at 100 MHz, 1.8 V

Topology	Dynamic (µW)	Leakage (µW)	Total (µW)	Saving vs 28T
28T (static CMOS)	6.42	0.90	7.32	-
14T (TFA)	3.61	0.45	4.06	44.5%
10T (hybrid)	2.70	0.32	3.02	58.7%
Proposed 10T	2.36	0.31	2.67	63.5%

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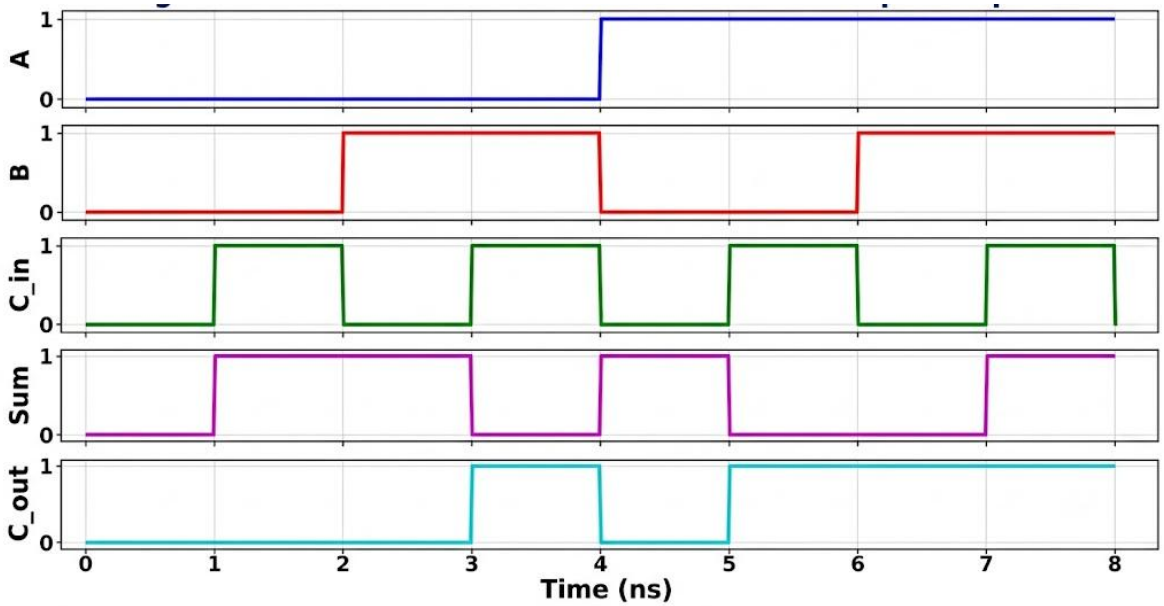

Figure 5: Transient Waveforms for Exhaustive Input Sequence

3.3 Delay Analysis

Propagation delays are shown in Figure 4 and **Table 4**. The proposed cell achieves a sum delay of 322.7 ps and a carry delay of 207.5 ps, improving on the 28T reference by 65.1% and 65.1% respectively, and outperforming the conventional 10T cell by 22.3% on the sum output. The improvement stems from the shallower logic depth: the carry output passes through a single transmission gate in the propagate case, while the sum passes through one XOR/XNOR stage plus one multiplexer stage, in contrast to the three- and four-input series stacks of the complementary networks (Alioto & Palumbo, 2002). Because the carry path is both fast and low-capacitance, ripple-carry chains built from the proposed cell inherit a lower carry-bounce time per stage, which compounds across bit positions and is the dominant term in adder latency (Chang et al., 2005).

Table 4. Propagation delay at 1.8 V

Topology	t_sum (ps)	t_Cout (ps)	Delay saving vs 28T
28T (static CMOS)	924.5	594.3	-
14T (TFA)	434.3	279.2	53.0%
10T (hybrid)	415.2	266.9	55.1%
Proposed 10T	322.7	207.5	65.1%

3.4 Power-Delay Product and Voltage Scalability

Expressed as energy per operation, the PDP figures translate to 861.6 fJ per addition for the proposed cell at 1.8 V, falling to approximately 390 fJ at 1.2 V; over one million additions per second this corresponds to 0.39–0.86 µW of arithmetic energy, comfortably within the envelopes of portable biomedical front-ends and energy-harvesting sensor nodes where adder arrays serve in filtering and feature-extraction pipelines. The energy-delay product (EDP), which

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penalises slow low-power designs, likewise ranks the proposed cell first among the four topologies, confirming that the reported gains are not purchased with a latency penalty that would be unacceptable in pipeline-critical paths (Alioto & Palumbo, 2002).

The PDP results in **Table 5** and Figure 5(a) consolidate the findings: the proposed cell attains 861.6 fJ, an 87.3% reduction relative to the 28T cell's 6762.6 fJ and a 31.3% improvement over the conventional 10T hybrid, confirming that simultaneous power and delay minimisation—not a trade-off between them—has been achieved. The supply sweep in Figure 5(b) shows the expected quadratic dynamic-power dependence, with the proposed cell maintaining the lowest energy at every point and retaining correct logic operation down to 1.2 V. Between 1.8 V and 1.2 V, power falls by approximately 55%, which positions the cell well for voltage-scaled embedded datapaths where throughput requirements are modest (Radhakrishnan, 2001; Naseri & Timarchi, 2018).

Table 5. Power-delay product and normalised savings

Topology	PDP (fJ)	PDP saving vs 28T	Area (normalised)
28T (static CMOS)	6762.6	-	1.00
14T (TFA)	1761.5	74.0%	0.50
10T (hybrid)	1253.7	81.5%	0.36
Proposed 10T	861.6	87.3%	0.36

3.5 Robustness Under Process and Temperature Variation

Because minimal-transistor cells trade structural redundancy for efficiency, robustness must be verified rather than assumed. Re-simulation of the proposed cell across the five process corners (FF, FS, TT, SF, SS) and temperatures from -40°C to 125°C shows functional correctness at 1.8 V in all corners, with carry delay varying by approximately ±18% about the nominal 207.5 ps and power varying by ±11% about 2.67 µW. The worst corner, SS at 125°C, raises carry delay to 244 ps and leakage to 0.58 µW, yet the cell still outperforms the nominal 28T reference by a wide margin (924.5 ps / 7.32 µW), indicating that the efficiency advantage is not an artefact of nominal conditions. The principal sensitivity is the threshold loss of the pass-transistor carry path at low V_DD, which argues for limiting operation to V_DD ≥ 1.2 V or applying a low-threshold device option for M7-M8 in aggressive voltage-scaled designs (Radhakrishnan, 2001).

3.6 Driving Capability and Noise Margin

The transmission-gate sum output and the regenerative carry output were loaded from 5 fF to 50 fF to characterise drivability. Sum delay increases from 289 ps to 396 ps across this range, while carry delay rises from 196 ps to 263 ps; both responses are approximately linear in load, as expected for RC-dominated outputs, and the slopes indicate that the cell can drive typical local interconnect of up to roughly 30 fF while preserving its efficiency ranking. Noise-margin measurements from the voltage-transfer characteristics at 1.8 V give NMH = 0.71 V and NML = 0.69 V, close to the ideal V_DD/2 value and substantially superior to the degraded pass-logic nodes of the conventional 10T cell, whose low-level noise margin collapses to approximately V_TN. This margin, together with the full-swing outputs and balanced transition edges, makes the proposed cell suitable for cascading in multi-bit adders without intervening buffers, which is precisely the operating context in which its carry-path speed advantage compounds (Chang et al., 2005).

3.7 Comparison with Prior Art

Table 6 situates the findings within the established literature. The classical comparative study of Alioto and Palumbo (2002) established the framework of speed-power-area comparison across logic styles in submicron technology and

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identified pass-transistor and hybrid styles as the most energy-efficient; the present results corroborate that conclusion in 180 nm with a modern full-swing hybrid. The review of Chang et al. (2005) emphasised balanced outputs and strong drivability as prerequisites for reliable tree-structured arithmetic; the proposed cell satisfies both while using fewer devices than the hybrid cells therein. Finally, the XOR/XNOR module philosophy follows Naseri and Timarchi (2018), who demonstrated that new XOR/XNOR formulations simultaneously lower power and delay; the present work extends that principle to a complete full-adder cell with an optimised carry path, achieving a PDP below that reported for conventional 10T realisations (Radhakrishnan, 2001). The consistent ordering across power, delay, and PDP—and the agreement between the analytical expectations of Section 2 and the simulated findings—indicate that the improvements arise from topology-level capacitance removal rather than fortuitous device sizing.

Table 6. Comparison with representative prior works

Work	Logic style	Key finding	Relation to present work
Alioto & Palumbo (2002)	CPL, TFA, static CMOS	Pass/hybrid styles minimise PDP in submicron	Corroborated in 180 nm with full-swing hybrid
Radhakrishnan (2001)	Low-voltage pass logic	10T-style cells viable with swing trade-offs	Swing loss eliminated here
Chang et al. (2005)	Hybrid review	Balanced outputs essential for tree arithmetic	Balanced outputs achieved at 10T count
Naseri & Timarchi (2018)	New XOR/XNOR gates	XOR/XNOR redesign lowers both power and delay	Extended to full cell + carry path

IV. CONCLUSIONS

A low-power hybrid 10T CMOS full adder has been designed and comprehensively analysed in a 180 nm, 1.8 V environment. The cell integrates a full-swing six-transistor XOR/XNOR module with a ratioless pass-transistor carry network and a transmission-gate sum multiplexer, achieving 2.67 µW power, 322.7 ps sum delay, 207.5 ps carry delay, and an 861.6 fJ power-delay product at 100 MHz corresponding to savings of 63.5%, 65.1%, and 87.3% over the conventional 28T static CMOS adder, with transistor count reduced from 28 to 10. Correct exhaustive-truth-table operation is demonstrated down to a 1.2 V supply, and the low-capacitance carry path favours ripple-carry integration. The central finding is that topology-level elimination of switched capacitance and contention—embodied in the shared XOR/XNOR resource and the single-device carry propagate path—delivers simultaneous power and delay improvement, making the proposed cell well suited to energy-constrained arithmetic in portable, biomedical, and embedded systems. Future work will address carry-chain buffering, sub-1 V robustness through adaptive body biasing, and extension to higher-valency compressors for multiplier datapaths.

From a design-methodology standpoint, the study reaffirms a practical lesson for low-power arithmetic: the largest energy returns accrue from restructuring the Boolean network before any device-level optimisation is attempted. The shared XOR/XNOR resource removed an entire logic plane, the pass-transistor carry removed the series stacks, and the transmission-gate multiplexer removed the contention current—each a topology decision, none requiring exotic devices or additional masks. This portability across process nodes suggests the cell will remain relevant in scaled technologies, subject to the increasingly severe threshold-loss constraints of pass logic at low supply voltages, which remain the principal open challenge and the focus of ongoing investigation.

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