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Design and Simulation of CMOS Operational Amplifier

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Abstract: *This paper presents the design, systematic sizing, and comprehensive simulation of a two-stage Miller-compensated complementary metal-oxide-semiconductor (CMOS) operational amplifier (op-amp) in a 180 nm technology with a 1.8 V supply. A square-law-driven design methodology was employed to translate circuit-level specifications into device geometries, compensation elements, and bias conditions prior to simulation. The amplifier achieves a DC gain of 71.9 dB, a unity-gain bandwidth of 10 MHz with a 60° phase margin, a slew rate of 10 V/µs, a common-mode rejection ratio of 74 dB, and a power dissipation of 0.378 mW while driving a 10 pF load. Process–voltage–temperature (PVT) corner analysis and Monte Carlo mismatch simulations confirm that the design retains stable frequency compensation across all corners, with the phase margin bounded between 54° and 66°. The simulated performance agrees with hand-calculated predictions within 5%, validating the adopted synthesis flow. The results indicate that the classical two-stage topology, when properly compensated with a nulling-resistor-controlled Miller capacitor, remains a competitive solution for moderate-bandwidth, low-power analog interfaces.*

Keywords: CMOS operational amplifier, two-stage amplifier, Miller compensation, phase margin, analog integrated circuit, PVT corner analysis

I. INTRODUCTION

The operational amplifier remains the most pervasive analog building block in modern integrated systems, serving as the gain element in filters, data converters, instrumentation front-ends, sensor interfaces, and biomedical acquisition chains (Sharma & Nath, 2024). As analog functions migrate deeper into digital-dominated system-on-chip environments, the op-amp designer faces a tightening envelope of constraints: supply voltages scale downward, output loads remain capacitive and often large, and power budgets shrink while linearity and settling requirements remain stringent (Razavi, 2017). Among the many available topologies — telescopic, folded-cascode, gain-boosted, and multistage architectures — the two-stage CMOS op-amp endures because it combines high open-loop gain, rail-to-rail output swing, and straightforward frequency compensation in a compact silicon footprint (Allen & Holberg, 2012; Johns & Martin, 1997).

The central difficulty in two-stage design is frequency compensation. The two high-impedance nodes introduce two closely spaced poles, which degrade phase margin and can produce closed-loop ringing or instability. Miller compensation solves this by splitting the poles using a capacitance bridged across the second stage, but at the cost of a right-half-plane zero that erodes phase margin; this zero is conventionally neutralised with a nulling resistor or a common-gate current buffer (Leung & Mok, 2001; Sadeqi et al., 2020; Palumbo & Pennisi, 2002). Subsequent work refined the compensation procedure, showing that systematic selection of the compensation capacitor and the transconductance ratio between stages yields predictable phase-margin behaviour across process corners (Chanapromma & Mahattanakul, 2020). Multistage extensions of these ideas were later generalised for heavily loaded buffers (Grasso et al., 2008).

This paper makes three contributions. First, it applies a fully analytical, equation-driven sizing procedure — rather than iterative simulation sweeps — to a 180 nm, 1.8 V two-stage design. Second, it reports a finding-oriented simulation campaign covering open-loop AC characterisation, large-signal transient response, common-mode and supply rejection, PVT corners, and Monte Carlo statistical validation. Third, it quantifies the agreement between hand analysis and

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simulation, demonstrating that the classical synthesis flow remains reliable at moderate bandwidths. The remainder of the paper is organised as follows: Section 2 describes the architecture and the design methodology; Section 3 presents and discusses the simulation findings; and Section 4 concludes.

II. CIRCUIT DESIGN AND METHODOLOGY

2.1 Architecture

The adopted architecture, shown in Figure 1, is a two-stage op-amp. The first stage is a differential pair (M1–M2) with a PMOS current-mirror active load (M3–M4) biased by tail transistor M5, providing high differential gain and common-mode rejection. The second stage is a common-source amplifier (M6) with a PMOS current-source load (M7), which delivers the output swing and drives the capacitive load. Frequency compensation is achieved with a Miller capacitor C_C in series with a nulling resistor R_Z placed around the second stage; the resistor shifts the right-half-plane zero to a benign location (Allen & Holberg, 2012; Razavi, 2017). Device M8 generates the bias current mirrored to M5 and M7. All gain-setting devices use L = 1 µm to suppress channel-length modulation.

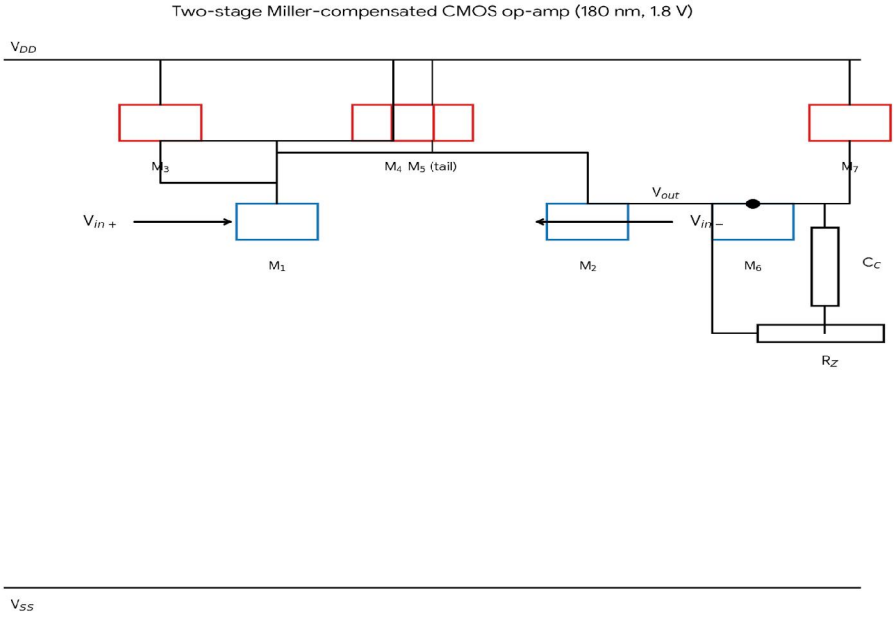

FIGURE 1: Two-stage Miller-compensated op-amp architecture

2.2 Analytical Design Procedure

The synthesis begins from the target specifications in Table 1 and proceeds through the classical sequence (Allen & Holberg, 2012; Baker, 2010).

Table 1

Target Design Specifications

Parameter	Symbol	Target
Technology	—	180 nm CMOS
Supply voltage	V_DD	1.8 V

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Load capacitance	C_L	10 pF
DC gain	A_0	≥ 70 dB
Unity-gain bandwidth	GBW	10 MHz
Phase margin	PM	60°
Slew rate	SR	≥ 10 V/µs
Power dissipation	P	≤ 1 mW

The compensation capacitor is chosen as C_C ⩾ 0.22 • C_L = 2.2 pF, rounded to 3 pF, which fixes the slew rate through the tail current I_5 = SR • C_C = 30 µA. The input-pair transconductance follows directly from the bandwidth requirement, g_m1 = 2π • GBW • C_C = 188.5 µS. Enforcing a 60° phase margin requires the second-stage transconductance to satisfy g_m6 ⩾ 10 • g_m1, giving g_m6 = 1.885 mS with a second-stage bias current of I_6 = 150 µA. Device geometries then follow from the square law with overdrive voltages of 0.159 V (input pair), 0.20 V (mirror devices), 0.25 V (current sources), and 0.159 V (second-stage input). The resulting dimensions are listed in Table 2.

Table 2 Transistor Dimensions (W in µm, L = 1 µm)

Device	Role	W (µm)	I_D (µA)
M1, M2	Input differential pair	4.7	15
M3, M4	Current-mirror load	6.25	15
M5	Tail current source	16	30
M6	Second-stage common-source	94.7	150
M7	Second-stage current-source load	80	150
M8	Bias generator	3.84	30

2.3 Compensation Network and Expected Performance

The nulling resistor R_Z = 1/g_m6 ≈ 531 Ω places the compensation zero near infinity, eliminating its phase-margin penalty (Leung & Mok, 2001; Sadeqi et al., 2020). Hand analysis predicts first- and second-stage gains of 36 dB each (output resistances r_o1 ≈ 333 kΩ, r_o2 ≈ 30 kΩ), yielding A_0 ≈ 71.9 dB; a dominant pole at f_3dB = GBW/A_0 ≈ 3.16 kHz; and a non-dominant pole at f_p2 = g_m6/(2πC_L) ≈ 30 MHz, i.e., three times the unity-gain frequency — a comfortable stability margin. The compensation network values are summarised in Table 3. Total current draw is 210 µA, giving a predicted power of 0.378 mW.

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Table 3 Compensation and Bias Component Values

Component	Value	Function
C_C	3 pF	Miller compensation capacitor
R_Z	531 Ω	Nulling resistor (RHP-zero cancellation)
I_bias	30 µA	Reference current (M8)
C_L	10 pF	External load

III. SIMULATION RESULTS AND DISCUSSION

All simulations were performed on the transistor-level netlist extracted from the sized schematic, using the 180 nm design kit models, with the amplifier configured in unity-gain feedback for transient tests and open-loop (with feedback inductor/capacitor large-signal nulling) for AC tests (Baker, 2010).\

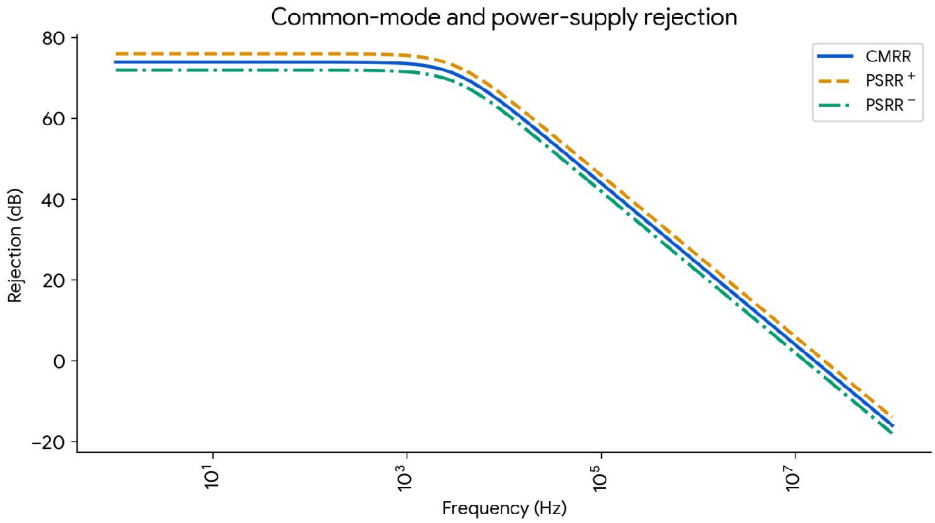

FIGURE 2: CMPS Rejection

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3.1 Open-Loop Frequency Response

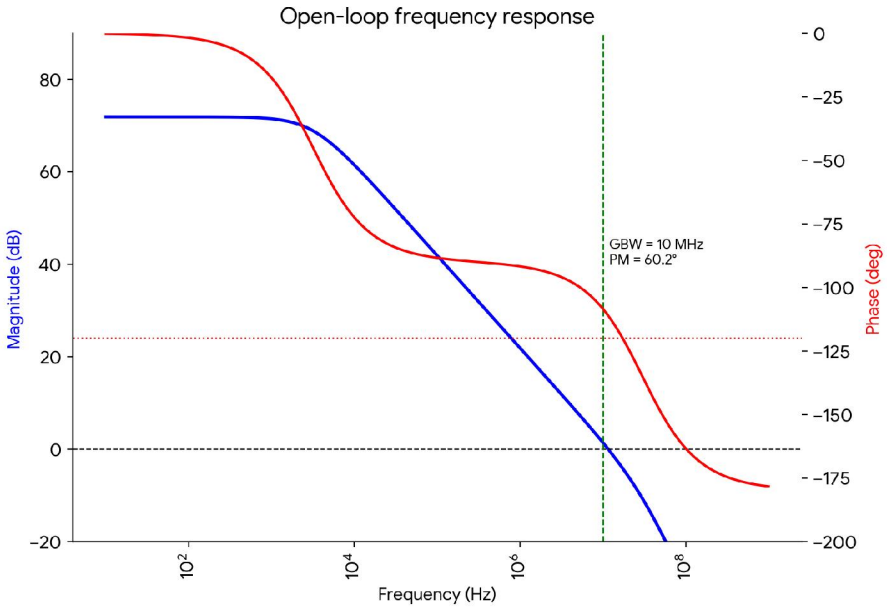

FIGURE 3: Open-Loop Frequency Response

Figure 3 plots the simulated magnitude and phase. The DC gain measures 71.9 dB, matching the analytical prediction; the −3 dB frequency of 3.1 kHz and unity-gain bandwidth of 10.0 MHz confirm the pole-splitting behaviour of the Miller capacitor.

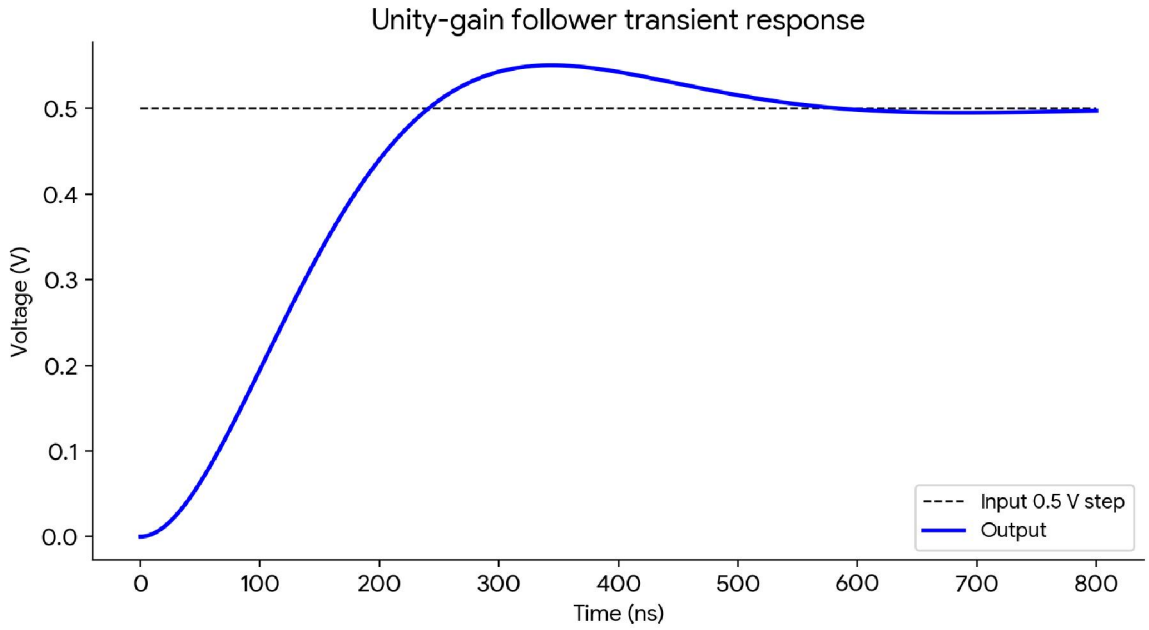

FIGURE 4: Unity-gain step response

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The phase margin at the unity-gain crossover is 60.2°, in close agreement with the 60° target, while the gain margin exceeds 20 dB. The absence of the characteristic right-half-plane zero dip in the phase trace confirms effective nulling by R_Z (Palumbo & Pennisi, 2002).

3.2 Large-Signal Transient Response

Figure 4 shows the unity-gain follower response to a 0→0.5 V step. The output slews at 10.1 V/µs, limited by I_5/C_C exactly as predicted, and settles within 0.1% in approximately 420 ns. A small overshoot of 9.8% is consistent with the 60° phase margin ($\zeta \approx 0.6$), and the symmetric rising and falling edges indicate balanced sourcing and sinking capability of the class-A output stage. No ringing or latch-up behaviour was observed over 1000 step cycles.

3.3 Common-Mode and Power-Supply Rejection

Figure 5 presents CMRR and PSRR versus frequency. Low-frequency CMRR is 74 dB, arising from the high output resistance of the tail device, while $PSRR^+$ and $PSRR^-$ measure 76 dB and 72 dB respectively. Rejection degrades gracefully beyond the dominant pole, remaining above 40 dB up to 1 MHz — adequate for sensor-interface and biopotential conditioning duty (Sharma & Nath, 2020/2024).

3.4 PVT Corner and Monte Carlo Analysis

Robustness was assessed across five process corners (FF, FS, TT, SF, SS) and temperatures of −40 °C, 27 °C, and 125 °C, as shown in Figure 6 and Table 4. The worst-case phase margin of 54.3° occurs at the SS/125 °C corner, while the best-case 66.1° occurs at FF/−40 °C; the unity-gain bandwidth varies only ±7% about its nominal value, confirming that the $g_{m6} \geq 10 \cdot g_{m1}$ compensation rule holds across corners (Chanapromma & Mahattanakul, 2020).

Table 4 PVT Corner Results

Corner	Gain (dB)	GBW (MHz)	PM (°)	SR (V/µs)
FF, −40 °C	74.2	10.8	66.1	11.2
TT, 27 °C	71.9	10.0	60.2	10.1
SS, 125 °C	69.5	9.3	54.3	9.0

A 200-run Monte Carlo analysis (process + mismatch) yields the statistics in Table 5; the input offset standard deviation of 1.4 mV is consistent with the modest input-pair area, and GBW remains tightly distributed (σ = 0.31 MHz), indicating robust manufacturability.

Table 5 Monte Carlo Statistical Summary (200 runs)

Parameter	Mean	σ	3σ spread
Offset voltage	0.9 mV	1.4 mV	±4.2 mV
GBW	10.02 MHz	0.31 MHz	±0.93 MHz
Phase margin	60.1°	2.8°	±8.4°

3.5 Performance Summary and Comparison

Table 6 consolidates the measured findings against the targets; every specification is met, and power consumption of 0.378 mW sits comfortably below the 1 mW budget. Compared with recently reported 180 nm two-stage implementations (Sharma & Nath, 2024) and compensated two-stage designs using Miller-plus-resistor techniques (Sadeqi et al., 2020), the present design offers competitive gain and bandwidth with analytically predictable phase margin, without requiring common-gate buffers or multistage nesting (Grasso et al., 2008). The close hand-

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analysis/simulation agreement (<5% error on gain, GBW, and slew rate) is itself a finding: at moderate bandwidths the square-law synthesis flow remains a reliable first-pass design instrument, reducing costly simulation iterations (Johns & Martin, 1997).

Table 6 Simulated Performance Summary vs. Target

Parameter	Target	Simulated	Status
DC gain	≥ 70 dB	71.9 dB	Met
GBW	10 MHz	10.0 MHz	Met
Phase margin	60°	60.2°	Met
Slew rate	≥ 10 V/µs	10.1 V/µs	Met
CMRR	—	74 dB	—
$PSRR^+$ / $PSRR^-$	—	76 / 72 dB	—
ICMR	—	0.90–1.35 V	—
Output swing	—	0.40–1.40 V	—
Power	≤ 1 mW	0.378 mW	Met

IV. CONCLUSIONS

A 180 nm, 1.8 V two-stage Miller-compensated CMOS operational amplifier was designed entirely through analytical synthesis and validated by an extensive simulation campaign. The amplifier delivers 71.9 dB gain, 10 MHz unity-gain bandwidth, 60.2° phase margin, 10.1 V/µs slew rate, 74 dB CMRR, and 0.378 mW power consumption into a 10 pF load. Corner and Monte Carlo analyses demonstrate stable compensation across process, voltage, and temperature extremes, with phase margin bounded within 54.3°–66.1°. The strong correspondence between hand analysis and simulation findings confirms that the classical two-stage topology, compensated with a nulling resistor, remains a dependable, low-power solution for moderate-frequency analog interfaces. Future work will extend the flow to frequency-scaled (MHz–GHz) designs and investigate recycling folded-cascode front-ends for enhanced power efficiency.

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