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Post-Silicon Timing Characterization of Dynamic Logic Using a Single Ring-Oscillator-Based Test Structure

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Abstract: *Dynamic logic offers high speed and reduced transistor count, but its precharge-evaluation operation introduces timing arcs that are more complex than those of static CMOS. Conventional simulation-based characterization may not faithfully represent post-fabrication behavior under process variation, supply fluctuation, loading mismatch, and temperature drift. This paper presents an expanded methodology for a single ring-oscillator-based test structure that extracts data-to-output delay, clock-to-output rise and fall delays, setup time, hold time, data-to-data timing constraints, duty-cycle asymmetry, and timing-failure probability from one observable output. The architecture combines five cascaded delay-measurement blocks, two setup/hold-measurement blocks, a multi-phase generator, programmable input-slew and output-load networks, through/bypass differential paths, and coarse/fine skew generators. Common parasitic delays are cancelled by differential period or pulse-width measurements, while repeated circulation of the timing event enables robust boundary detection under realistic operating conditions. Analytical expressions are derived for timing extraction, calibration, uncertainty, and error-rate estimation. The proposed workflow supports characterization across input transition, output capacitance, voltage, temperature, and process conditions and can directly populate lookup tables required by standard-cell liberty models. A results section is intentionally reserved for measured or simulated data to be inserted by the user.*

Keywords: Dynamic logic, domino circuit, ring oscillator, timing characterization, propagation delay, setup time, hold time, post-silicon validation, liberty file, process variation.

I. INTRODUCTION

Dynamic CMOS circuits use a clock-controlled precharge device and an evaluation network to implement logic with smaller input capacitance and reduced pull-up complexity. These characteristics make domino and related dynamic circuit families attractive for high-speed arithmetic, critical data paths, mixed-signal interfaces, and deeply pipelined systems [1], [2]. Hybrid dual-mode logic further demonstrates that static robustness and dynamic speed can be combined in practical digital blocks [3]-[6].

Despite their speed advantage, dynamic circuits are difficult to integrate into conventional static timing analysis because the output depends not only on data arrival but also on the clock phase, the history of the dynamic node, charge sharing, leakage, keeper contention, input ordering, and the width of the precharge and evaluation windows. Earlier studies established important timing constraints for dynamic and sequential domino circuits [7]-[12], but post-silicon

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extraction remains necessary because fabricated silicon may deviate from pre-layout and post-layout simulation models.

Post-silicon timing characterization is especially important at advanced technology nodes where random and systematic process variation, interconnect parasitics, local supply noise, temperature gradients, aging, and measurement loading can alter delay and timing margins. General post-silicon validation methods and dedicated on-chip timing platforms have therefore become important for correlating silicon behavior with design models [16]-[18]. Ring oscillators are widely used for such tasks because a small per-stage delay is accumulated over many stages and transformed into a frequency that can be measured accurately [19]-[22].

A conventional inverter ring, however, cannot directly exercise the precharge/evaluation sequence of a dynamic gate or independently extract the several timing arcs needed for a liberty model. A specialized architecture is required to propagate only the relevant edge, reset the dynamic node at the correct time, selectively include or bypass the device under test, and generate controllable clock-data skew. Building on the single-ring concept reported in [13], [14], this paper presents a detailed research methodology, analytical model, measurement sequence, verification plan, and uncertainty framework suitable for an academic project or ASIC test-chip implementation.

The principal contribution is a unified test structure that converts a set of difficult time-domain constraints into period, pulse-width, oscillation-boundary, and oscillation-duration measurements at one output. The methodology minimizes sensitivity to common test-path delay through differential extraction, supports programmable input-slew and output-load conditions, and repeatedly tests setup/hold constraints over many cycles rather than making a single pass/fail observation.[23]

II. LITERATURE SURVEY

2.1 Dynamic-Logic Timing Models

Krambeck et al. introduced high-speed CMOS dynamic circuits and established the architectural basis for precharge-evaluation logic [1]. Standard VLSI texts later formalized domino operation, noise concerns, charge sharing, monotonicity, and keeper design [2]. Because a dynamic output is conditioned by both data and clock, its timing model requires more arcs than a static combinational gate.

Venkat et al. presented timing verification concepts for dynamic circuits [7], while Van Campenhout et al. developed methods for sequential domino and sequential dynamic timing verification [8], [9]. Thorp et al. studied design and synthesis methodologies for dynamic circuits [10], and Jung et al. analyzed timing-dependent keeper constraints [11]. Yuzhaninov et al. proposed a characterization flow for dual-mode logic [12]. These works motivate explicit definitions of data-clock and data-data constraints but largely rely on simulation-derived values.

2.2 Post-Silicon Validation and On-Chip Timing Measurement

Mitra et al. summarized the opportunities and challenges of post-silicon validation, emphasizing observability, controllability, and model-to-silicon correlation [16]. Yang et al. demonstrated a universal high-frequency on-chip testing platform [17], and Agarwal et al. reported high-resolution characterization circuits for memory timing parameters [18]. These contributions show that embedded test support can provide timing information that is difficult to obtain through external probing alone.

Setup/hold characterization traditionally uses two programmable paths whose relative delay is swept until a functional boundary is observed. Two-step digital calibration [11], memory timing test circuits [12], and memory-compiler characterization structures [13] provide useful precedents. Nevertheless, a single boundary observation can be vulnerable to jitter and metastability, whereas a ring-based repeated test offers stronger statistical confidence.

2.3 Ring-Oscillator-Based Delay and Variability Measurement

Ring oscillators have been used for process monitoring, gate-delay measurement, NBTI/PBTI analysis, and within-die variability characterization [19]-[22]. Reconfigurable rings enable different paths or device types to be selected while

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preserving a common measurement infrastructure [24],[25]. Differential ring measurements have also been applied to library-cell characterization in other device technologies [23].

The primary advantage is delay amplification. If N identical stages each contribute delay t_d, the oscillation period is approximately 2Nt_d for a conventional inverting ring. However, dynamic gates are non-inverting and need explicit reset sequencing. The specialized dynamic ring in [21] addresses oscillation using feedback-controlled reset, but it does not provide the complete collection of clock-to-output, setup/hold, slew-dependent, and load-dependent timing arcs required for library construction.

2.4 Research Gap

The literature indicates four remaining needs: (i) a complete and unambiguous definition of dynamic-circuit timing arcs; (ii) extraction of all major arcs using one physical ring to limit location-dependent mismatch; (iii) differential cancellation of switch, wiring, and dummy-cell delays; and (iv) repeated setup/hold testing that provides both a boundary and an estimated failure probability. The proposed methodology addresses these needs in an integrated architecture.

III. METHODOLOGY

3.1 Methodology Overview

The complete methodology consists of timing-arc definition, single-ring construction, programmable delay measurement, setup/hold measurement, differential extraction, calibration, PVT sweeping, statistical uncertainty analysis, and liberty-table generation. Five delay-measurement blocks and two setup/hold blocks are connected in one loop. Each delay block contains four identical units, resulting in twenty instances of the dynamic cell under test for propagation-delay extraction. A phase generator derives local evaluation and precharge clocks from adjacent ring outputs so that a transition is accepted only when the destination block is in evaluation and the source block is reset after the transition has advanced.

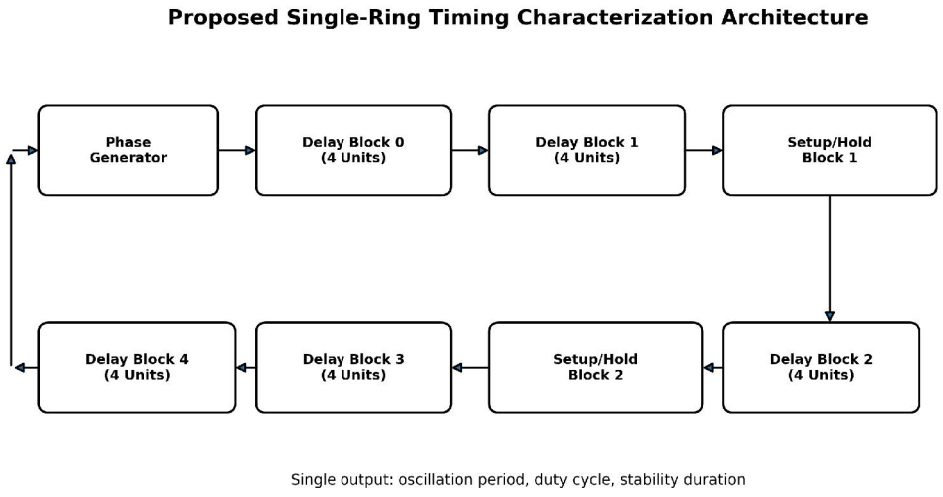

Fig. 1. Proposed single-ring architecture for complete dynamic-circuit timing characterization.

3.2 Definition of Timing Parameters

Consider a domino-style dynamic cell with data input D, clock CLK, and static output Q. During evaluation, a rising data transition can discharge the internal dynamic node and produce a rising transition at the static output. During

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precharge, the falling clock transition resets the dynamic node and produces a falling output transition. The data-to-output delay is defined as

$$t_{d2q} = t\,(Q_{\text{rise}}) - t\,(D_{\text{rise}}) \qquad (1)$$

Because both clock edges can alter the output, separate clock-to-output delays are required:

$$t_{\text{clkr2q}} = t\,(Q_{\text{rise}}) - t\,(\text{CLK}_{\text{rise}}) \qquad (2)$$

$$t_{\text{clkf2q}} = t\,(Q_{\text{fall}}) - t\,(\text{CLK}_{\text{fall}}) \qquad (3)$$

The rising-data setup constraint is referenced to the falling edge of CLK, which terminates evaluation. The falling-data hold constraint is referenced to the rising clock edge, which begins evaluation:

$$t_{\text{stu-drcf}} = t\,(\text{CLK}_{\text{fall}}) - t\,(\text{DATA}_{\text{rise}}) \qquad (4)$$

$$t_{\text{hld-dfcr}} = t\,(\text{DATA}_{\text{fall}}) - t\,(\text{CLK}_{\text{rise}}) \qquad (5)$$

For series-connected inputs A and B, correct discharge may require A to rise sufficiently before B falls. The corresponding data-to-data setup constraints are

$$t_{\text{stu-arbf}} = t\,(B_{\text{fall}}) - t\,(A_{\text{rise}}) \qquad (6)$$

$$t_{\text{stu-braf}} = t\,(A_{\text{fall}}) - t\,(B_{\text{rise}}) \qquad (7)$$

Together, (1)-(7) form a sufficient set of principal arcs for a basic domino AOI cell. Additional arcs may be added for more inputs, keeper control, scan/test modes, minimum pulse width, or multi-output cells.

3.3 Ring-Oscillator Operation

Each block receives a locally generated clock. Before the propagating edge enters block k, CLK_k is placed in evaluation. When block k+1 produces its output transition, the phase generator returns block k to precharge, resetting all dynamic nodes in that block. The next transition then progresses around the ring. This edge-selective sequence differs from a conventional inverter ring because the dynamic cell propagates one functional edge and relies on a later phase event for reset.

The general oscillation period may be written as

$$T_{\text{RO}} = T_{\text{fixed}} + \sum_{k=1}^{M} T_{\text{block},k} \qquad (8)$$

where T_fixed contains phase-generator and setup/hold-block delay and T_block,k contains the cascaded measurement-unit delay. Since the same physical loop is used in through and bypass modes, most common terms cancel in the difference.

3.4 Delay-Measurement Unit

The delay-measurement unit contains an input selector, the dynamic cell under test, a programmable input-slope network, a programmable output-load network, output switches, and a dummy dynamic cell. The input selector connects the circulating signal to the timing pin under test while idle pins are forced to sensitizing values. In Mode T, the signal propagates through the device under test. In Mode P, the selected signal bypasses the device. The dummy cell preserves the reset behavior and contributes approximately equal delay in both modes.

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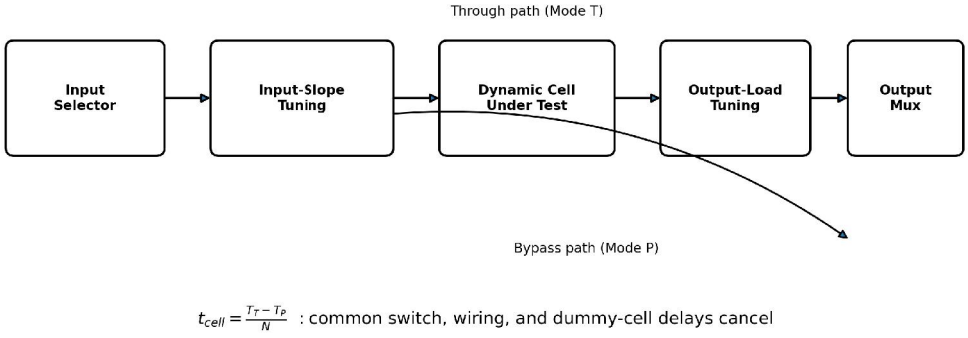

Fig. 2. Delay-measurement unit and through/bypass differential extraction principle.

3.5 Data-to-Output Delay Extraction

Let T_T be the measured oscillator period in through mode and T_P the period in bypass mode. For N identical devices under test, the period models are

$$T_{\mathrm{T}} = T_{\mathrm{exc}} + N\left(t_{\mathrm{aux}} + t_{\mathrm{d2q}}\right) \qquad (9)$$

$$T_{\mathrm{P}} = T_{\mathrm{exc}} + N\, t_{\mathrm{aux}} \qquad (10)$$

where T_exc represents delay external to the measurement units and t_aux represents common switch, dummy, and local wiring delay. Subtracting gives

$$t_{\mathrm{d2q}} = \frac{T_{\mathrm{T}} - T_{\mathrm{P}}}{N} \qquad (11)$$

For the proposed architecture N = 20. Measuring multiple periods and averaging reduces counter quantization and random jitter. If K periods are accumulated over observation time T_obs, then

$$\hat{T}_{\mathrm{RO}} = \frac{T_{\mathrm{obs}}}{K} \qquad (12)$$

$$\hat{t}_{\mathrm{d2q}} = \frac{\hat{T}_{\mathrm{T}} - \hat{T}_{\mathrm{P}}}{20} \qquad (13)$$

3.6 Clock-to-Output Rise and Fall Delay

To measure clock-to-output delay, all data inputs are held at values that keep the pull-down network active, and the circulating signal is routed to the dynamic-cell clock. Because the pull-up and pull-down paths are asymmetric, positive and negative output pulse widths are measured separately. Define differential widths

$$\Delta W^{+} = W_{\mathrm{T}}^{+} - W_{\mathrm{P}}^{+} \qquad (14)$$

$$\Delta W^{-} = W_{\mathrm{T}}^{-} - W_{\mathrm{P}}^{-} \qquad (15)$$

For a loop in which nineteen stages contribute one polarity delay and one stage contributes the opposite polarity delay, the measured differences satisfy

$$\Delta W^{+} = 19\, t_{\mathrm{clkr2q}} + t_{\mathrm{clkf2q}} \qquad (16)$$

$$\Delta W^{-} = 19\, t_{\mathrm{clkf2q}} + t_{\mathrm{clkr2q}} \qquad (17)$$

Solving the simultaneous equations yields

$$t_{\mathrm{clkr2q}} = \frac{19\Delta W^{+} - \Delta W^{-}}{360} \qquad (18)$$

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$$t_{\text{clkf2q}} = \frac{19\Delta W^{-} - \Delta W^{+}}{360} \qquad (19)$$

The pulse-width method is preferable to period-only measurement because a period contains the sum of rise and fall delays and cannot independently resolve the two asymmetric arcs.

3.7 Input-Slew and Output-Load Tuning

A standard-cell timing model tabulates delay and transition as functions of input transition S and effective load capacitance C_L. The input-slope network uses selectable buffer strength or capacitive loading to generate several transition values. The output-load network uses a binary- or thermometer-coded capacitor bank. At tuning indices i and j, the extracted delay is

$$t_{\text{d2q}}(i,j) = \frac{T_{\text{T}}(i,j) - T_{\text{P}}(i,j)}{N} \qquad (20)$$

A first-order delay model useful for checking the measured trend is

$$t_{\text{pd}}\,(S, C_{\text{L}}) = t_{\text{int}} + k_{\text{s}}S + R_{\text{eq}}C_{\text{L}} \qquad (21)$$

where t_int is intrinsic delay, k_s represents slew sensitivity, and R_eq is an effective output resistance. The final liberty table uses measured values rather than relying on the linear approximation.

3.8 Setup/Hold-Time Measurement

Two setup/hold blocks are inserted into the ring. Block 1 measures data-clock constraints, and Block 2 measures data-data constraints. Each block contains a dynamic cell and a skew generator with two nominally matched paths. The skew is initially set to a safe value. The test then reduces the timing margin until the ring no longer sustains oscillation for the required observation interval. The last stable setting defines the measured timing boundary.

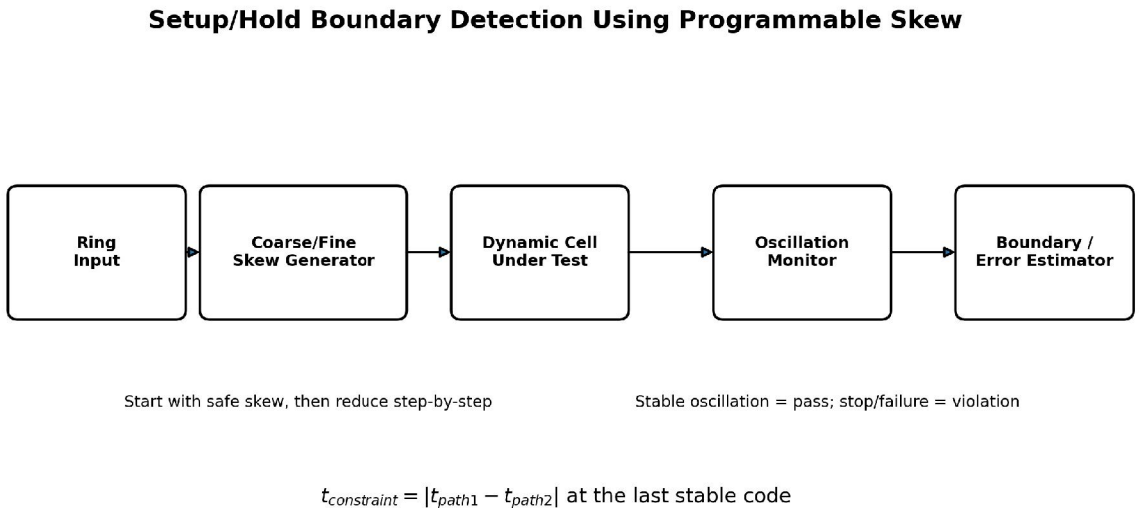

Fig. 3. Setup/hold boundary detection using a programmable coarse/fine skew generator.

For path p, the digitally controlled delay is modeled as

$$t_{\text{path},p} = C_p\, t_{\text{coarse}} + F_p\, t_{\text{fine}} + t_{0,p} \qquad (22)$$

The relative skew is

$$t_{\text{skew}} = |\, t_{\text{path},1} - t_{\text{path},2}\, | \qquad (23)$$

After matching or calibration removes the fixed offset, the timing constraint is estimated by

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$$t_{\text{constraint}} = | (C_1 - C_2)t_{\text{coarse}} + (F_1 - F_2)t_{\text{fine}} | \qquad (24)$$

A two-step search reduces test time. First, a coarse sweep locates the transition region. Second, a fine sweep around that region determines the minimum stable skew. Repeating the sweep in both directions identifies hysteresis or noise sensitivity.

3.9 Error-Rate Estimation Near the Timing Boundary

Near the setup/hold boundary, the ring may oscillate for a finite duration before a timing event fails to propagate. Since each cycle re-applies the critical relationship, the number of successful cycles before failure provides a direct estimate of the per-trial failure probability. If the ring period is T_RO and the observed duration before failure is T_fail, the number of trials is approximately n = T_fail/T_RO. A simple geometric-model estimator is

$$\hat{P}_{\text{error}} = \frac{1}{n} = \frac{T_{\text{RO}}}{T_{\text{fail}}} \qquad (25)$$

For repeated experiments r = 1,...,R with n_r successful trials before failure, a pooled estimate is

$$\hat{P}_{\text{error}} = \frac{R}{\sum_{r=1}^{R} n_r} \qquad (26)$$

This estimate assumes independent trials and a nearly constant failure probability. Correlated jitter, thermal drift, and low-frequency supply noise should be reported separately because they can produce burst failures.

3.10 Calibration and Measurement Uncertainty

Coarse and fine delay steps are calibrated using dedicated auxiliary rings. If T_c,m and T_c,m+1 are periods measured with adjacent coarse codes in a calibration ring containing N_c delay elements, the coarse step is

$$t_{\text{coarse}} = \frac{T_{\text{c},m+1} - T_{\text{c},m}}{N_{\text{c}}} \qquad (27)$$

The fine delay step is obtained similarly as

$$t_{\text{fine}} = \frac{T_{\text{f},n+1} - T_{\text{f},n}}{N_{\text{f}}} \qquad (28)$$

Suppose the standard deviation of the individual cell delay is σ_{d}, and n_{d}identical devices are averaged. For a confidence coefficient z, the error bound of the sample mean is

$$\text{EBM}_{\text{process}} = \frac{z\,\sigma_{\text{d}}}{\sqrt{n_{\text{d}}}} \qquad (29)$$

If the standard deviations of the through-mode and bypass-mode period measurements are $\sigma_{\text{TT}}$and σ_{TP}, respectively, and n_{p}periods are averaged, the corresponding delay uncertainty after differential extraction is approximately

$$\sigma_t = \frac{\sqrt{\sigma_{\text{TT}}^2 + \sigma_{\text{TP}}^2}}{N\sqrt{n_{\text{p}}}} \qquad (30)$$

The total uncertainty can be conservatively combined as

$$U_{\text{total}} = \sqrt{U_{\text{process}}^2 + U_{\text{jitter}}^2 + U_{\text{quant}}^2 + U_{\text{cal}}^2} \qquad (31)$$

where U_quant is counter or oscilloscope resolution and U_cal includes skew-step calibration error, output-buffer distortion, and mismatch between through and bypass paths.

3.11 Complete Experimental Procedure

Select the dynamic-cell timing arc and program idle inputs to sensitize the required path.
Select input-slew code, output-load code, supply voltage, and temperature.
Enable the phase generator and verify stable oscillation in bypass mode.
Measure period and positive/negative pulse widths over a fixed number of cycles in Mode P.

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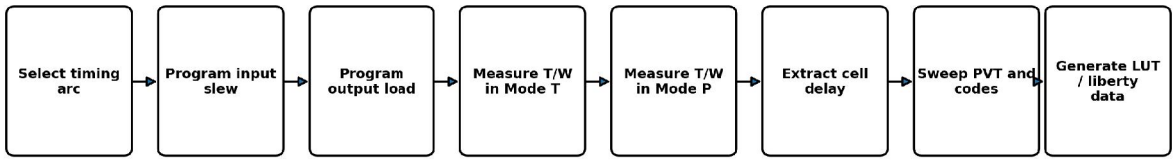
Switch to Mode T without changing the external conditions and repeat the measurement.
Apply (11), (18), or (19) to extract propagation delay.
For setup/hold characterization, sweep the coarse skew code, then refine with the fine code until the last stable setting is found.
Repeat measurements to estimate mean, standard deviation, confidence interval, and failure probability.
Sweep input transition and output load to populate a two-dimensional timing table.
Repeat across PVT corners and export characterized timing arcs into a liberty-compatible format.

Characterization and Liberty-Table Generation Flow



$LUT(i, j) = t_{arc}(S_i, C_j)$, repeated for voltage, temperature, and process corners

Fig. 4. End-to-end characterization flow for lookup-table and liberty-data generation.

3.12 Verification and Implementation Considerations

At RTL or behavioral level, the architecture can be verified using a dynamic-cell model, programmable delay elements, a phase generator, mode-control logic, a period/pulse-width counter, and a self-checking testbench. Delay statements are appropriate for architectural simulation but are not synthesizable. A physical ASIC implementation requires custom transistor-level dynamic cells, characterized tunable delay elements, careful shielding of high-impedance dynamic nodes, matched routing for through and bypass paths, and an output divider or buffer that minimizes duty-cycle distortion.

For FPGA demonstration, a logical ring can be used only with device-specific LUT or carry-chain primitives and preservation constraints. The FPGA model is useful for demonstrating period measurement, configuration control, and test automation, but it does not reproduce transistor-level dynamic-node effects. For silicon measurement, the output should be observed through a calibrated divider or a low-skew buffer, and supply/temperature sensors should be logged with every timing sample.

IV. RESULTS AND DISCUSSION

This section is intentionally reserved for insertion of simulation or silicon measurement results. The following structure is recommended so that the reported data directly supports the proposed methodology.

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4.1 Functional and Oscillation Waveforms

Insert waveforms showing phase-generator outputs, block clocks, ring outputs, precharge/evaluation sequencing, through/bypass mode operation, and the failure of oscillation at a setup/hold violation. Discuss whether each dynamic node is reset before the next evaluation and whether the measured duty cycle is stable over the observation window.

4.2 Propagation-Delay Results

Report T_T, T_P, DeltaW+, DeltaW-, extracted t_d2q, t_clkr2q, and t_clkf2q. Compare transistor-level simulation, post-layout simulation, and measured values when available. Include percentage deviation using

$$\textbf{Deviation}(\%) = \frac{|\, \boldsymbol{t}_{\textbf{measured}} - \boldsymbol{t}_{\textbf{reference}} \,|}{\boldsymbol{t}_{\textbf{reference}}} \times \mathbf{100} \qquad (32)$$

4.3 Slew-Load Lookup Tables

Provide two-dimensional tables or surface plots for each timing arc versus input transition and output capacitance. Confirm that delay generally increases with load and degrades for slower input transitions. Discuss any non-monotonic behavior caused by keeper contention or charge sharing.

4.4 Setup/Hold and Error-Rate Results

Report the calibrated coarse and fine steps, last stable code, first failing code, repeated boundary measurements, standard deviation, and estimated failure probability. A useful summary table should include timing arc, safe skew, boundary skew, mean constraint, confidence interval, and number of repeated trials.

4.5 PVT and Statistical Analysis

Show the impact of supply voltage and temperature and, when available, process corners or multiple dies. Calculate coefficient of variation

$$\mathrm{CV}(\%) = \frac{\sigma_t}{\mu_t} \times 100 \qquad (33)$$

Synthesized Device View

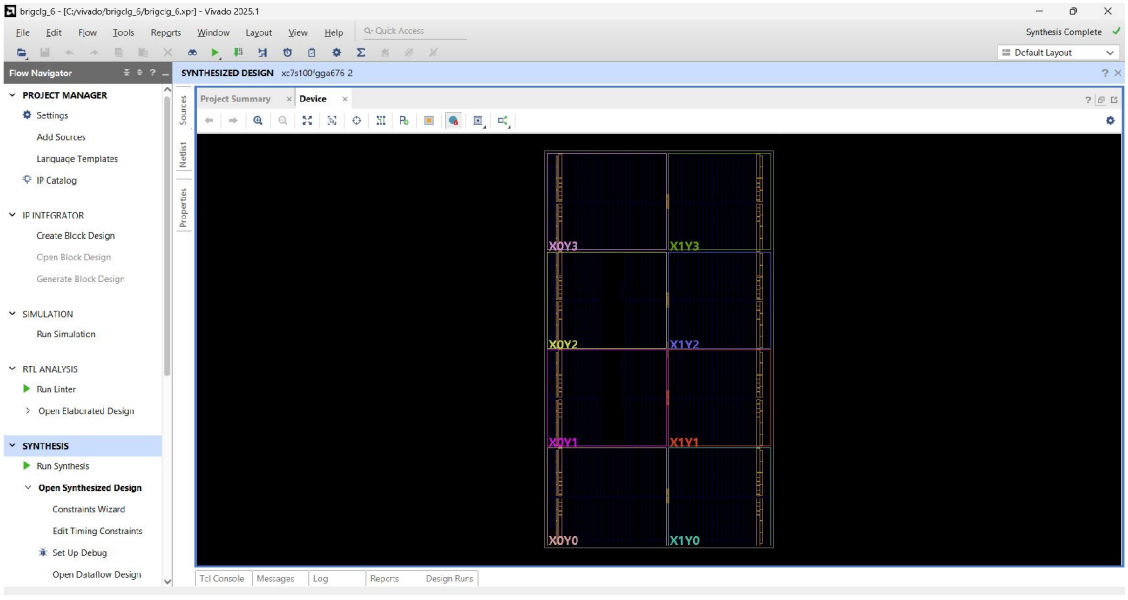

Figure 1. Synthesized device view of the target FPGA.

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The synthesized device view shows that the project was opened successfully for the xc7s100fgga676-2 FPGA. The device floorplan is divided into the available clock regions, identified in the display as X0Y0 to X1Y3. At this stage, the image represents the available FPGA fabric after synthesis rather than a final placed-and-routed utilization map.

The successful opening of the synthesized design confirms that the RTL hierarchy and inferred logic are compatible with the selected target. Final placement density, routing delay, and physical ring-oscillator behavior must be evaluated only after implementation, because synthesis alone does not determine the exact physical location or routing of delay-sensitive elements.

Synthesis Result

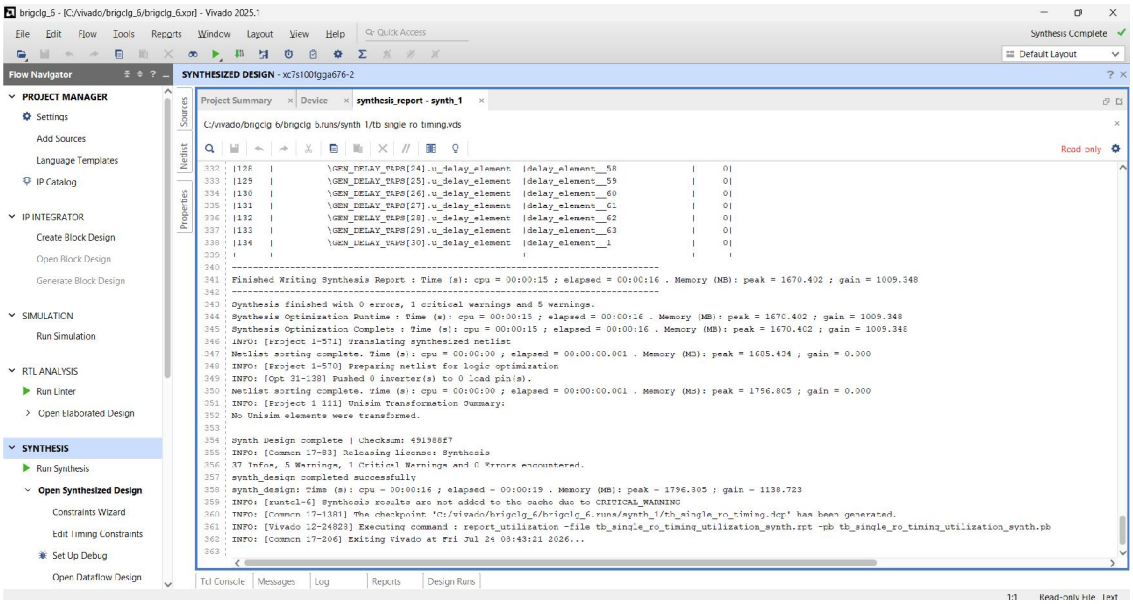

Figure 2. Vivado synthesis report showing successful synthesis completion.

The synthesis report shows that synthesis finished with zero errors. Vivado reports one critical warning and five warnings, while the final synthesis command completed successfully and generated the design checkpoint file tb_single_ro_timing.dcp. The report also shows a synthesis elapsed time of approximately 19 seconds for the displayed run.

The absence of synthesis errors demonstrates that the Verilog hierarchy is structurally acceptable to Vivado. The remaining critical warning must nevertheless be reviewed before hardware programming. In ring-oscillator designs, critical warnings commonly arise from combinational-loop handling, unconstrained clocks, testbench selection, or timing constraints. Such warnings should not be ignored because synthesis success alone does not guarantee correct physical oscillation on the FPGA.

The report further indicates that no Unisim elements were transformed. This suggests that the displayed synthesis run is primarily based on RTL-inferred logic rather than a design dominated by explicit vendor primitives. For a physical FPGA ring oscillator, vendor-specific LUT or carry-chain primitives and preservation attributes are typically required to prevent optimization and to obtain a stable, repeatable physical delay path.

Power Estimation Result

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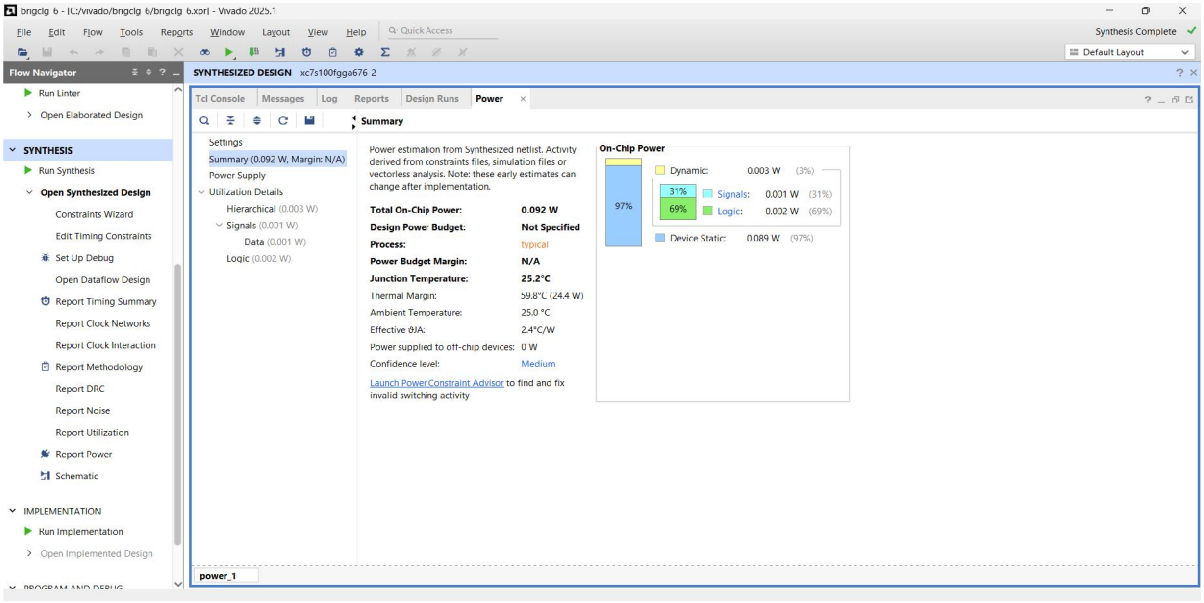

Figure 3. Post-synthesis power-estimation summary.

The Vivado power report estimates a total on-chip power of 0.092 W. The device static component is 0.089 W, corresponding to approximately 97% of the total estimate, whereas the dynamic component is 0.003 W, or approximately 3%. Within the dynamic component, signal power is shown as 0.001 W and logic power as 0.002 W.

The estimated junction temperature is 25.2 °C for an ambient temperature of 25.0 °C. The reported thermal margin is 59.8 °C, corresponding to 24.4 W, and the effective junction-to-ambient thermal resistance is 2.4 °C/W. These results indicate that the synthesized digital model has a very small estimated thermal burden under the activity assumptions used for this report.

The report explicitly states that activity was derived from constraints, simulation files, or vectorless analysis and that early estimates can change after implementation. Because a ring oscillator can have continuous high-frequency switching, the final dynamic power may be higher than this early estimate if realistic oscillation activity is not represented. A post-implementation power report using switching-activity data from simulation is therefore recommended.

RTL Schematic Result

The elaborated RTL schematic confirms the organization of the proposed architecture. Five delay-measurement blocks are visible on the right side of the main design hierarchy. Two setup/hold-measurement blocks are placed on the left and are controlled by independent coarse-code, fine-code, and measurement-mode inputs. A phase-generator block receives ring-node feedback and produces the clock-phase outputs required for coordinated operation.

The schematic also includes ring-start logic, external data controls a_ext, b_ext, and c_ext, the through/bypass mode control, the delay-measurement input selector, and the ring-oscillator output. Vivado reports 10 cells and 59 nets in the elaborated view. The interconnection confirms that the major methodology components have been integrated into one top-level structure instead of being implemented as unrelated test modules.

The presence of the phase generator is especially important because ordinary ring oscillators cannot directly support dynamic circuits that require precharge and evaluation. The schematic demonstrates that feedback and phase-control paths are available to coordinate the repeated operation of the delay and setup/hold blocks.

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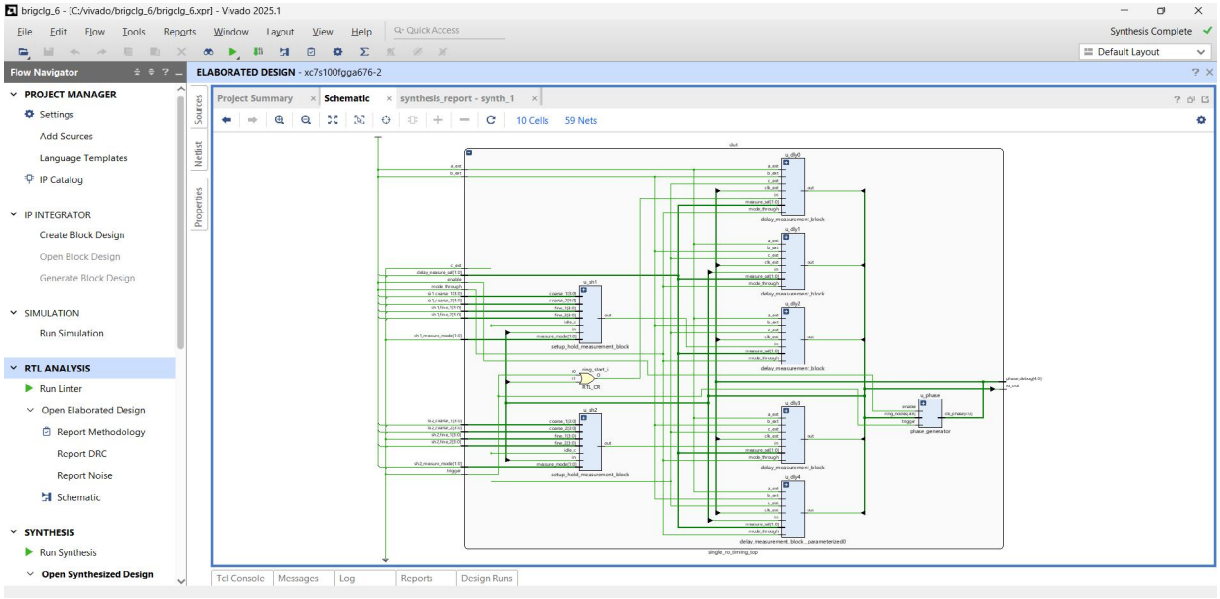

Figure 4. Elaborated RTL schematic of the proposed test architecture.

Behavioral Simulation Result

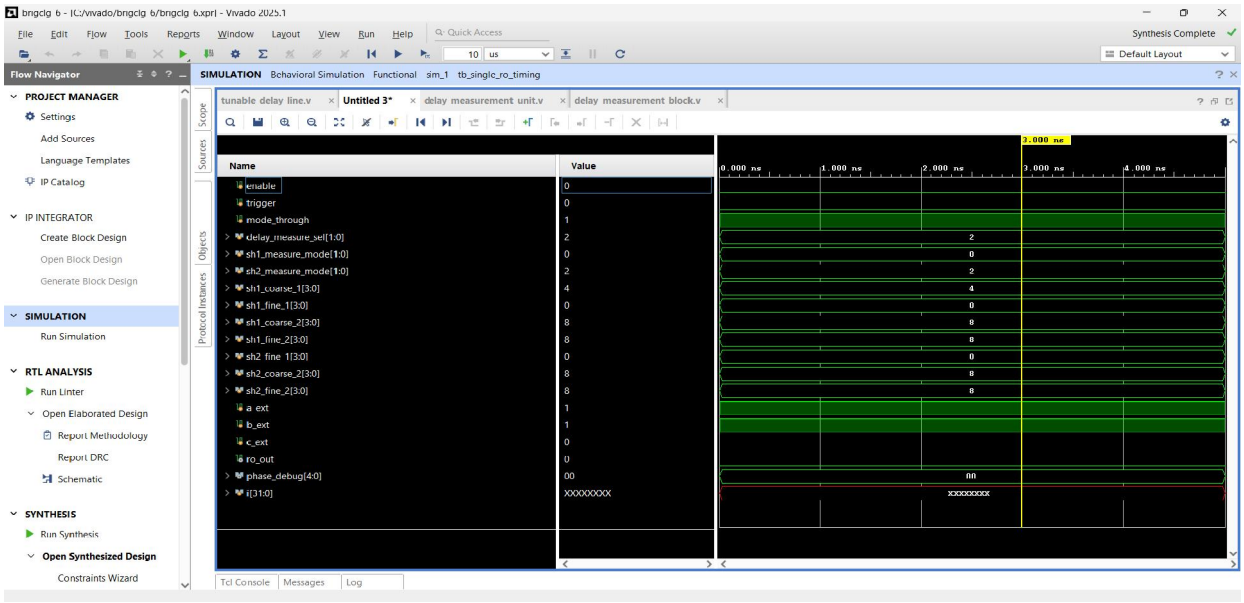

Figure 5. Behavioral simulation waveform at the initial idle condition.

The behavioral simulation screenshot shows the design at approximately 3 ns in an initial idle condition. The enable and trigger signals are both low, while mode_through is high. The selected delay-measurement input code is 2. The first setup/hold measurement mode is 0 and the second is 2. The coarse and fine controls shown in the waveform include values such as 4, 0, and 8, while the external data inputs are a_ext = 1, b_ext = 1, and c_ext = 0.

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Because enable = 0 and trigger = 0 at the displayed instant, the phase output remains 00 and ro_out remains at logic 0. The internal signal i[31:0] is displayed as unknown. This unknown value is consistent with an uninitialized or inactive counter/state signal during the idle interval and does not, by itself, demonstrate a functional failure of the design.

To demonstrate successful oscillation and timing extraction, the simulation should be extended beyond the idle interval by asserting enable, applying the trigger pulse, and observing repeated transitions in ro_out and phase_debug. Through-mode and bypass-mode waveforms should then be captured over multiple cycles so that the period difference, pulse-width difference, and setup/hold boundary can be calculated using the project equations.

V. CONCLUSION

A complete methodology for post-silicon timing characterization of dynamic logic has been presented. The proposed single-ring architecture combines multi-phase control, cascaded delay blocks, setup/hold blocks, through/bypass switching, programmable slew and load tuning, and coarse/fine skew generation. Differential period and pulse-width equations isolate the delay of the dynamic cell from common test-structure parasitics, while repeated circulation converts setup/hold verification into a stable-oscillation boundary problem. The same repeated operation also supports estimation of timing-failure probability near the critical boundary.

The methodology is suitable for constructing liberty lookup tables because it measures timing across input transition, output capacitance, voltage, temperature, and process conditions. It can be extended to minimum clock-pulse-width measurement, dynamic comparators, latches, flip-flops, memory peripherals, and other circuits that respond to a specific edge and require controlled reset. Future implementation work should focus on custom-layout matching, automated digital calibration, integrated counters, adaptive search of timing boundaries, aging-aware characterization, and silicon-to-model correlation across multiple dies.

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