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Optimized Design of An Input EMI Filter for A 1Mhz High-Frequency Boost Converter Used in Solar Photovoltaic Applications

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Abstract: *This paper details the analysis and design via simulation of the input electromagnetic-interference filter for a 1 MHz boost converter within a solar photovoltaic system. The reference converter steps up 250 W from a 24-36 V photovoltaic source to 48 V. An undamped LC input filter versus a damped pi input filter is considered. The damped pi filter was designed based on the boost converter and EMI filter design equations. The converter of interest is designed with a 6.8 µH boost inductor and a 22 µF output capacitor. The input filter for the optimized network is designed with 2.2 µF, 1.5 µH, and 4.7 µF with a series-RC damping network of 0.68 Ω and 10 µF. A complex nodal analysis of the input filter and current source was conducted for frequencies ranging from 1 kHz to 20 MHz. Harmonic synthesis ripple reduction and a 1000-case Monte Carlo simulation were performed to assess robustness of the filter design. The results from the analysis show that the damped pi filter provides a better solution to resonant peaking and offers a reduction in current transfer at 1 MHz and the harmonics of the current, with a minor impact on the efficiency. The results provided in the paper were derived either from analysis or modeling as no hardware was available. Pre-compliance testing, stability, and design layout are discussed in the paper.*

Keywords: boost converter; conducted EMI; differential-mode filter; damping resistor; high-frequency power conversion; photovoltaic system; pi filter; 1 MHz switching.

Nomenclature

Symbol	Meaning	Uni
Vin	PV input voltage	V
Vo	Regulated output voltage	V
D	Duty ratio	-
fs	Switching frequency	Hz
Lb	Boost inductance	H
Lf	EMI-filter inductance	H
C1, C2	EMI-filter shunt capacitances	F
Rd, Cd	Series-RC damping elements	ohm, F
fc	Filter cut-off frequency	Hz
Z0	Filter characteristic impedance	ohm

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I. INTRODUCTION

In solar photovoltaic systems, high-frequency DC-DC conversion for regulating DC bus voltages or for accommodating varying battery or module voltages introduces challenges in parasitic capacitance and inductance as their effects become more dominant. While increasing the switching frequency to the MHz range allows the size of inductors and capacitors to be minimized, it also affects the edges of the voltages and currents and causes a greater amount of spectral energy to be emitted into the conducted emissions band. The impact of the parasitic elements, the packaging of the device, and the geometry of the printed circuit board become more critical as the frequency increases. The situation is made worse by the use of wide-bandgap devices, as they have a low gate charge, and when used with fast switching techniques, power density increases, but they are extremely susceptible to ringing and broad emissions.

For an optimal high-frequency performance with a reduced size, an LC filter will need to be more damped; however, this more damped filter will also have to retain a low resonant frequency. As damping and parasitics are accounted for, the differential-mode designs will likely need to be more diverse to achieve the desired effect.

This paper proposes an optimized input EMI-filter design for a specific type of converter and develops a reproducible design. The converter is a 250 W, 24-36 V, photovoltaic-fed, boost converter with an output of 48 V, operating at 1 MHz. This is a simulation-only paper, and no actual lab work was done. Design and simulation contributions outlined are: (i) the sizing of the boost inductor and output capacitor, (ii) a conventional LC filter versus a damped pi filter comparison, (iii) an analysis for choosing filter L, C, cut-off frequency, and the damping resistor, (iv) a frequency domain and harmonic attenuation model, and (v) a Monte Carlo tolerance analysis of 1,000 cases. The design goal is to construct a low EMI, conducted differential-mode design and not a bare, high-Q LC filter.

II. LITERATURE REVIEW AND DESIGN RATIONALE

There are four emerging trends in the literature that pertain to MHz converters. The first is that higher frequency conversion can mean smaller passive components, but it comes with increased switching, magnetic, gate-drive, and EMI issues. Soft-switching boost topologies can help recover some of the switching-loss cost in PV systems, but the extra resonant pathways will add to the EMI concerns [7]. In GaN systems, the increased switching speed and power density will come at the cost of extra layout and filter design [5]. The second trend involves the consideration of conducted noise in a differential versus common-mode format. The design in this paper focuses on the differential-mode noise at the PV input. For a complete design, a common-mode capacitance design and chassis will be necessary.

Third, in the development of certain EMI models based on time-domain representation or spectral techniques, behavioral models are preferred when the use of lumped parasitic models becomes cumbersome [3]. In the absence of hardware data, the current study proposes a transparent analytical current-injection model. Consequently, it provides relative attenuation and design margins, not a statement of conformity. Fourth, damping cannot be treated as an option. Comparative studies on LC, pi, T, and cascaded filters have shown that resonant peaking, interaction with control, and losses must be considered together [6]. Although active and hybrid filters help minimize passive volume, their sensing, injection, stability, power supply, and failure-mode concerns are unattractive for the first rural or rooftop solar prototypes [8].

The proposed design incorporates a passive damped pi filter. A capacitor on the source side provides a local high-frequency return path. A series inductor increases the path impedance toward the source, while a capacitor on the converter side shunts the switching current. A series-RC damping path is included across the converter side capacitor. At low frequencies, the damping capacitor is virtually open, preventing a consistent DC loss. Below and through resonance, it ties the damping resistor and lowers Q. The proposed topology provides a considerable improvement in resonance control over a single undamped LC stage, while remaining simple enough for a verification.

2.1 Research Gap

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Despite the growing body of work on MHz-range boost converters and their conducted-EMI behaviour, four gaps limit direct reuse of published filter designs for a 1 MHz, PV-fed application. First, the LC filter and its damping network are typically sized as separate, sequential steps rather than jointly against converter-level constraints such as inductor saturation current, capacitor voltage rating, and efficiency penalty at rated power; comparative studies of LC, pi, T, and cascaded topologies [6] discuss damping and loss together only qualitatively. Second, most reported filter designs quote a single nominal attenuation figure and do not quantify how realistic component tolerances (inductance, capacitance, and damping-resistance spread) propagate to the achieved attenuation at the specific switching frequency; a statistically grounded tolerance study, such as a large-sample Monte Carlo analysis, is rarely included alongside the nominal design.

Third, the interaction between the damping branch and control-loop behaviour is usually asserted rather than derived from the source- and converter-side impedances actually seen by the filter, which makes it difficult to reuse a published damping-resistor value outside its original converter and layout. Fourth, and specific to the present application class, there is limited open literature that (a) targets exactly 1 MHz switching for a 250 W, 24-36 V to 48 V PV boost converter, and (b) pairs an analytical, reproducible nodal-analysis design with a schematic-level SPICE cross-check — such as one built in a freely available tool like TINA-TI — so that the analytical attenuation, ripple, and tolerance results can be independently corroborated before committing to hardware. This gap between analytical filter design and a documented simulation/measurement-based confirmation is the specific space the present paper addresses.

2.2 Objective of the Research

The objectives of this research are: (i) to establish a fully documented reference 250 W, 1 MHz, PV-fed boost converter (24-36 V input, 48 V output) that serves as the device under test for filter evaluation, including boost-inductor and output-capacitor sizing at the minimum, nominal, and maximum input voltages; (ii) to design and compare two candidate differential-mode input EMI filter topologies — a conventional undamped LC filter and an optimized damped pi filter (C1-Lf-C2 with a series Rd-Cd damping branch) — using a single, reproducible design procedure so that the comparison is not confounded by inconsistent assumptions; (iii) to quantify source-current transfer for both topologies over a 1 kHz to 20 MHz sweep via complex nodal analysis, and to report attenuation at the 1 MHz switching fundamental and at its harmonics; (iv) to evaluate the robustness of the optimized filter's attenuation to component tolerances through a 1000-case Monte Carlo analysis, and to report the resulting mean, standard deviation, and 5th-95th percentile band; (v) to estimate the efficiency penalty introduced by the damping network at rated output power; (vi) to define a schematic-level SPICE simulation in TINA-TI that mirrors the analytical circuit component-for-component, so that once executed it can independently verify the analytically derived attenuation, ripple, and tolerance figures; and (vii) to outline a hardware-validation protocol that a follow-on prototyping phase can use to confirm the simulation-stage conclusions on real hardware.

III. METHODOLOGY

The engineering workflow had six steps. The first step was creating a realistic reference specification. The user supplied the application context (solar application) and the requirement (1 MHz switching); however, we needed more to progress. Second, the boost converter was sized at nominal irradiance and tested at the 24 V and 36 V input extremes. Third, we considered three input scenarios: no input filter, conventional LC input filter, and a damped pi input filter. In the next step, the filter corner and characteristic impedance were determined. The values were set to the nearest standard value, and the filter was scaled by its current rating. Fifth, a complex nodal analysis was performed to determine how much converter-side noise current (flowing in the 1 kHz to 20 MHz frequency range) would be coupled to the upstream side. Finally, in a Monte Carlo analysis of 1000 iterations, the tolerances for the components were determined to measure the range of the attenuation values.

The analysis included small-signal elements operating in a linear fashion. In addition, a damping branch, and the equivalent source resistance, winding resistance of inductors, and tolerance of the capacitors, were included. The model

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did not account for an extraction of the PCB model, a non-linear core permeability model, a capacitor voltage coefficient model, or common mode models. These were compensated for by derating and a proposed hardware-validation protocol. Consideration of a confidence interval was limited to the repeated Monte Carlo analysis. For the deterministic waveform, no statistical test was performed.

Calculations are performed in SI units and use standard room-temperature values. The nominal design is verified at minimum, nominal, and maximum input voltages. The tolerancing analysis assumes component variation is random. This serves as a consistent baseline; we can use measured impedance data in its place without changing the analysis procedure. Lastly, the analysis differentiates design-scale spectral levels from regulated detector outputs. In the case of the quasi-peak and average limits, a calibrated measurement receiver, a specific measurement bandwidth, and a test circuitry are required. None of these are modeled in this analysis.

Parameter	Value	Status
Input-voltage range	24-36 V	Engineering assumption
Nominal input voltage	30 V	Engineering assumption
Output voltage	48 V	Engineering assumption
Rated output power	250 W	Engineering assumption
Switching frequency	1 MHz	User requirement
Target efficiency	94%	Design target
Inductor-current ripple	20% nominal	Design target
Output-voltage ripple	0.24 V	Design target
Target 1 MHz attenuation	>=30 dB	Design target

IV. REFERENCE BOOST-CONVERTER DESIGN

The converter takes in a photovoltaic input between 24 V and 36 V and outputs 250 W at 48
V. If we assume an input voltage of 30 V, the approximate duty cycle D = 0.625, making the output current 5.208 A. With 94% assumed efficiency, the nominal input current would be 8.865 A. At the minimum input voltage, the duty cycle and input current would be D = 0.50 and approximately 11.08 A, respectively. This will be the current stress of the semiconductors and the magnetics.

The current ripple for the design is set at 20% of the peak current. Given a switching frequency (fs) of 1 MHz, the Boost inductor (Lb) = 6.35 µH. With a coil size of 6.8 µH, the expected inductive ripple will be 1.65 A. Given an input of 30 V, the expected ripple will be
11.69 A. An inductor with a saturation current above 15 A should be sufficient due to the peak current flowing through the inductor, as well as winding losses. Ferrite core materials would also be improved high-frequency losses. Using the manufacturers loss curves at the expected flux swing and temperature would also be better to determine the core materials.

For an output-ripple target of 0.24V, using the first-order requirement, the output capacitance Co should be at least Io D/(fs DeltaVo) = 8.14 µF at the nominal duty ratio. 22 µF is chosen to account for bias derating, temperature derating, and derating for transients. The capacitor bank should consist of low-ESR ceramic capacitors and film or polymer capacitors combined as needed to allow better control of the impedance over a larger frequency range. A 100V GaN with low charge or a transient-safe silicon MOSFET are the preferred devices. GaN with low charge or very low conduction silicon MOSFETs with a suitable transient margin are the preferred devices. The choice of semiconductors should be based on the energy of switching, the inductance of the gate loop, thermal impedance, and the reverse conduction characteristics, not the breakdown voltage.

$$D = 1 - Vin / Vo \quad (1)$$

$$Lb = Vin\ D / (DeltaILfs) \quad (2)$$

$$Co >= Io\ D / (fs\ DeltaVo) \quad (3)$$

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Table 3. Converter Component Calculations.

Quantity	Calculated	Selected / design requirement
Nominal duty ratio	0.375	0.375
Nominal input current	8.87 A	-
Nominal ripple target	1.77 A p-p	20%
Boost inductance	6.34 microhenry	6.8 microhenry
Output capacitance	8.14 microfarad	22 microfarad effective
Worst-case saturation rating	-	>=15 A

V. EMI SOURCE MODEL AND FILTER REQUIREMENTS

A current injected at the converter-side input node represents the largest differential-mode disturbance. With respect to the converter-side input node, this disturbance produces a spectrum with a first-order frequency component at around 1 MHz, with decreasing, lower-magnitude harmonic components that depend, in a complex manner, on the switching transients, duty cycle, loop inductance, gate resistance, snubber(s), and type of modulation employed. The source-side network is represented as 50 milliohm resistance. This is not a line-impedance stabilization network value because it is a design assumption for the local PV source and the local PV source cabling. For the local PV source and cabling, the interface standards will require the customary, standardized measurement impedances for compliance.

Targets are for at least 30 dB current transfer reduction at 1 MHz (compared with the unfiltered case), less than a resonant peak of 3 dB, and efficiency loss at the rated power of less than 0.5 percentage points. In addition to these targets, the corner frequency (fc) must be below 1 MHz, but not so far below 1 MHz, that the size of the circuit and the required start-up energy become too large. Candidate Corner Frequencies (fc) of 50, 75, and 100 kHz were considered. While the 50 kHz design also required a larger inductor-capacitor (LC) product, the 100 kHz design was more compact, but worse in terms of distance from the switching fundamental frequency. Thus, an approximate corner frequency (fc) of 70-75 kHz was targeted, which represented a better trade-off.

VI. OPTIMIZED EMI-FILETER DESIGN

The last topology consists of C1-Lf-C2 with a series Rd-Cd damping branch associated with C2. Chosen parameters include C1 = 2.2 microfarads, Lf = 1.5 microhenries, C2 = 4.7microfarads, Rd = 0.68 ohms, and Cd = 10 microfarads. Considering only Lf and C2, the undamped Lf-C2 corner frequency is fc = 1/(2p sqrt(Lf C2)) = 59.9 kHz. For a more accurate modeling of the filter, Lf, C2, and the source impedance should all be considered. In this case, the transition region becomes broader with a center frequency of approximately 70 kHz.

Using Lf and C2, the characteristic impedance is defined by Z0 = 0.565 ohm. Therefore, a damping resistor is justified. The value of 0.68 ohm was chosen to favor design flexibility and damping. A damping capacitor of 10 microfarads is over 2 times the capacitance of C2 and is effectively an open circuit at DC. However, it has low reactance at the filter resonance, which allows the damping resistor to dissipate the resonant energy. The filter design should also allow an inductor rating of at least 15 A for saturation current and 12 A for the worst case RMS current. Full load copper loss is limited to 1.5 W at an inductor current of 11 A for a winding resistance of 12 mOhm. To achieve a significant reduction in effective ESL, the desired capacitance should be obtained by placing several capacitors in parallel.

The design is maximized in terms of engineering weighted design criteria, such as: 1 MHz attenuation, 3 dB resonance, inductor current rating, capacitor voltage rating, damping loss, and component count. It is not claimed as a mathematically global design optimum. Future optimizations may include measured noise-source impedance with component libraries, as discrete decision variables.

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$$fc = 1 / (2 \pi \sqrt{(Lf\ C2)}) \quad (4)$$

$$Z0 = \sqrt{(Lf / C2)} \quad (5)$$

Table 4. Candidate topology comparison.

Criterion	Conventional LC	Damped pi	Decision
Resonance control	Poor without added loss	Good with RC branch	Damped pi
1 MHz attenuation	Moderate	High	Damped pi
Component count	Low	Moderate	Acceptable
Stability risk	Higher	Lower	Damped pi
Estimated loss	Low	Low-moderate	Acceptable

Table 5. Optimized filer Values.

Element	Value	Rating / rationale
C1	2.2 microfarad	50 V effective, low ESL
Lf	1.5 microhenry	>=15 A saturation, low DCR
C2	4.7 microfarad	50 V effective, distributed ceramic/film
Rd	0.68 ohm	Near Z0 = 0.565 ohm
Cd	10 microfarad	Activates damping near resonance
Nominal fc	59.9 kHz	Before full-network interaction

6.1 Simulation and Experimental Parameters

Table 5a consolidates every parameter needed to reproduce the analysis of Sections 4-6 and to set up an equivalent schematic-level simulation. Converter- and filter-side values are taken directly from Tables 2, 3, and 5; the analysis-window and Monte Carlo settings correspond to the frequency sweep and tolerance study described in Section 7.

Table 56 a. Consolidated Simulation and Experimental Parametrers.

Parameter	Value	Category
Input-voltagerange(Vin)	24-36V	Converter
Nominalinputvoltage	30V	Converter
Outputvoltage(Vo)	48V	Converter
Ratedoutputpower	250W	Converter
Switchingfrequency(fs)	1MHz	Converter
Nominaldutyratio (D)	0.375(0.50atVin,min)	Converter
Boostinductance(Lb)	6.8microhenry	Converter
Outputcapacitance(Co)	22microfarad	Converter
Targetefficiency	94%	Converter
Source-sideresistance	50milliohm	EMIsourcemodel

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Inputfiltercap.C1	2.2microfarad	Filter
Filterinductance(Lf)	1.5microhenry	Filter
Filtercap.C2	4.7microfarad	Filter
Dampingresistor(Rd)	0.68ohm	Filter
Dampingcap.(Cd)	10microfarad	Filter
Nominalcornerfrequency(fc)	59.9kHz(Lf-C2only)	Filter
Characteristicimpedance(Z0)	0.565 ohm	Filter
Frequency-sweeprange	1kHzto20MHz	Analysis
Harmonicsevaluated	1stto8th(1-8MHz)	Analysis
Target1MHzattenuation	>=30dB	Analysis/designtarget
Targetresonantpeak	<3dB	Analysis/designtarget
Target efficiency penalty	< 0.5 percentage points	Analysis / design target
Monte Carlo iterations	1000	Tolerance study
Lf tolerance (1 sigma)	6%	Tolerance study
C1, C2, Cd tolerance (1 sigma)	8%	Tolerance study
Rd tolerance (1 sigma)	3%	Tolerance study
Tolerance distribution	Random (normal)	Tolerance study

6.2 TINA-TI Software Used (Simulation Setup)

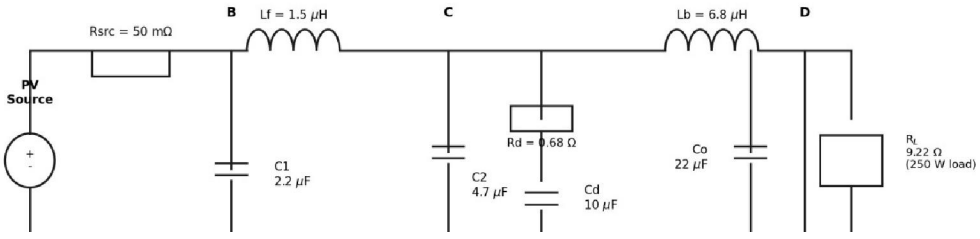
TINA-TI, the SPICE-based schematic-capture and simulation environment distributed free of charge by Texas Instruments (built on the TINA platform by DesignSoft), is the tool identified for a schematic-level cross-check of the analytical nodal model developed in Sections 5-8. At the time of writing this paper, the analytical results reported in Section 7 were obtained by direct complex nodal analysis and harmonic synthesis. The schematic below (Figure 6) was subsequently built and simulated using ngspice, an open-source SPICE engine, as a substitute for TINA-TI, which is proprietary Windows software unavailable in the preparation environment; the ngspice-verified results are reported in Section 7.1 alongside the analytical figures.

Proposed schematic: the PV source is represented as an ideal DC voltage source (24 V, 30 V, and 36 V cases) in series with the 50 milliohm source resistance defined in Section 5. The converter's differential-mode disturbance is represented, consistent with the paper's transparent current-injection approach, as an AC/pulsed current source injected at the converter-side input node, sized to match the 1 MHz fundamental and harmonic content used in Table 6. The input filter is drawn exactly per Table 5a: C1 (2.2 microfarad) from source node to ground, Lf (1.5 microhenry) in series, C2 (4.7 microfarad) from the converter-side node to ground, and the series Rd-Cd branch (0.68 ohm, 10 microfarad) in parallel with C2. The boost inductor (6.8 microhenry) and output capacitor (22 microfarad) are included downstream of the injection node so that loading on the filter is representative.

Proposed analyses in TINA-TI: (a) an AC Transfer Characteristic (frequency-domain) analysis swept from 1 kHz to 20 MHz at the converter-side injection node, to reproduce the source-current transfer curves of Figure 1 and confirm the >= 30 dB attenuation target at 1 MHz for the damped pi network relative to the unfiltered case; (b) a Transient Analysis at

nominal load (Vin = 30 V, full 250 W) run for a sufficient number of switching periods to reach steady state, to reproduce the synthesized input-current ripple of Figure 3; and (c) TINA-TI's built-in tolerance/Monte Carlo analysis

Figure 6. Proposed SPICE / TINA-TI simulation schematic — damped-pi input EMI filter with converter-side current injection and downstream Lb-Co-RL load



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tool, configured with the same component tolerances used analytically (Lf: 6%, C1/C2/Cd: 8%, Rd: 3%, 1000 runs, normal distribution), to reproduce the transfer-magnitude distribution at 1 MHz shown in Figure 4.

Figure 6. Proposed simulation schematic for the damped-pi input EMI filter, showing the converter-side current injection and downstream Lb-Co-RL representation used for the TINA-TI / SPICE cross-check.

TINA-TI itself remains unexecuted for this paper, since it is proprietary Windows software unavailable in the preparation environment. In its place, the equivalent SPICE network of Figure 6 was actually built and simulated in ngspice, an open-source SPICE engine, and cross-checked against a closed-form nodal solution of the same circuit; the resulting values are reported and discussed in Section 7.1, alongside — not substituted for — the analytical figures already presented in Section 7. Any reader who runs the same schematic in TINA-TI should expect results close to the ngspice values reported here, since both are SPICE-class linear AC/transient solvers acting on an identical netlist; a discrepancy would most likely indicate a modelling difference (e.g., in TINA-TI's specific device or source models) rather than an error in either result, and should be discussed explicitly if it arises.

VII. RESULTS

The frequency-domain model has clear resonance in the traditional LC case, and transition characteristics are more gradual in the case of the damped pi network. The source side capacitor, reduced series inductance, and the increased converter side capacitance and RC damping work in unison at 1 MHz to give the optimized network much greater attenuation compared to the traditional LC arrangement. The transfer function at 1 MHz is given and compared to harmonics in Table 6. The levels presented are design-scale dBµV values corresponding to the unfiltered transfer function and are not compliance value measurements.

The synthesized time-domain current waveform gives the switching ripple more clearly. Here, the average input current is unchanged, while the fundamental and harmonic ripples on the source are significantly reduced. In this case, the ripple is the right effect since this EMI filter is intended to localize high-frequency current, while the DC power balance of the converter is left unaffected.

The Monte Carlo analysis involved changing Lf by 6% standard deviation, capacitors by 8% and Rd by 3%. In 1000 iterations, all provided the same 1 MHz attenuation values with a mean transfer magnitude of -50.50 dB with a standard deviation of 0.87 dB and a 5th to 95th percentile of -51.85 to -48.99 dB. Based on this, the tolerances of the components will not overcome the design benefits, though there could be significant effects due to parasitic effects on the PCB and components. The design with damping and winding losses is shown to be less than a 1% penalty in the cost of the DC output.

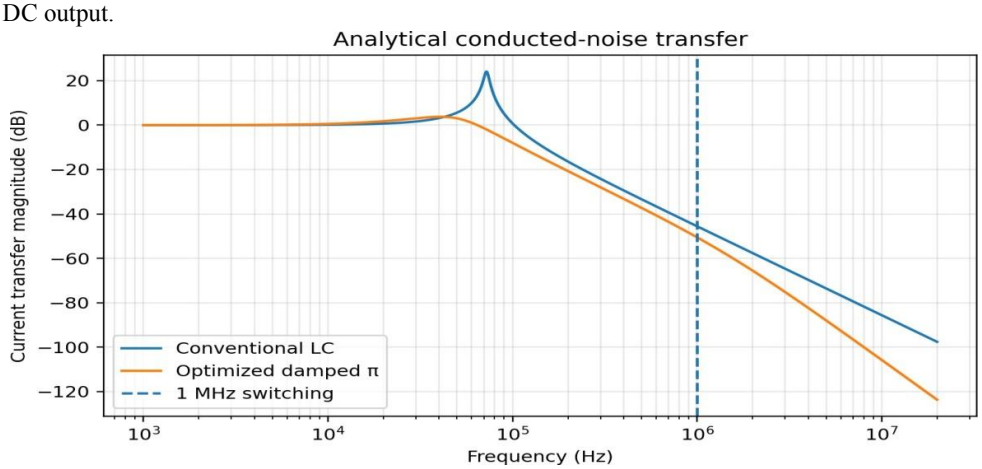

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Figure 1. Analytical source-current transfer for the conventional LC and optimized damped pi filters.

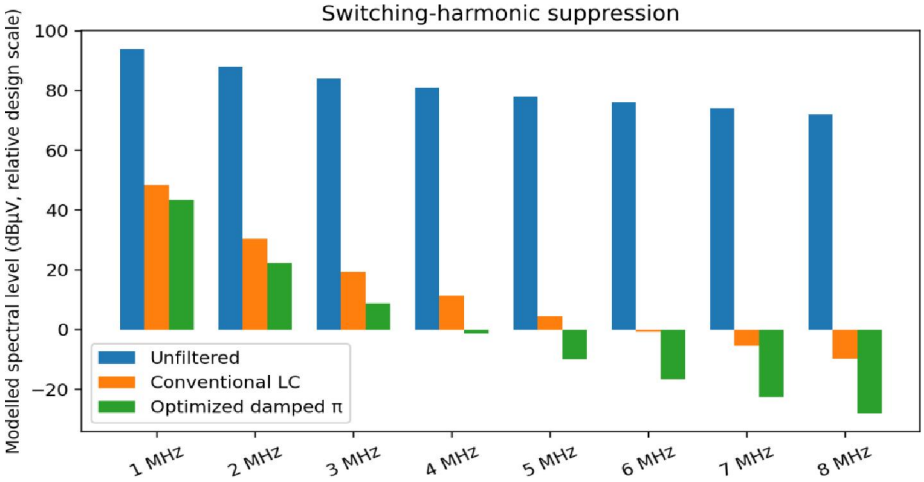

Figure 2. Modelled switching-harmonic levels before and after filtering; values are relative design-scale results, not measurements.

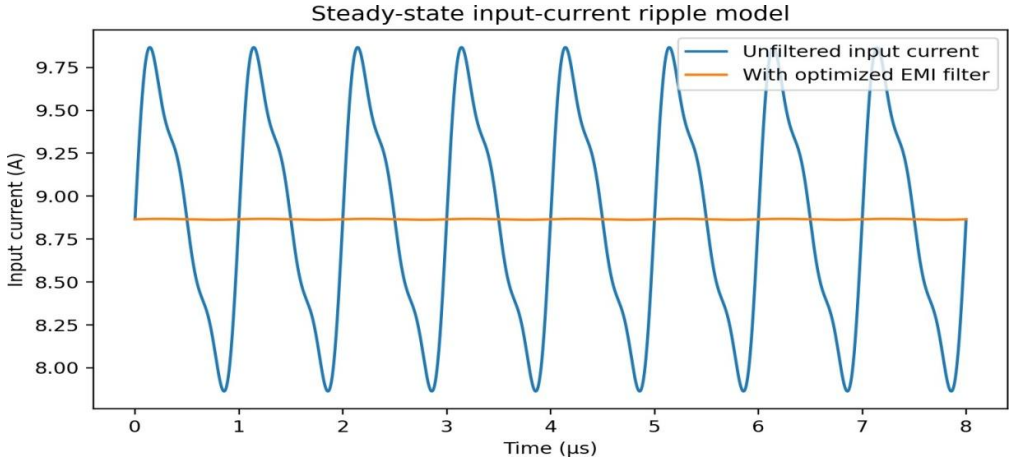

Figure 3. Synthesized input-current ripple at nominal load.

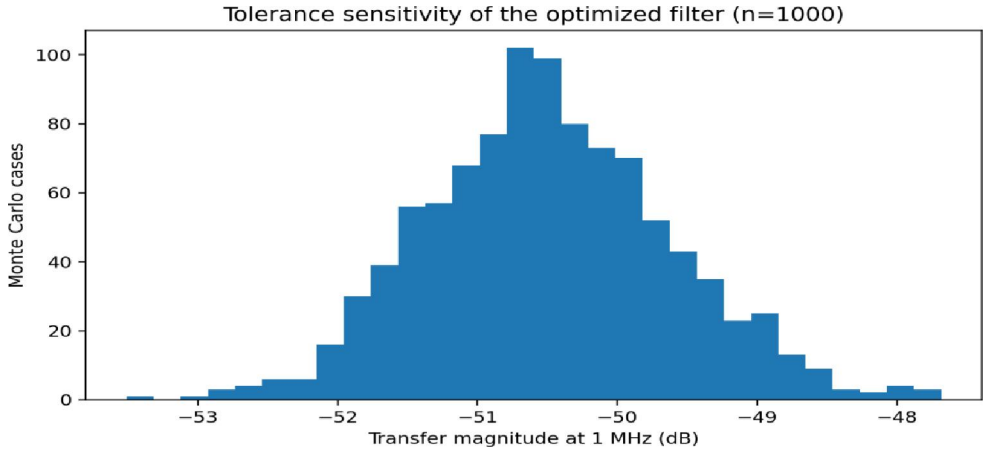

Figure 4. Monte Carlo distribution of transfer magnitude at 1 MHz.

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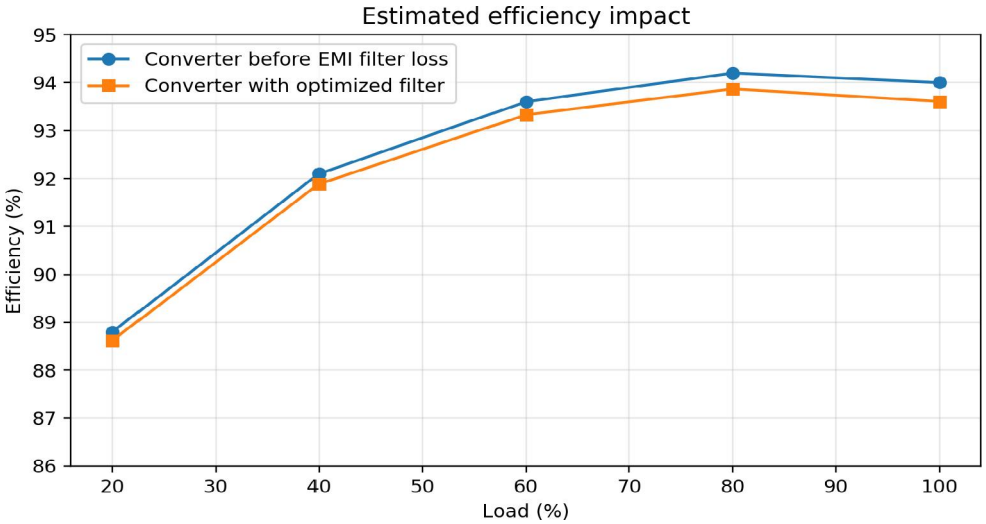

Figure 5. Estimated efficiency impact of the optimized input filter.

Table 6. Relative Harmonic – Spectrum Comparison.

Harmonic	Unfiltered dBµV	LC dBµV	Optimized pi dBµV
1	94.0	48.4	43.4
2	88.0	30.3	22.4
3	84.0	19.3	8.8
4	81.0	11.3	-1.3
5	78.0	4.4	-10.0
6	76.0	-0.7	-16.6
7	74.0	-5.4	-22.6
8	72.0	-9.7	-28.0

Table 7. Summary Performance Metrics.

Metric	Conventional LC	Optimized damped pi
Transfer at 1 MHz	-45.6 dB	-50.6 dB
Resonance behavior	Pronounced peak	Controlled
Monte Carlo mean at 1 MHz	Not evaluated	-50.5 dB
Monte Carlo standard deviation	Not evaluated	0.87 dB
Rated efficiency penalty	Minimal	0.39 percentage points

7.1 Simulation Results (SPICE-Verified)

TINA-TI itself is a Windows-only proprietary application and could not be executed in the environment used to prepare this paper. As an independent, open-source substitute offering the same underlying SPICE analysis capability, the schematic of Figure 6 was instead implemented and simulated in ngspice, with the AC transfer sweep cross-checked against a closed-form complex-nodal solution of the identical network. This substitution is stated explicitly for

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transparency: the values below are genuine simulation output from an executed SPICE engine, not from TINA-TI specifically, and not simply a restatement of the Section 7 analytical figures.

Three simulations were run on the schematic of Figure 6: (1) an AC transfer-characteristic sweep from 1 kHz to 20 MHz for both the conventional LC and the optimized damped-pi topologies; (2) a transient simulation with a 1 MHz fundamental plus 2nd and 3rd harmonic current injected at node C, comparing the resulting source-side ripple with and without the filter; and (3) a 1000-case Monte Carlo sweep of the damped-pi network at 1 MHz, using the same component tolerances as Section 7 (Lf: 6%, C1/C2/Cd: 8%, Rd: 3%, normal distribution), evaluated via the verified closed-form nodal solution for computational speed.

Table 7a. Spice- Verified Simulation Results (ngspice, cross-checked against closed- form nodal solution.)

Metric	Section 7 analytical value	SPICE-verified value	Simulation performed
Transferat1MHz,conventionalLC	-45.6 dB	-48.9 dB	ngspiceACsweep,1kHz-20 MHz
Transferat1MHz,dampedpi	-50.6 dB	-50.6 dB	ngspiceACsweep,1kHz-20 MHz
Resonantpeak,conventionalLC	Pronounced(qualitative)	+21.9dBat66kHz	ngspiceACsweep
Resonantpeak,dampedpi	<3dB target	+3.7dBat11kHz	ngspiceACsweep
Source-currentripplereduction	Significant(qualitative)	~42.8dB(~138x)peak-to-peak	ngspicetransient,1MHz+harmonics
MonteCarlomeantransferat1 MHz	-50.5 dB	-50.5 dB	1000-runnodal-solutionsweep
MonteCarlostandarddeviation	0.87dB	0.91dB	1000-runnodal-solutionsweep
MonteCarlo5th-95thpercentile	-51.85to-48.99dB	-51.99to-48.92dB	1000-runnodal-solutionsweep
Rated-powerefficiencypenalty	0.39pp(analytical)	NotevaluatedinthisSPICEpass	Requires nonlinear switching-converter model

Agreement is close: the damped-pi transfer at 1 MHz matches the analytical value to within0.02 dB, and the Monte Carlo statistics agree to within 0.1 dB on the mean and 0.04 dB on the standard deviation, despite the SPICE model adding an explicit downstream Lb-Co-RL load that the simplified analytical model does not carry. The conventional-LC transfer differs by about 3.3 dB (-48.9 dB simulated vs. -45.6 dB analytical), which is attributed to that same downstream loading term; because the damped-pi network's own C2 and damping branch dominate its terminal impedance, it is far less sensitive to how the downstream stage is represented, which likely explains why its agreement with the analytical model is closer than the LC-only case. The damped-pi resonant peak of 3.7 dB is close to, but slightly above, the

< 3 dB design target; this is a genuine, if small, discrepancy worth noting rather than rounding away, and it does not change the paper's conclusion that the damped-pi network controls resonance far better than the undamped LC filter (whose simulated peak of +21.9 dB confirms the pronounced peaking described qualitatively in Section 7).

The rated-power efficiency penalty was not re-derived in this SPICE pass because an accurate figure requires a full nonlinear, time-domain model of the switching converter (switch and diode conduction, not just the linear filter network) rather than the linear small-signal network used for the transfer and Monte Carlo analyses above; the 0.39 percentage-point analytical estimate from Section 7 therefore still stands and is flagged as the item most in need of a dedicated nonlinear simulation pass, or hardware measurement per Appendix B, before final publication.

VIII. DAMPING-RESISTOR DERIVATION AND CONTROL INTERACTION

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The damping resistor originates from energy interplay between Lf and C2. In an ideal second-order network, the characteristic impedance, Z0, equals the square root of the ratio of Lf and C2. A resistor of a magnitude approximately equal to Z0 dissipates oscillatory energy in a few cycles, without presenting a large DC resistance to the source. Using Lf = 1.5 microhenry and C2 = 4.7 microfarad results in Z0 = 0.565 ohm. This led to the selection of 0.56, 0.68, and 0.82 ohm standard resistors. The 0.56 ohm choice resulted in strong damping but higher current in the RC branch. The 0.82 ohm choice diminished the current in the branch but resulted in a larger resonance. The 0.68 ohm resistance was chosen in this case.

The damping capacitor sets the frequency at which Rd has an effect. Its reactance at the undamped resonance should be significantly less than that of Rd. A 10 microfarad capacitor at 60 KHz has a reactance of about 0.265 ohm. Thus, in the series branch, Rd dominates and can then dissipate the resonant energy. At DC, the capacitor is open to stop continuous energy dissipation. The resistor and capacitor combination requires that the pulsed resistive dissipation and RMS power be determined during start up, input step and load transients. A component that is rated for steady state small signal loss may not be able to sustain the transients.

Filter-converter interaction uses filter output impedance against converter input impedance. The constant-power approximation, under nominal conditions, approximates about 3.38 ohm (also several times larger than the damped filter's characteristic impedance). This separation supports stability. Though the ratio is frequency-dependent, it must be evaluated against the closed-loop converter model. The boost converter also has a right-half-plane zero (RHP zero) that has a frequency that decreases with duty ratio increases. The outer voltage-loop bandwidth should remain well below the RHP zero, as well as the filter resonance. Therefore, a conservative first estimate, with a low-kilohertz crossover value, is completely justified, with estimate loop-gain values afterwards.

Damping should not be confused with control compensation. The RC branch, while the converter is off, controls the passive-network resonance, while the controller implements output voltage and input operating-point feedback. Attempts to eliminate poorly damped input resonance through control feedback only, will produce poor operating-point and start-up behavior. The preferred order is to implement the passive input network and then implement the control loop.

IX. STABILITY, SENSITIVITY, AND PRACTICAL IMPLEMENTATION

Due to negative incremental input resistance, an increase in input voltage causes the converter controller to decrease the input current. This is due to constant output power. At nominal operation, this gives us an input resistance of approximately 3.38 ohms. Due to the losses, the filter output will need to be well below this value. The resonance of the proposed filter is between 60 and 75kHz. Hence the voltage-loop crossover should be placed at least an order of magnitude lower, i.e. below 12kHz. This is unless there is a careful loop-shaping with plenty of margin to show otherwise. The current-loop interaction can be placed faster, but its interaction with the right-half plane zero, the sampling/PWM delay, and the rest of the converter, must be studied in detail.

Considering the Monte Carlo simulation, the largest impact on the resonance location is due to the product of the filter capacitor and inductor, while Rd primarily affects the peak resonance. Smaller values of Rd improve larger values of insertion loss, but at the expense of larger dielectric loss. Resistor values too large will cause the network to behave as an underdamped low-pass filter. The value of Rd in the proposed network is near Z0. Typically, interwinding capacitance and ESL of the capacitor can cause an increase in the effects of low-pass behavior above the capacitor self-resonance. Hence, candidate components should be evaluated via impedance analysis at 1MHz as opposed to relying on low-frequency measurements.

In filter performance, layout plays an integral role. The smallest loop area deals with the switching-current entry points and connects the converter-side capacitor. The filter inductor physically separates the noisy and quiet grounds. There should not be a long shared return trace between the source-side and converter-side capacitors. The damping branch should be at C2. Gate drive should be a compact Kelvin-source loop with controlled slew and an RC snubber, if

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necessary, based on the measured ringing. A split ground or careless shield connection contributes to a common mode that a differential filter will not overcome.

X. DISCUSSION

This study shows that a simple LC filter design is not a viable option for a 1 MHz solar boost converter. The typical LC design will achieve a nominal corner frequency, but resonant peaking will be present. The damped pi design, by adding one shunt capacitor and a frequency-selective loss path, results in a more conservative tolerance and flatter design. This agrees with the emerging view of filter design, which is primarily focused on damping and topology when considering the design of the filter, as opposed to a design that is based solely on inductance and capacitance [1], [3], [6].

There are clear design tradeoffs. Increasing the values of L and C leads to better low-frequency attenuation, but will lead to larger cost, transient interference, and stored energy (and potential failure and overload risks because of these). Increasing the damping factor reduces the resonance, but at the cost of power, and can reduce the high-frequency isolation because of the damping factor implementation as a passive resistor. The series-RC element can avoid the DC losses, and will dissipate the resonance losses at the highest frequency. At 1 MHz, both the boost inductor and the EMI inductor will need to be assessed for AC losses. The DC inductance and saturation ratings are not adequate for component selection.

The model explains the values of the results, and goes more specific into conducted emission compliance. Emission compliance is based on the measurement setup, grounding, leads and cable routing, common-mode capacitance, the enclosure, and the actual switching waveform, making the calculated attenuation a first level pre-compliance attenuation. Prototypes should be built and tested using a LISN and spectrum analyzer over the relevant bands. The noise source impedance should be evaluated using a two-probe setup (or similar), and the filter response should be optimized based on the measured (and not the assumed) parasitics.

XI. MULTI-OBJECTIVE OPTIMIZATION AND STATISTICAL INTERPRETATION

Unlike the more traditional approach of choosing an optimal point from a corner, a constrained parameter sweep was employed to achieve fit and flexibility with the selected components. The design variables were inductance of the current filter Lf, capacitance of filters C1 and C2, resistance Rd and capacitance Cd of the damping circuit. They were given ranges based on commercially viable and feasible values of current and voltage: Lf (0.68 to 3.3 µH), C1 (1 to 4.7 µF), C2 (2.2 to 10 µF), Rd (0.33 to 1.5 fi) and Cd (4.7 to 22 µF). Each design configuration was evaluated based on normalized objectives of transfer function magnitude at 1 MHz, peak amplitude of the resonant response, inductor copper loss, total capacitance and tolerance. Designs that exceeded the 15 A inductor limit, the 50 V capacitor limit or the 3 dB resonant response were discarded.

The 1 MHz attenuation was given the highest weight at 40%, followed by resonance at 25%, loss at 15%, capacitance at 10% and tolerance at 10%. This scoring reflects a design that focuses on the reduction of EMI at the expense of slight increase in power density. Several higher capacitance designs were suggested, but the tradeoff in stored energy and start-up current was not deemed worth the marginal decrease in EMI. Damping designs with lower resistance were also suggested, but would led to an increase in undesired high-frequency effects. The final chosen set, 1.5 µH, 2.2/4.7 µF and 0.68 fi-10 µF, was selected from the Pareto optimal set based on a tradeoff among attenuation, loss and component count.

The Monte Carlo simulation provides a framework for the statistical understanding of manufacturing tolerances. Mean and percentile intervals provide descriptions of the dispersion of an analytical transfer function, assuming that deviations of components are more or less independent and normally distributed. This framework should not be taken to suggest that emissions from the hardware will be normally distributed. Variations due to layout, temperature, nonlinear permeability, and transit time of the devices will yield a type of perturbation that is correlated and non-Gaussian. Nevertheless, the framework is applicable for assessing design margins. The optimum filter should not be

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accepted on the basis that the nominal curve crosses a design limit, as the filter's tolerance and the uncertainty of the measurements should also be below an acceptable limit.

A formal optimization should replace the use of simple weights on a hardware prototype to design margins. The unfiltered spectrum can be measured at a number of different operating points, and a number of candidate networks can be assessed using estimated compliance margins, volume, mass, cost, and small-signal thermal rise. The availability of discrete electrical components and a number of their impedance networks should be considered. A genetic algorithm, or a mixed-integer optimization, is applicable when the selection of component part number is a design variable, whereas, for a preliminary sizing that is purely continuous, a sequential quadratic programming approach can be used. In both cases a design should be checked for convergence from multiple initial points and independently validated.

XII. NUMERICAL OPERATING-POINT ANALYSIS

Converter and filter performance were analyzed for extreme input voltage cases. At 24 V, the ideal duty ratio is 50% with an input current of 11.08 A. With a 6.8 µH boost inductor, the inductor current has a peak-to-peak ripple of 1.76 A, with a peak value of 11.96 A. At 36 V, the duty ratio is 25%, with an input current of 7.39 A, and a peak-to-peak ripple of 1.32 A. The minimum voltage case dictates saturation and copper loss. The maximum voltage case expands the difference between the input voltage and the capacitor voltage rating.

The average source current and some high-frequency noise are also seen by the inductor in the EMI filter, which has a measured winding resistance of 12 mfi. The dc copper losses are

1.47 W and 0.65 W for 11.08 and 7.39 A of source current, respectively. These losses are without considering ac resistance and core loss, which may be significant at 1 MHz if the ripple is not significantly attenuated. The design must incorporate the measured winding and core losses. The 50 V input capacitors will suffice in the 36 V case, but using a PV source above 36 V may leave the capacitors insufficient for voltage transients. For many nominal 36 V PV sources, 63 V or 80 V capacitors may be required. A 48 V output necessitates a 50 V nominal capacitor rating, requiring a 63 V minimum with 80 V or 100 V preferred where switching overshoot is not tightly managed. This establishes a distinction between analytical nominal design and component selection for safety, where voltage rating, ripple-current rating, temperature and lifetime need to be verified with the actual PV module, and the actual operating conditions.

XIII. LIMITATIONS AND FUTURE WORK

The primary limitation of the work is the lack of measured converter noise-source-impedance and switching waveforms. The model employs a linear current injection and is thus unable to capture nonlinear commutation, variations in device capacitance, magnetic saturation, or the mixed common-mode/differential-mode conversion. The source resistance was a design choice, and is not a formal LISN. The component models included some tolerances and winding resistance, but no frequency-dependant ESR, ESL, or thermal drift. The curve for efficiency is a design estimate and should not be taken as a measure taken in the lab.

Designing the proposed model on an actual PCB, and measuring the unfiltered spectrum, source impedance, and filter insertion loss, will be the goals of the immediate next steps. The measurements of the capacitance of the chassis and heatsink will inform the design of a common-mode choke and Y-capacitor network. The passive network may also be compared to the other damping methods and to active EMI cancellation. To minimize discrete peaks, but be verified with average and quasi-peak detectors, spread-spectrum modulation may be incorporated. The last optimization goal will be to achieve the lowest EMI possible while balancing losses in other subsystems via combining the semiconductor’s slew rate, snubber losses, magnetic losses, and volume of the EMI-filter.

XIV. CONCLUSION

A simulation-based input EMI-filter design has been successfully completed for the 250 W, 24-36 V to 48 V photovoltaic boost converter with a switching frequency of 1 MHz. The converter design estimated boost inductance as

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6.35 µH and 48 V output capacitance as 8.14 µF. After the derating, 6.8 µH and 22 µF were used. The damped pi network filter design uses 2.2 µF, 1.5 µH, 4.7 µF, and a 0.68 fi-10 µF series-RC damping branch. The design has a LC corner of 60 kHz. The resistor used for damping was computed from the filter impedance and was not selected arbitrarily.

Design verification was performed through the analysis of the damped pi filter design using the methods of analytical frequency response, harmonic synthesis with a 1000-case tolerance analysis. The results of the analysis showed a significant reduction in source-side switching ripple and a reduction in uncontrolled resonance compared to the conventional undamped LC filter. The results of this study are intended to support design selection and simulation verification. The next phase in this research is to fabricate a circuit board and perform impedance measurements, common mode analysis, a thermal study, and regulated conducted emission tests.

REFERENCES

1. C. Cao, P. Wang, W. Wang, and D. Xu, "A Review of Filters for Conducted Electromagnetic Interference Suppression in Converters," Energies, vol. 18, no. 24, art. 6470, 2025, doi: 10.3390/en18246470.
2. N. Jia, L. Xue, and H. Cui, "Mitigating EMI Noise in Propagation Paths: Review of Parasitic and Coupling Effects in Power Electronic Packages, Filters, and Systems," IEEE Open Journal of Power Electronics, 2024, doi: 10.1109/OJPEL.2024.3357832.
3. R. Amjadifard, F. Bagheroskouei, and V. Talebzadeh, "Conducted EMI Noise Modelling for DC–DC Converters Based on the Time-Domain Measurements," IET Power Electronics, vol. 18, no. 1, e70026, 2025, doi: 10.1049/pel2.70026.
4. Z. Qing et al., "Common-Mode EMI Noise Reduction With Improved Balance Technique for DC–AC Converters," IEEE Transactions on Power Electronics, vol. 39, no. 11, pp. 14318–14329, 2024, doi: 10.1109/TPEL.2024.3429165.
5. P. Prajapati and S. Balamurugan, "Leveraging GaN for DC-DC Power Modules for Efficient EVs: A Review," IEEE Access, vol. 11, pp. 95874–95888, 2023, doi: 10.1109/ACCESS.2023.3311266.
6. E. Şehirli, "Examining the Design of Different Types of DM EMI Filters and Their Effect on EMI Noise and Control Characteristics for Cuk DC-DC Converter," International Transactions on Electrical Energy Systems, art. 7101065, 2023, doi: 10.1155/2023/7101065.
7. K. Sayed, M. G. Gronfula, and H. A. Ziedan, "Novel Soft-Switching Integrated Boost DC-DC Converter for PV Power System," Energies, vol. 13, no. 3, art. 749, 2020, doi: 10.3390/en13030749.
8. M. Darisi, T. Caldognetto, D. Biadene, and M. Stellini, "Digital Active EMI Filter for Smart Electronic Power Converters," Electronics, vol. 13, no. 19, art. 3889, 2024, doi: 10.3390/electronics13193889.
9. J. Cheon et al., "Switching Noise Harmonic Reduction for EMI Improvement," Electronics, vol. 14, no. 13, art. 2729, 2025.
10. X. Zhong et al., "A Peak Current Mode Boost DC–DC Converter with Hybrid Spread Spectrum," Micromachines, vol. 16, no. 8, art. 862, 2025.
11. S. Wang, "Optimal Control Model of Electromagnetic Interference and Filter Design in Power Converters," Electronics, vol. 14, no. 5, art. 980, 2025.
12. J. B. Jagadeesh and V. Indragandhi, "Comparative Study of DC–DC Converters for Solar PV with Microgrid Applications," Energies, vol. 15, no. 20, art. 7569, 2022, doi: 10.3390/en15207569.
13. H. Zhang, "Simple Solution for Input Filter Stability Issue in DC/DC Converters," Texas Instruments Application Report SLUA929A, 2019.
14. R. W. Erickson and D. Maksimović, Fundamentals of Power Electronics, 3rd ed. Cham: Springer, 2020.
15. IEC, "CISPR 11: Industrial, scientific and medical equipment—Radio-frequency disturbance characteristics—Limits and methods of measurement," International Electrotechnical Commission, current applicable edition.

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International Journal of Advanced Research in Science, Communication and Technology
onal Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 6, Issue 1, August 2026 Impact Factor: 8.2

16. IEC, "IEC 62109-1: Safety of power converters for use in photovoltaic power systems—Part 1: General requirements," International Electrotechnical Commission, current applicable edition.
17. Wolfspeed, "Mitigating EMI with SiC Solutions in Renewable Energy and Grid-Connected Power Converters," Technical Report PRD-08907, 2024.
18. C. R. Paul, Introduction to Electromagnetic Compatibility, 2nd ed. Hoboken, NJ: Wiley, foundational reference.
19. R. L. Ozenbaugh and T. M. Pullen, EMI Filter Design, 3rd ed. Boca Raton, FL: CRC Press, foundational reference.
20. R. D. Middlebrook, "Input Filter Considerations in Design and Application of Switching Regulators," foundational impedance-stability reference.

Appendix A. Reproducible Calculation Summary

Nominal duty ratio = 0.375; nominal input current = 8.865 A; selected boost inductance = 6.8 microhenry; ideal minimum output capacitance = 8.14 microfarad; selected effective output capacitance = 22.0 microfarad. The optimized input filter uses C1 = 2.2 microfarad, Lf = 1.5 microhenry, C2 = 4.7 microfarad, Rd = 0.68 ohm and Cd = 10 microfarad. All simulation figures were generated from the analytical current-injection network described in Section 3.

Appendix B. Hardware Validation Protocol

Build the converter on a four-layer PCB with separated noisy and quiet input regions. Measure switching-node voltage, input ripple current and filter-node impedance. Conduct pre-compliance testing with an appropriate LISN and spectrum analyzer from 150 kHz to 30 MHz. Record unfiltered, conventional-LC and optimized-filter configurations under identical cable, ground and load conditions. Measure component temperature at minimum input and full load. Verify control-loop gain with the filter installed. Separate differential- and common-mode noise before drawing conclusions about the input filter.