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Designing 10T SRAM for noise and Leakage Power Reduction using Stack Transistor Technique – A Review

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Abstract: *The SRAM Semiconductor memory, utilize a bistable latch circuit to store logic 1 or 0 data. It differs from dynamic RAM (DRAM) which requires a periodic refresh operation to store logical data. SRAM power consumption varies with operating frequency, i.e., at higher frequencies, it consumes very high power, similar to DRAM. Because the cache included in the microprocessor required high-speed memory, SRAM can be used in the microprocessor for this purpose. DRAM is often used in processor main memory, where density is more important than speed. SRAM as well used in industrial, scientific electronics, and automotive subsystems. In this paper, the SRAM investigation report was studied to develop a new SRAM design for low power consumption.*

Keywords: Static Random Access Memory (SRAM), Stability, Power Consumption, Read Write modes

I. INTRODUCTION

In computer data storage, Random access memory (RAM) is an important part of the system. Regardless of the order that data objects accessing, a random access memory (RAM) device can able to read and write data items in about the same amount of time. When compared to other media data storage for instant, hard drives, Read-Write of DVD, and Read-Write of CD, the required time for reading and writing data items differs significantly depending on its physical position as well as limitation of mechanical parts such as speed of vehicle rotation and delay in arm movement. After the innovation of Integrated circuits (IC's), Random access memory (RAM) is also made with Integrated circuits (IC's). The "random access memory" is commonly accustomed to denote volatile memory category such as DRAM memory modules. But the information stored in this memory type will be vanished in case of power cut-offs. The efforts have been put to develop a non-volatile Random Access Memory Integrated circuits for stability of memory system. There are other types of non-volatile storage that allow random read access, but do not allow or restrict writes. This contains most varieties of ROM and NOR flash, which are flash memory type. The following are the advanced RAM categories in use today:

- Static Random Access Memory (SRAM)
- Dynamic Random Access Memory (DRAM)

1.1 Static Random Access Memory (SRAM)

This type uses a bistable latching circuit which is a form of semiconductor memory that store one bit. The term static RAM is distinguished from dynamic RAM, which needs to be updated on a regular basis. Static RAM contains residual data. However, it is volatile in the traditional sense, and if the memory is not powered, it eventually loses data.

1.2 Dynamic Random Access Memory (DRAM)

A pair of transistors and capacitors are used in DRAM that form a dynamic RAM cell to store some data. The capacitor maintains both a high and low charge, while the transistor functions as a switch, enabling the chip's control circuitry to read and modify the capacitor's charge state. This type of memory, which is less expensive to produce than static RAM, is the most common type of computer memory in today's computers. Dynamic RAM is considered volatile because information and data are lost when the system is powered off.

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II. Operation of Static Random Access Memory (SRAM)

The SRAM has three modes of operations which is Standby, Read, and Write. The cell of 6T SRAM as shown in fig 1 built up of two cross coupled inverters (M1, M2, M3, M4) and two access transistors (M5, M6), connecting the cell to the bit lines. For the outside communication and communication with cross coupled inverters, the access transistors are used for storage element. In order to function in read mode and write mode, the SRAM should have readability and write stability respectively. [1]

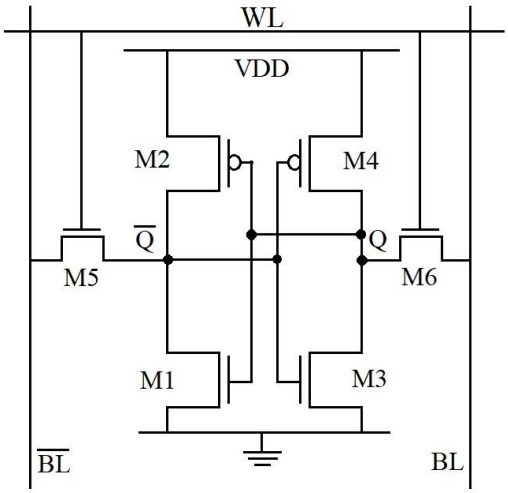

Figure 1: 6-Transistor Static Random Access Memory (SRAM)

2.1 Standby Mode

The M5 and M6 access transistors disconnect the cell from the bitstream if the word line is not asserted. Two cross-coupled inverters have developed, and as long as they are linked to the mains, they will continue to boost.

2.2 Read Mode

Let's take an example of 6T SRAM cell as shown in Figure 1. Let's aassume that the value of the memory is 1 and that content is stored in Q. By charging both the bitstream to 1, the read cycle begins. Then both access transistors M5 & M6 are turned on determining receive word line (WL). In second step, the stored values in Q and Qbar at its pre-charge are moved to the bit lines by withdraw from BL and BL discharging to logic 0 through M1 and M5. On the other side of bit line BL, the M4 and M6 transistors drag the bit line near Vdd a logic 1. If the memory content was 0, the reverse will happen and BL will be dragged to 1 and BL to 0 [2]. Then while reaching sense amplifier, the BL and BL-bar lines will have a small potential difference between them [2]. It will detect which line has the highest voltage and then determine if a 1 is stored or a 0. If the sensitivity of sence amplifier is higher, then the read operation will be faster and vice versa.

2.3 Write Mode

By applying the value to be written to the bitstreams, the start of a write cycle begins. When 0 is applied to the bitstream If we want to write 0, and 1 is written by inverting the values of the bitstreams. The word stream (WL) is then asserted and the stored value is locked. The input drivers of bitstream are designed to be much more powerful than the relatively weak transistor in the cell, so they can effortlessly substitute the earlier state of cross-coupled inverters.

2.4 Power and Clock Rate

The power consumption of SRAM varies considerably depending on the access frequency. When used at high frequencies, it can be as power-hungry as dynamic random-access memory (DRAM), and at full bandwidth some ICs consume more watts [3]. Static RAM, on the other hand, is being used in a slower rate and requires minimal power, like in application areas with moderately clocked processors, and this may utilize almost no power. even when operating at a low power level of a few micro watts

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2.5 SRAM as Embedded

For real-time digital signal processing circuits, the dual-port static RAM is used [4]. The various categories of Scientific & Industrial subsystems, automotive electronics requires static random-access memory. The products having complex circuits used few megabytes of static random-access memory such as cellphones, digital cameras, portable tablets, synthesizers, computers, hard disk caches, routers, etc. [3]. To maintain the image display, printers and LCD monitors also often use static RAM.

III. Literature Survey

Birla, Shilpi analysed the 8T static random access memory cell as shown in fig. 2 at 65 nm process technology. This study was originally proposed for a sub-threshold static RAM design enhanced for function and performance. power over a wide voltage range. Writes are performed through the WWL, WBL, and WBLX ports, while asymmetric reads are performed through the RWL and RBL ports. At the end of each read cycle, the RBL is preloaded and remains preloaded during a write cycle. The write and read ports are separated unlike the traditional 6T cell in this binary cell. The Read SNM problem is eliminated and for better writes without sacrificing RSNM, the 6T static RAM portion can be sized. This invalidates the voltage drop in the unchecked read buffer and thus the leakage on the read bitstream is greatly reduced. For cross-coupled inverters, the Vdd are virtual power nodes and its voltage can be lowered during write access to weaken the PMOS load device and alleviate the low voltage write problem. Since all binary cells in a row are written and read at the same time, Vdd is split across a row of memory cells. [5]

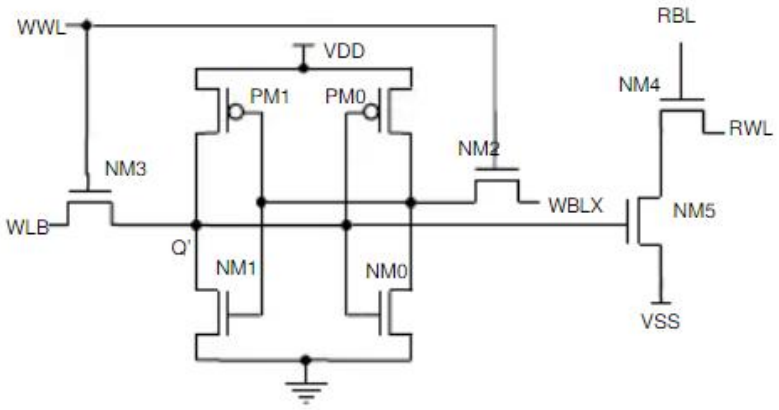

Figure 2: 8T SRAM

Venmathi & Vivekanandan proposed to design a memory cell for FPGA that consumes less power. A self-monitoring voltage level (SVL) circuit and a 10T SRAM cell are among the components of the proposed work. An asynchronous counter is present in the memory block of the read circuit, instead of shift registers. Various components are designed using 180nm technology. The average power consumption and power delay products for all stages are calculated and compared. The main drawback is that they did not take temperature and surface constraints into account when designing the FPGA memory cell. The advantages of this method include high resistance to interference, data retention at rest and also providing high operating speed. [6]

Kiran & Mondal proposed 10T SRAM structure is modeled and simulated to produce faster read operations without any constraints. The detailed layout of the 10T is achieved using 45nm technology. Read power and latency have been calculated and compared with 6T SRAM cartridges. Leakage current and capacity are also calculated based on temperature. They analyzed the 10T SRAM cell by varying the temperature and voltage supplied to the cell, which showed stable and desirable power consumption. [7]

Nath Mandal D Recommended for stable and energy efficient SRAM, low consumption and desired minimal leakage component. The leakage currents flowing in the circuit are different so electricity from different places can leak. Subthreshold leakage current, gate leakage current and junction leakage current are mainly taken into account to calculate leakage power, and subthreshold leakage current is the most relevant component of all. [8]

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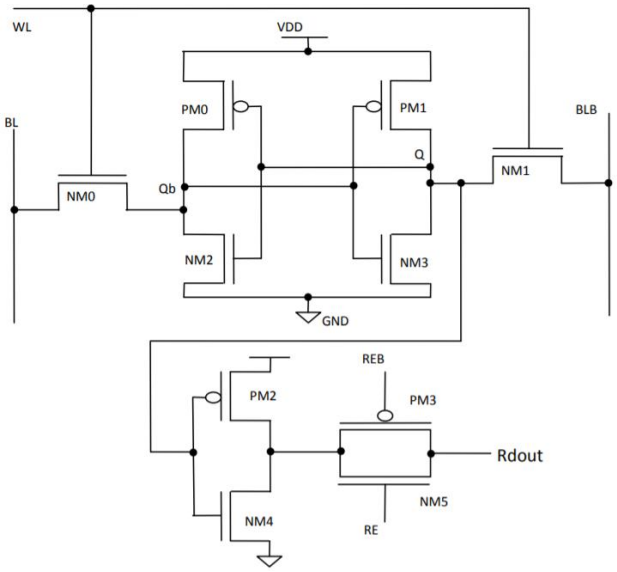

Figure 3: 10T SRAM cell

Prachi Sanvale, Neha Gupta, Vaibhav Neema, Ambika Prasad Shah, Santosh Kumar Vishvakarma proposed NM4 and NM5 transistors, which are high threshold voltage (HVT) transistors, are used for the read operation, which decreases the leakage current. The proposed cell during write operation has an improved noise margin as well as it has lowest power consumption. The proposed cell also has a better RSNM (Static Read Noise Margin) compared to other structures. [9]

Shikha Saun and Hemant Kumar analyzed the performance of conventional 6T SRAM cartridges on different technology nodes using PTM models in terms of power dissipation, latency, power delay product, and amplitude static noise. The comparison of results was performed at 45nm, 32nm, 22nm and 16nm technology nodes, showing that power dissipation and latency improved as the channel length was reduced, but stability was also a concern. great interest. The percentage reduction in the total power dissipation of the Technology Node from 45nm to 16nm is 91.27%. Stability is also tested for read, write and sleep modes at different technology nodes. However, the static noise amplitude also decreased by 22.92% in write mode, 20% in read mode and 57.89% in hold mode with the channel length reduced from 45 nm to 16 nm. The change of the SNM from the supply voltage shows that the SNM is also a function of the supply voltage, the selection of an appropriate supply voltage is also necessary to maintain the stability of the memory cell. Stability must be maintained for reliability issues, although power dissipation and latency are improved with the reduction of technology nodes. The additional performance of the SRAM 6T cartridge can be improved by applying various low power techniques. [10]

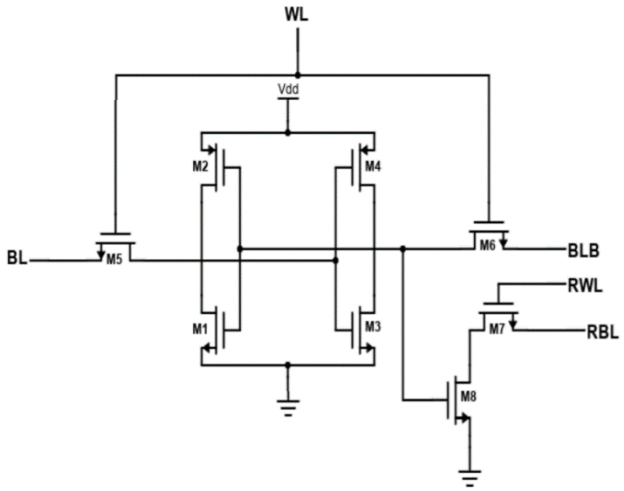

Figure 4: 8T Conventional SRAM

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S. Ahmad, M. K. Gupta, N. Alam and M. Hasan, proposed the ST11T is another Schmitt-Trigger cell made up of 11 transistors and has a separate read decoupling circuit with asymmetric cell operation. Figure 11 shows the SRAM ST11T cartridge. This cell is designed of cross-coupled ST inverters, a read path buit of two transistors and a write access transistor. The internal storage nodes Q and QB are responsible for driving the Schmitt Trigger, MNFL and MNFR feedback transistors respectively with their drains connected to the wordline bar (WLB) control signal (the complement of the signal). write permission) Due to the feedback mechanism, this cell has increased data storage capacity. In addition, this cell has reduced leakage current and power and improved reading stability. But this cell cannot record activity "1". As an asymmetric cell, it has a write access time and requires write-enabled circuits to minimize the "1" write access time. [11]

L. Chang proposed this cell which consists of a separate circuit with two supplementary NMOS transistors for reading operations which shown in fig 4. This reading scheme improves the cell stability by providing a reading mechanism that does not interfere with the internal nodes of the cell. This cell has independent read and write lines in addition with separate read and write lines for bits which allows two-port operation. 8T cell has better stability, higher SNM and lower power consumption. This cell also allows continuous scaling associated to the 6T cell which suffers from various downscaling issues. The 8T cell uses 30% more on the matrix compared to a conventional 6T cell. [12]

IV. Conclusion

Besides the different SRAM cells discussed here, many other SRAM cells using 7, 8, 9, 10 and even more transistors have also been designed to meet different design goals depending on depending on device requirements. In the future, it will be possible to analyse existing designs by applying various techniques for power reduction, voltage scaling, and stability improvement. In addition, given the current need to design low power dissipation devices, optimization of the design to decrease consumption of power can be made. The size of the device is also an important parameter nowadays, and therefore it is possible to proceed with the design of new SRAM cells that required less power and contain fewer transistors.

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