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A Modular Approach to Analog Signal Conditioning Circuit Design for Real-Time DSP Systems

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Abstract: *This paper delineates the design of a flexible analog signal conditioning circuit (SCC) that can be reconfigured in accordance with the needs of the user. It is feasible to implement the SCC with systems that are based on DSPs. The design is intended for use in power electronics applications that involve a diverse array of signal types. The design is composed of interconnected phases that can be activated in accordance with the characteristics of the input signal to ensure reconfiguration. The proposed circuit is a cost-effective and straightforward solution that utilizes commercially available components.*

Keywords: Analog-to-Digital Conversion, Digital Signal Processing

I. INTRODUCTION

For monitoring and regulation, engineers have collected data on power electronics applications such active filters, DC/DC converters, inverters, and others [1]–[6]. Data acquisition boards, DSPs, FPGAs, and microcontrollers that employ analog-to-digital converters need voltage and current signals from power electronics systems to be adjusted. ADCs digitalize conditioned signals. Conditioning is needed if the measured signal exceeds 3.3V, which DSPs, FPGAs, and microcontrollers need to power their ADCs.

Despite being essential to the measurement system, signal conditioning circuits are frequently neglected and poorly designed. Application strongly impacts signal conditioning. Common processes include galvanic isolation, impedance transformation, level translation and amplification, and linearization.

Current commercial boards may be utilized for amplification and filtering [7], [8]. However, these boards lack isolation, DC level shift, and attenuation.

This research proposes a flexible and changeable SCC that may be connected to an FPGA or DSP ADC. Low power consumption, component count, and affordability were considered while designing the reconfigurable circuit. SCC steps include attenuation, isolation, LPF, DC level shift, and voltage limiting. This SCC offers the following benefits over prior circuits [9], [10], and [11]: high ADC compatibility, reconfigurable design, simplicity of implementation, low power consumption, low component count, and low cost.

Document structure is as follows. Section 2 describes, designs, and specifies each proposed SCC level. Section 3 presents the circuit implementation and experimental demonstration of its operation. Section 4 concludes with some ideas.

II. DESCRIPTION AND OPERATION

Fig. 1 shows the suggested signal conditioning circuit block diagram. The design has five stages: attenuation, isolation, antialiasing filter, DC level shift, and voltage limiter. Most analog inputs to be converted are beyond the ADC's input range. Attenuators lower input signal loudness. Isolators safeguard electrical circuits against transients and ground loops (where passive resistive devices like shunt resistors are utilized). The filter reduces aliasing by reducing

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bandwidth, ensuring correct signal sampling. In particular, the DC level shift allows devices like DSPs and FPGAs to collect positive and negative AC signals. Lastly, the limiter prevents A/D converter saturation from over voltages.

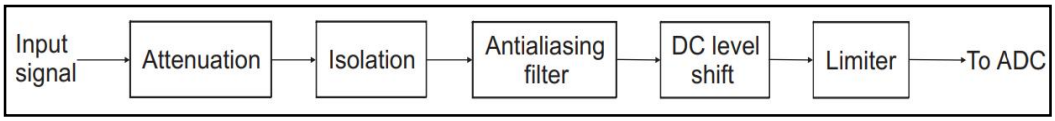

Fig.1: Block diagram of the signal conditioning circuit.

The suggested circuit design is presented in Fig. 2.

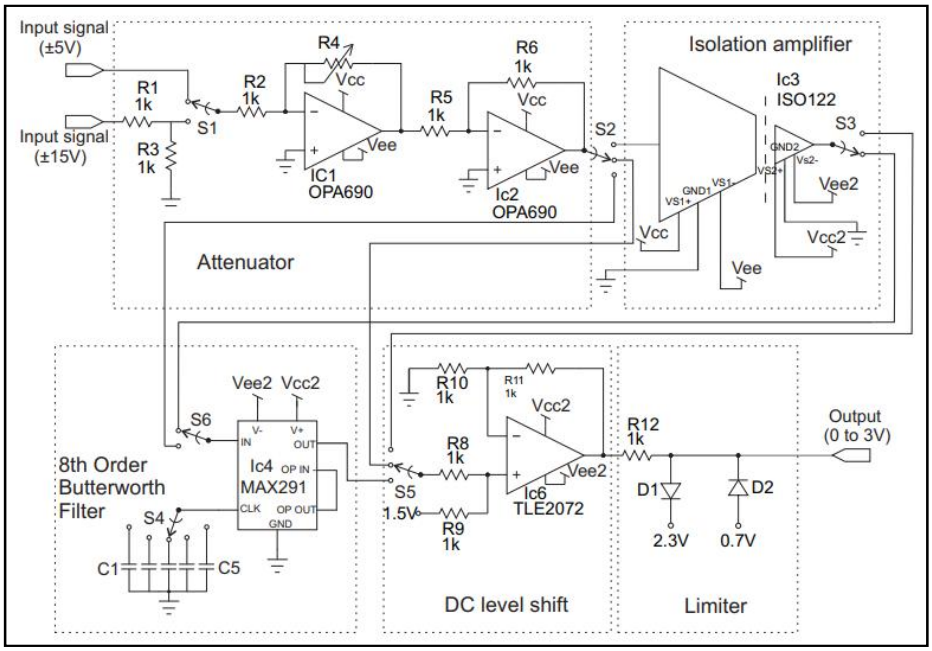

Fig.2: Schematic diagram of the signal conditioning circuit.

A. Attenuator

Fig. 2 shows an inverter amplifier attenuating input voltages 0–5V. Two attenuation scales are available with S1. At a scale of ±5V, the attenuation is:

$$G = -\frac{R_4}{R_3} \tag{1}$$

A voltage divider with attenuation of 2 is added to the inverter amplifier input for higher input signals (up to ±15V). $R_1 = R_2 = R_3$ gives the attenuation:

$$G = -\frac{R_4}{3R_1} \tag{2}$$

B. Isolation amplifier

The ISO122JP isolation amplifier (IA) galvanically isolates the attenuator's output signal. Two isolated DC/DC converters TEL 2-0521 (Traco Power) supply the IA with output voltages of ±5V and an input voltage range of 4.5–9V.

C. Antialiasing filter

An 8th order low-pass Butterworth switched-capacitor filter is employed to prevent aliasing. An external capacitor can be used to determine the cut-off frequency. Its value is determined by the following formula:

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$$C_{OSC}(pF) = \frac{10^5}{300 f_c(kHz)} \quad (3)$$

Jumpers with five on-board capacitors allow selection of five corner frequencies (5, 10, 15, 25, and 50 kHz). According to [12], sampling electric power line data at 5 and 10 kHz permits on-line voltage and current distortion investigation (harmonic and interharmonic). Inverter signals may be sampled at 15 and 25 kHz cut-off frequencies. A 50 kHz cut-off frequency is sufficient for capturing inductor currents from common DC/DC converters.

D. DC level shift

The fourth stage is a DC level converter. The analog input range of its ADC is typically imposed by any DSP, with the recommended operation conditions being V_{in}= 0–3V [13].

$$0 \le V_{in} \le V_{DDA} \quad (4)$$

where V_{in} is the input voltage of the ADC and VDDA is the supply voltage of the DSP.

A VDDA/2 voltage shift is necessary for bipolar analog signals. Figure 3 illustrates a schematic for the DC level converter. A well-known configuration of a summing amplifier enables us to add an offset voltage of +1.5V to the input signal.

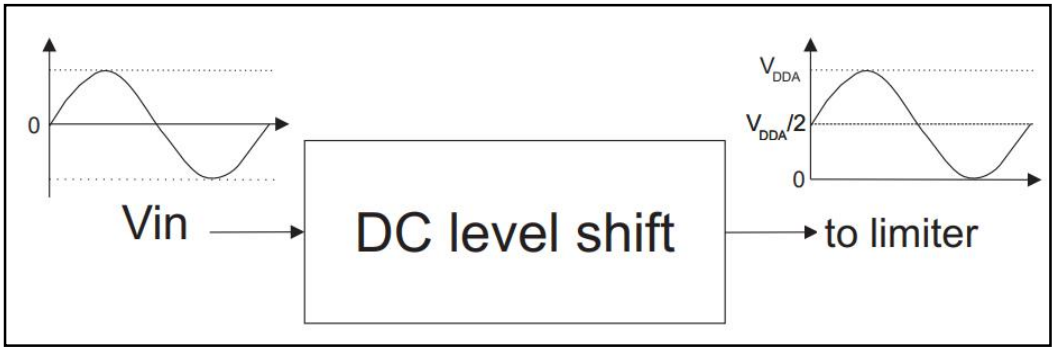

Fig.3: DC level shifter.

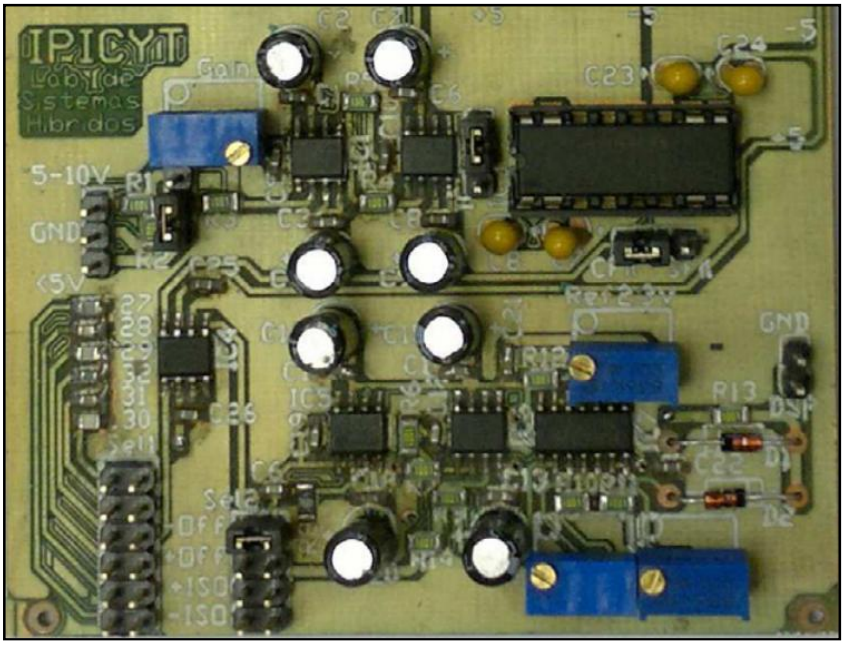

Fig.4: Prototype of the SCC.

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E. Limiter

The design of voltage limiters for DSPs or FPGAs devices must be meticulously analyzed, as in the aforementioned case. For instance, the ADC in the DSP TMS320F2812 necessitates a supply voltage of 3.3V (VDDA) and operates within the range of 0 to 3V. The conversion may be momentarily impacted by voltages applied to an analog input pin that are either above V = VDDA + 0.3V or below − 0.3V [13]. In order to prevent this, a double shunt limiter is employed to maintain the analogue input within these parameters. The output voltage follows the input (i.e., Vi = Vo) if the input voltage is between 0 and 3V. Consequently, both D1 and D2 are non conducting.

III. REALIZATION AND TESTING OF THE SCC

In order to confirm that the design objectives have been achieved, the frequency response of the SCC prototype is derived and demonstrated in this section. Additionally, the laboratory performance of the proposed SCC is assessed. Figure 4 illustrates the SCC prototype that was developed.

The circuit that has been proposed has the potential to accommodate the subsequent configurations:

Attenuator-isolation-antialiasing-DC level shift-Limiter

Attenuator-antialiasing-DC level shift-Limiter

Attenuator-DC level shift-Limiter

Attenuator-isolation-DC level shift-Limiter

Thus, the SCC may operate in four modes, depending on the application. Note that the suggested SCC requires less than 0.5W and costs around US$60. The prototype's frequency response is measured using a Tektronix AFG3022B function generator, a National Instruments acquisition board, and a Pentium IV running Windows 2000. Our instrument is intended for five frequency ranges, thus the generator and chirp signal are used to execute a linear frequency survey from 1Hz to 500kHz. The Compact RIO device acquires the instrument's input and output using two 16-bit ADCs to determine frequency response. After plotting the answer in Matlab, an appropriate program identified the system. Table 1 compares experimental and planned cut-off frequencies. The experimental values are close to the theoretical values, but capacitor tolerance and other imperfections cause the tiny variations.

Table 1: Comparison of the theoretical and experimental cut-off frequencies of the SCC

Cut-off frequency	
Theoretical (kHz)	Experimental (kHz)
5	4.98
10	9.98
15	15.10
25	25.25
50	49.80

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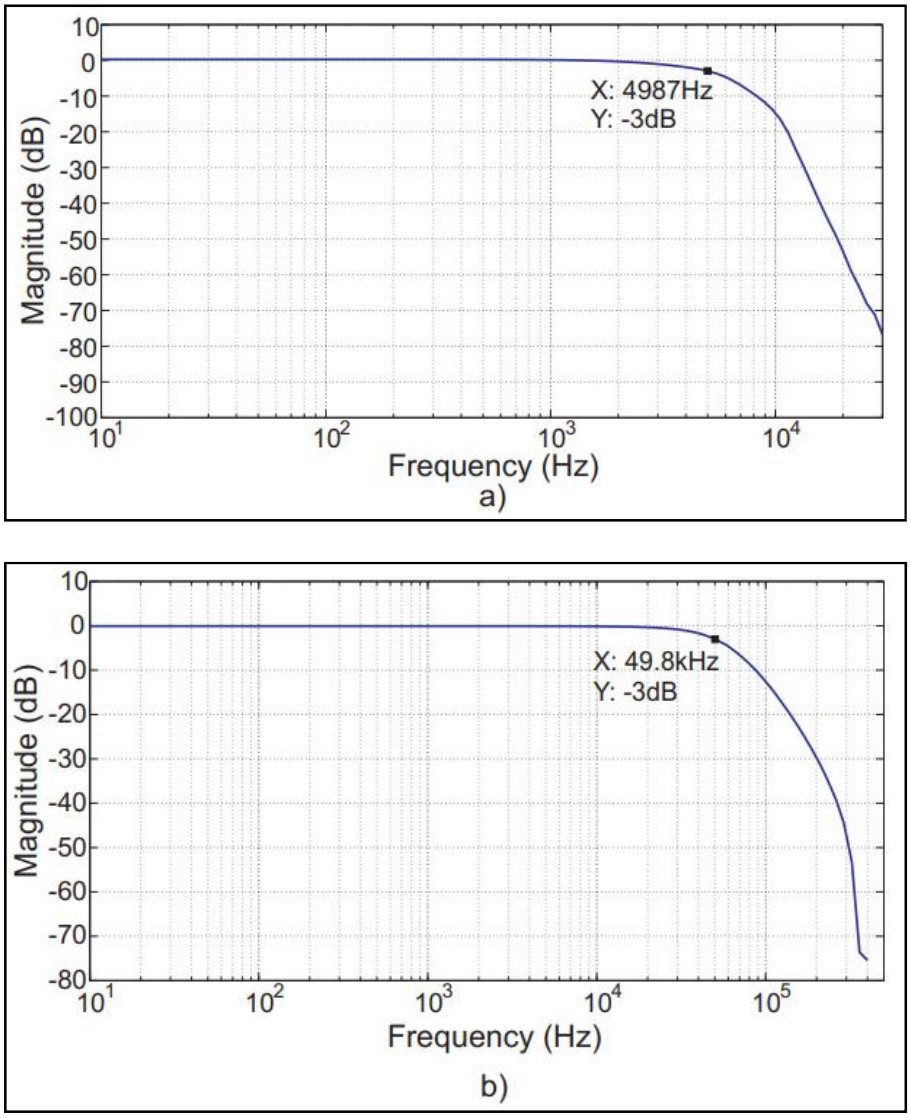

Fig.5: Frequency response of the SCC for cut-off frequencies of a) 5 kHz and b) 50 kHz.

Figure 5 a) and b) demonstrate the system's frequency response at 5kHz and 50kHz cut-off frequencies. The frequency response of the SCC is clear before the cut-off frequency.

The SCC was tested for operational aspects. Peak-to-peak input and output voltages were monitored. SCC results for sinusoidal signals employing each step are given in Fig. 6. A 1.5V DC level shift has been introduced to the input signal, resulting in a phase shift owing to the antialiasing filter.

The suggested SCC was also tested utilizing a hammer drill AC signal. To measure and condition a hammer drill's input current for comparison, the suggested SCC was used. The current was measured using a hall effect sensor (LEM55-P) and a Tektronix AC/DC current probe model A622 with a 100mV/A scale. The measured and SCC signals are shown in Fig. 7 a). As observed, the SCC signal has the same structure as the measured signals, but the conditioning may correct the voltage from 0 to 3V.

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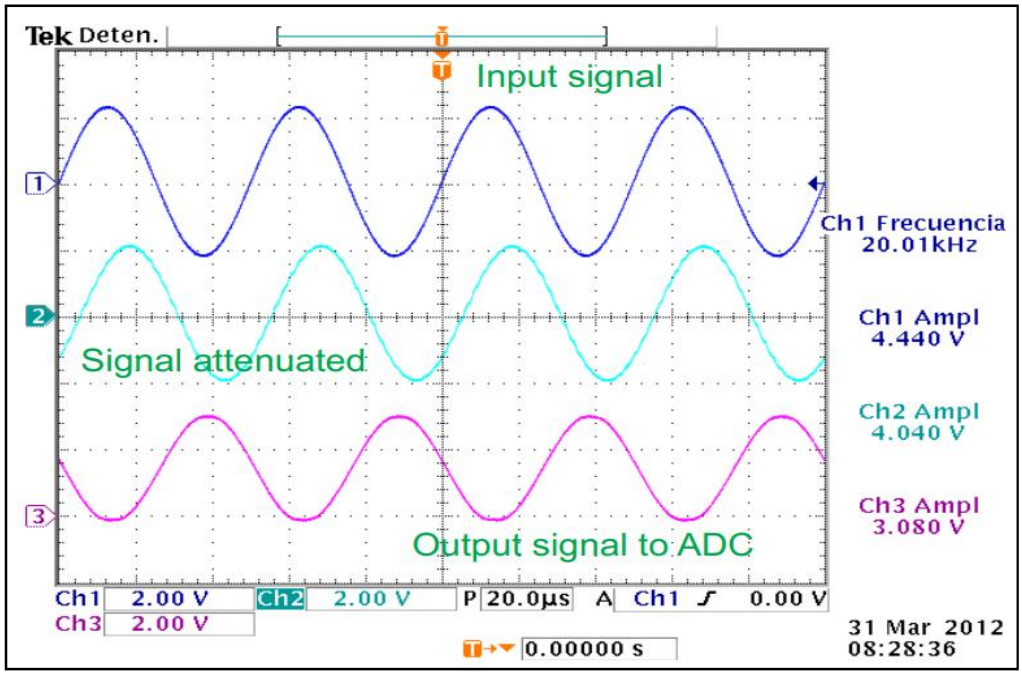

Fig.6: Test with sinusoidal input.

A perturbation is implemented on the impact tool to assess the limiter. An increase in its current consumption is observed in (Fig. 7 b). It is evident that the SCC restricts the output signal to prevent the ADC from becoming saturated.

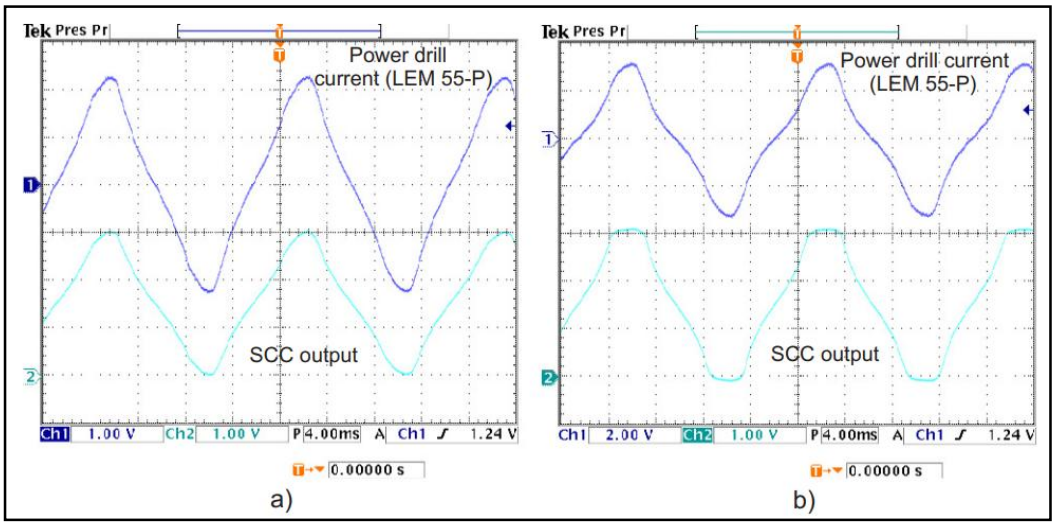

Fig.7: Time evolution of a hammer drill current. Comparison of SCC with measurement devices a) normal operation, b) disturbed operation

IV. CONCLUSION

This work proposes a straightforward, reconfigurable architecture for SCC. The card was de-signed with the requirements of low-cost and low-power consumption. The SCC is demonstrated to be capable of attenuating signals for up to ± 15V and effectively filtering frequencies above 5k, 10k, 15k, 25k, and 50kHz through the use of a reconfigurable antialiasing filter. The output signal is restricted to a range of 0–3V by the SCC, and an isolated stage

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may be implemented for power electronics applications. The SCC is constructed using components that are readily available.

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