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FPGA-Based Real-Time 2D FIR Filter Implementation on DE10-Standard Board

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Abstract: *This paper presents the design, implementation, and validation of a 4×4 two-dimensional Finite Impulse Response (2D FIR) filter on an Intel Cyclone V FPGA development board (DE10-Standard). The architecture utilizes Verilog HDL with a pipelined convolution engine and a seven-state finite-state machine (FSM) for streaming data processing. Functional verification through RTL simulation in ModelSim and real-time hardware validation using Intel SignalTap Logic Analyzer confirm correct operation. Synthesis results demonstrate efficient resource utilization (< 5% logic elements, ~5% DSP blocks), timing closure at 108.6 MHz, and sustained throughput of ~10 M pixels/s. Bit-exact matching between simulation and hardware validates the design's correctness. The work demonstrates that FPGA-based 2D FIR filtering meets real-time constraints with minimal resource overhead, providing a scalable foundation for advanced image processing systems.*

Keywords: FPGA, 2D FIR filter, convolution, Verilog HDL, Cyclone V, FSM, pipelining, real-time image processing

I. INTRODUCTION

Digital image and signal-processing applications increasingly demand real-time performance, deterministic latency, and efficient resource utilization. Two-dimensional FIR (Finite Impulse Response) filters are fundamental operations in image and video processing, where each output pixel is computed via convolution with a fixed kernel over a neighborhood of input pixels.

The computational intensity of 2D convolution poses challenges for general-purpose processors and digital signal processors (DSPs). Field-Programmable Gate Arrays (FPGAs) provide an attractive alternative by offering reconfigurable logic, embedded multipliers, and on-chip memory for parallel and pipelined architectures. This enables real-time processing with deterministic latency—essential for applications such as medical imaging, industrial vision systems, and embedded camera systems.

This work presents a complete hardware realization of a 4×4 2D FIR filter using Verilog HDL on the Intel Cyclone V SoC (5CSEBA6U23I7N) device integrated in the DE10-Standard development platform. The design is verified through simulation and validated on real hardware using logic analysis tools. The primary objectives are: (1) design an efficient hardware architecture for streaming 2D convolution, (2) implement the design in Verilog HDL targeting the DE10-Standard board, (3) verify correctness through functional simulation, (4) synthesize and analyze resource and timing metrics, and (5) perform on-chip hardware validation.

II. PROBLEM STATEMENT

Traditional 2D FIR filters are computationally intensive and consume high power due to repetitive additions and multiplications, especially when processing high-resolution images in real time. This leads to significant hardware overhead and limits their suitability for embedded or low-power platforms. Therefore, there is a need for an efficient implementation that reduces the arithmetic load, optimizes hardware resource utilization, and still preserves the filtering accuracy required for practical image-processing applications.hat allows individuals with limited or no use of their

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hands to navigate their environment independently and safely using voice commands, ensuring affordability, accuracy, ease of use, and adaptability to different user needs."

III. METHODOLOGY

The project follows a systematic FPGA design methodology that begins with the mathematical definition of the 2D FIR filter and ends with real-time verification on hardware.Design considerations: Detail the chosen components and justification, such as selecting the Arduino for its Wi-Fi and Bluetooth capabilities and the L298N motor driver for controlling DC motors.

Algorithm Development

The 2D FIR filtering operation is defined as a convolution between a 4×4 coefficient kernel and a corresponding 4×4 pixel window from the input image. The convolution produces a single output pixel, and the window slides across the image to generate the filtered output.

RTL design in Verilog

The algorithm is mapped to hardware by describing the system in Verilog HDL as a set of modules: input buffer, coefficient memory, convolution engine, FSM-based controller, and output memory, all integrated in a top-level fir_system module

Simulation and verification (ModelSim)

An RTL testbench (tb_fir_system) is created to generate clock, reset, and start stimuli, observe FSM state transitions, and compare output_ram contents with expected convolution results using ModelSim Intel FPGA Edition.

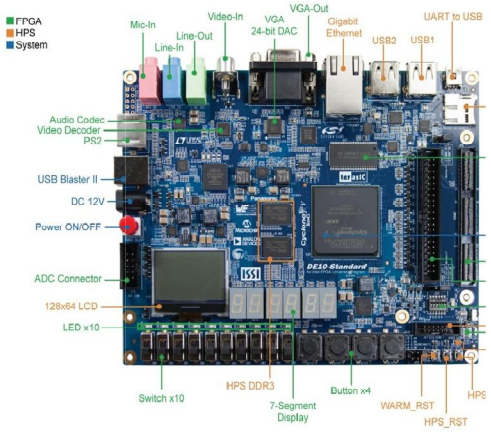
Synthesis and implementation (Quartus Prime)

The verified RTL is compiled in Intel Quartus Prime Lite; synthesis, fitting, and timing analysis are performed to generate the .sof configuration file and obtain resource utilization and Fmax reports for the Cyclone V device on the DE10-Standard board

Hardware testing and debugging (SignalTap)

The .sof file is downloaded to the DE10-Standard via USB-Blaster II, and Intel SignalTap Logic Analyzer is used to capture internal signals such as current_state, row_counter, col_counter, and filter_result to confirm correct real-time behavior and measure effective throughput and latency.

IV. HARDWARE COMPONENTS



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DE10-Standard FPGA Development Board

The DE10-Standard board provides a Cyclone V SoC FPGA with embedded DSP blocks, memory resources, and JTAG debugging support. It serves as the hardware platform for implementing the proposed design.

Cyclone V FPGA

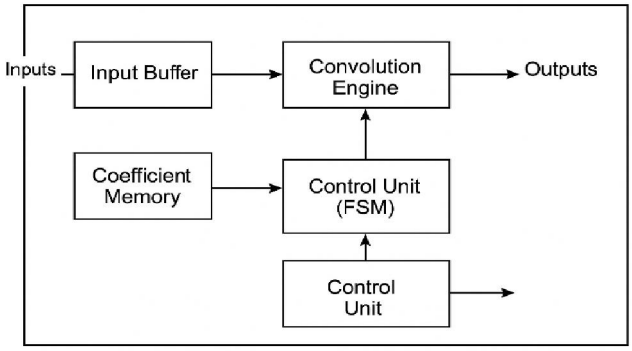
The Cyclone V FPGA offers logic elements, DSP blocks, and embedded memory blocks that are effectively utilized to implement the pipelined 2D FIR filter architecture.

On-Chip Memory

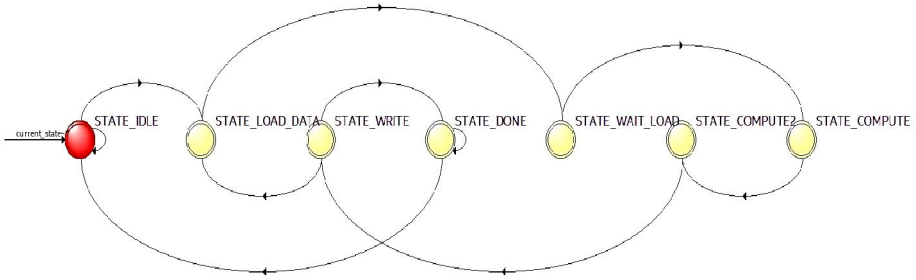
Internal RAM blocks are used to store filter coefficients, input image data, and output results, ensuring low-latency memory access.

V. CIRCUIT DIAGRAM

System Architecture



FSM control



The system architecture consists of an input buffer that forms a 4×4 sliding window of image pixels, a coefficient memory holding fixed kernel values, and a convolution engine performing parallel multiply–accumulate operations. An FSM controller coordinates data loading, computation, and output storage. The pipelined design enables continuous processing of input data with improved throughput.

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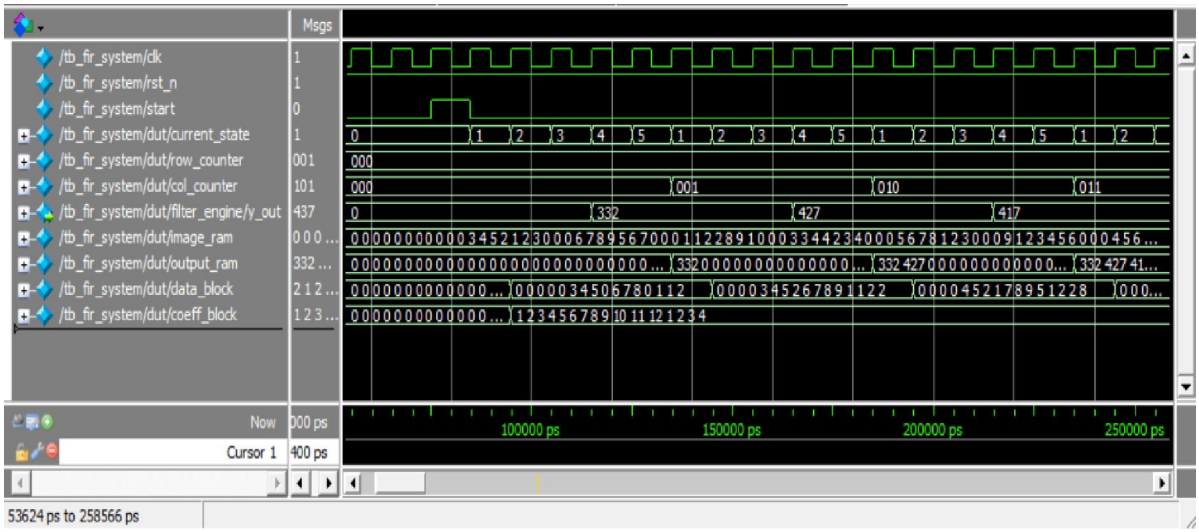
VI. RESULTS



Functional simulation confirms correct FSM operation and accurate convolution outputs. Synthesis results indicate successful timing closure with a maximum operating frequency of approximately 108 MHz. The design is tested at 50 MHz, achieving stable real-time operation. Hardware validation using SignalTap shows that the output signal aligns correctly with the write state of the FSM. The measured throughput is approximately 10 million pixels per second, demonstrating efficient real-time performance with low resource utilization.

VII. CONCLUSION

This paper presented the design and implementation of a real-time 4×4 2D FIR filter on an FPGA platform using Verilog HDL. The proposed architecture leverages parallel processing, pipelining, and FSM-based control to achieve deterministic real-time performance. Functional simulation and hardware validation confirm the correctness of the design.

The results demonstrate that FPGA-based implementations are well suited for real-time image processing applications requiring high throughput and efficient resource utilization. Future work includes extending the design to support larger kernel sizes and multi-channel image processing.

VIII. ACKNOWLEDGMENT

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