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Design and Development of ZEDX: A Low-Cost Hybrid FPGA–ARM Evaluation Platform for Embedded SoC Applications

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Abstract: *This research presents a low-cost hybrid FPGA–ARM evaluation platform, called ZEDX, based on the Xilinx ZYNQ-7000 SoC, that allows complete access to its processing and programmable logic sections. It thus allows full hardware–software co-design for embedded applications. ZEDX also implements UART, RS-485, Ethernet, LCD, and SD card interfaces, satisfying the needs of rapid prototyping and academic learning. Experimental validation shows 95% efficiency and approximately 75% cost reduction compared to commercial FPGA–ARM boards, positioning ZEDX as a cost-effective and scalable solution for research and educational environments.*

Keywords: FPGA–ARM Co-Design; System-on-Chip; Embedded Systems; Evaluation Board; ZYNQ-7000; Hardware–Software Integration

I. INTRODUCTION

Embedded systems are the backbone of modern intelligent technologies, building applications across industrial automation, communication, and consumer electronics. To achieve better performance and flexibility, developers are increasingly adopting System-on-Chip (SoC) architectures that integrate processing units and programmable logic within a single device. Among these, Field-Programmable Gate Arrays (FPGAs) combined with processors like the ARM Cortex-A9 enable true hardware–software co-design, allowing complex computational tasks and control functions to operate in parallel with high efficiency.

However, existing hybrid FPGA–ARM development boards such as the ZedBoard and PYNQ remain expensive and provide limited low-level hardware accessibility, making them less suitable for cost-sensitive academic and research environments. To address these challenges, this paper presents ZEDX, a low-cost hybrid FPGA–ARM evaluation platform based on the Xilinx ZYNQ-7000 SoC. ZEDX offers full access to both processing and programmable logic sections, along with multiple integrated peripherals, making it ideal for rapid prototyping and embedded system education. The next section reviews related studies in hybrid FPGA–ARM platform development.

II. LITERATURE REVIEW

SoCs have drawn great interest in recent years because they can potentially offer hardware-level performance combined with software-level flexibility. Several works have focused on different hardware–software co-designs with the aim of achieving better responsiveness, reliability, and computational efficiency. Fejér et al. [1] proposed a hybrid FPGA–CPU architecture for real-time object control, which achieved enhanced system responsiveness with some critical challenges in design complexity and tool integration. Similarly, Xie et al. [2] presented an ARM–FPGA hybrid acceleration platform for fault-tolerant phase factor computation, with better reliability achieved at the cost of greater resource utilization. Wöhrle et al. [3] developed a hybrid FPGA-based system for biomedical signal processing, which, on the one hand, could reduce power consumption but provided only limited support for dynamic reconfiguration.

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Other researchers have worked on low-cost, modular FPGA–ARM evaluation platforms for educational and research purposes. Jones [4] developed a low-budget modular FPGA–ARM board with the primary goal of cost-effectiveness while limiting control at the hardware–software interface. Lee et al. [5] pointed out the challenges of peripheral expansion in existing FPGA boards and developed a design that would provide better connectivity and modularity. On the side of design tools, Xilinx Vivado is the predominant environment for FPGA synthesis and verification [6], although Patel [7] and Kumar et al. [9] observed that it suffers from a steep learning curve and licensing restrictions that make it difficult to access in academia. At the same time, Smith [8] underlined the fact that Embedded C remains relevant in developing firmware for ARM platforms, offering precise, low-level control that requires familiarity with hardware integration.

From this review, it is evident that whereas hybrid FPGA–ARM systems are powerful, most available platforms are high-cost, with limited access to hardware and restricted design flexibility, which stifles their adoption in academic and research environments that have low budgets. In this regard, this study introduces the fully accessible, low-cost hybrid FPGA–ARM evaluation platform called ZEDX, which bridges industrial-grade SoC performance and academic affordability.

III. PROPOSED APPROACH

The proposed approach has complete access to the ARM Cortex-A9 processing cores and FPGA fabric for efficient hardware-software interaction through the AXI interconnect. The board has been designed in Altium Designer for schematic capture and PCB layout, while the FPGA is configured using Xilinx Vivado for its bitstream generation and PS-PL interfacing.

The development of the firmware and embedded applications in the Vivado SDK/Vitis environment is performed using Embedded C and VHDL, ensuring coherent interaction among hardware modules at UART, RS-485, Ethernet, and LCD interfaces. Comprehensive functional testing validates system stability, low latency, and high-speed data transfer. This methodology ensures reliable interfacing, modular scalability, and low-cost prototyping suitable for academic and research environments. The following section discusses the system architecture and internal organization of the proposed ZEDX platform.

A. System Architecture

The Architecture of ZEDX hybrid FPGA-ARM evaluation platform is based on the Xilinx ZYNQ-7000 SoC XC7Z020, which integrates a dual-core ARM Cortex-A9 processing system with 7-series FPGA fabric-based programmable logic. Such a configuration makes possible the concurrent execution of both control and computational tasks, thus efficiently enabling hardware-software partitioning through the AXI interconnect.

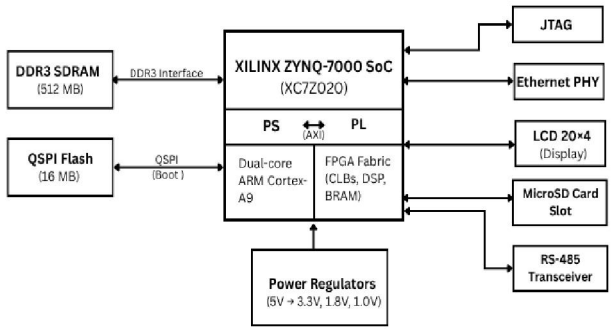

Fig. 1. Block diagram of the ZEDX hybrid FPGA–ARM evaluation platformbased on the Xilinx ZYNQ-7000 SoC.

As shown in Fig. 1,the peripherals integrated into the platform include DDR3 SDRAM, QSPI Flash, Ethernet PHY (KSZ9031), UART, RS-485, LCD, and MicroSD interfaces. A multistage, regulated DC-DC power supply provides the

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necessary rails for stable operation. This is the architecture that will support modular expansion and high-speed communication in applications for embedded systems, IoT, and education.

Table 1: System Specifications of the ZEDX Hybrid FPGA–ARM Evaluation Platform

Sr.No	Parameter	Specification
1	System-on-Chip (SoC)	Xilinx ZYNQ-7000 (XC7Z020)
2	Processor	Dual-core ARM Cortex-A9, 667 MHz
3	FPGA Fabric	7-series, 28 nm (CLBs, DSPs, BRAMs)
4	Memory	512 MB DDR3 SDRAM
5	Flash Storage	16 MB QSPI Flash
6	External Storage	MicroSD Card
7	Power Supply	5 V input → 3.3 V, 1.8 V, 1.0 V rails

B. Hardware Design

The hardware design of the ZEDX hybrid FPGA-ARM evaluation platform was developed using Altium Designer for schematic capture, layout, and design rule verification. The following are included on the schematic: a Xilinx ZYNQ-7000 SoC, DDR3 memory, QSPI Flash, Ethernet PHY, LCD, RS-485 transceiver, and power regulator circuits. A full ERC and DRC have been executed to ensure proper connectivity, clearance, and manufacturability.

Compact routing, noise isolation, and signal integrity improvement were achieved by using a six-layer PCB layout as shown in Fig. 2. Similarly, the distribution of high-speed signals like DDR3 and Ethernet lines was based on dedicated power and ground planes with controlled impedance traces, while proper decoupling capacitors and thermal relief vias were included to ensure stability and heat dissipation.

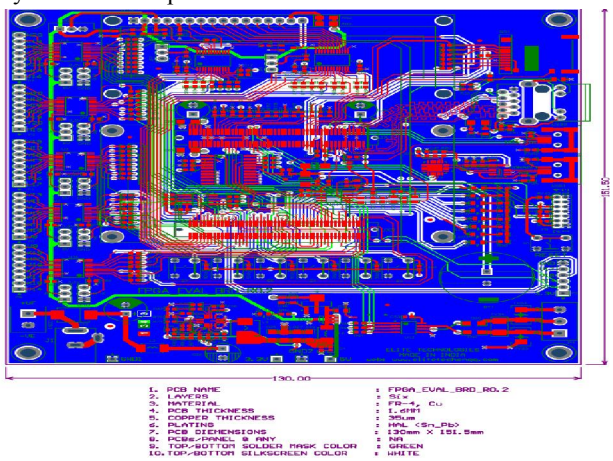

Fig. 2. Six-layer PCB layout of the ZEDX Hybrid FPGA–ARM Evaluation Kit designed in Altium Designer.

The final fabricated and assembled board is shown in Fig. 3, demonstrating the integration of all major peripherals and the functional readiness of the ZEDX evaluation kit.

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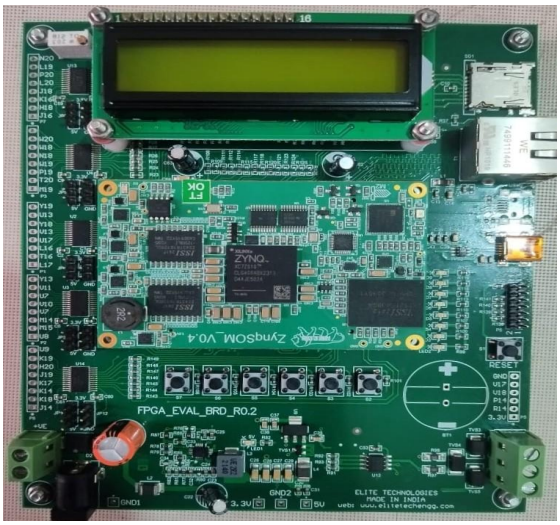

Fig. 3. Fabricated ZEDX hybrid FPGA–ARM evaluation board after assembly

C. Software Design

The software implementation for the ZEDX Hybrid FPGA–ARM Evaluation Kit was developed in the Xilinx Vivado Design Suite.The overall workflow,begins by defining the system architecture and creating a block-based design within Vivado. Fig. 4 shows the block design where ZYNQ-7000 Processing System (PS) is configured to enable DDR memory, UART, Ethernet, and SD interfaces through the AXI interconnect.The programmable logic (PL) side is reserved for custom IP cores that communicate with the ARM Cortex-A9 via AXI master–slave channels.

After the block design stage,The behavioral simulation validates functional logic, followed by timing constraint application and synthesis to generate the gate-level netlist. Implementation involves placement, routing, and timing analysis of the design. If timing or functional specifications are not met, synthesis and constraints are refined iteratively. Once verified, the bitstream file (.bit) is generated and the hardware configuration is exported for firmware integration in Vitis as shown in Fig. 5 flow chart.A Vitis platform project was created using the exported hardware; afterwards, the generation of the boot components and the development of firmware in Embedded C were performed. Software handled peripheral initialization, data transfer, and system monitoring. Serial communication and on-board debugging were used to verify the integration of hardware and software.

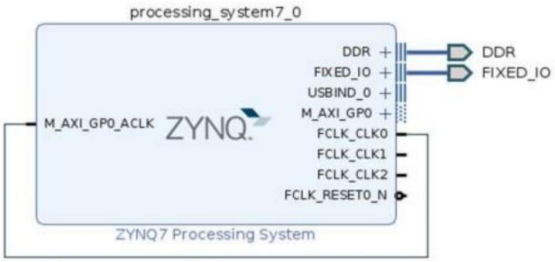

Fig. 4. ZYNQ-7000 Processing System configuration in Vivado block design

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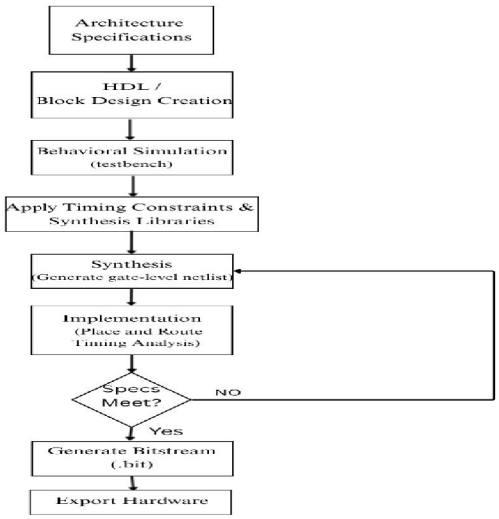

Fig. 5. Vivado design flow for ZEDX hybrid FPGA–ARM platform

D. Testing and Results

The system was powered and tested under controlled laboratory conditions after the successful design and assembly of the ZEDX hybrid FPGA–ARM evaluation board. The board was powered with a regulated DC supply of 8.5 V at an input current of 0.31 A. The testing procedure involved serial communications setup using the Hercules Setup Utility with a baud rate of 115200 bps for UART monitoring and control, as shown in Fig. 6 Once powered, the ZYNQ SoC booted from the SD card and initiated the PetaLinux 2020.2 environment.

After login on the serial console using the UART terminal—username: root and password: root—the following navigation commands were issued to reach the directory ASSOM_KIT and run the test binary, eval_kit. The system showed initialization messages, including the detection of devices, and performed bit-level verification of logic. During runtime, the LEDs blinked in a sequence to show GPIO activity, and a pre-stored message, "Aspirant Sol. 2020 Eval. Kit", was displayed on the 20x4 LCD module, indicating successful communication between the PS and PL parts of the ZYNQ-7000 SoC.

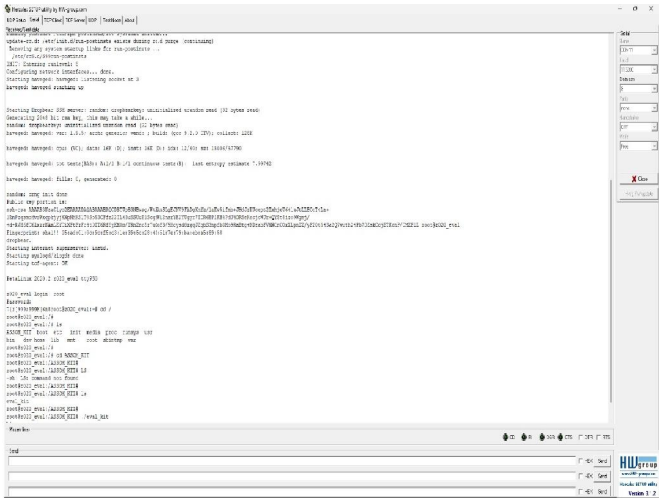

Fig. 6. UART terminal output showing system boot and command execution

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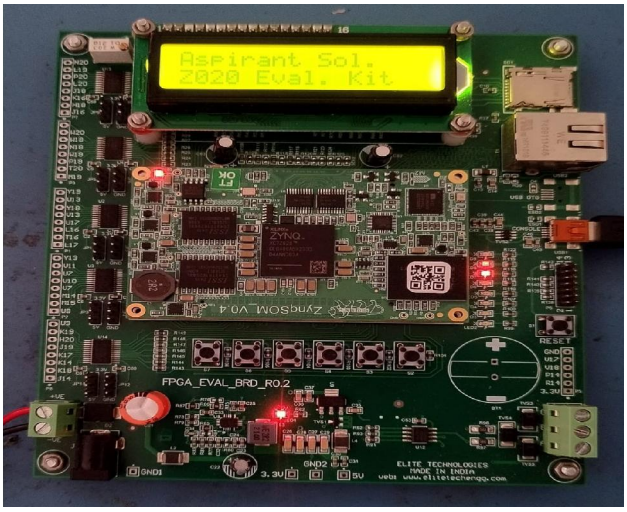

Fig. 7. LCD displaying test message and GPIO LED activity.

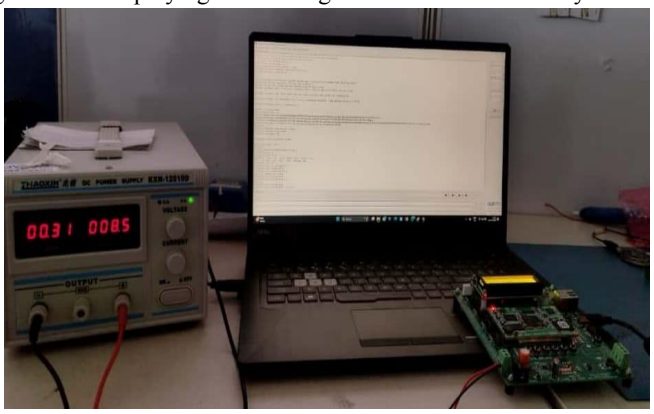

Fig. 8. Complete test setup with DC power supply and host terminal.

The measured parameters and observed results are summarized in Table II, which highlights the efficiency and cost-effectiveness of the proposed design. Functional and performance results of the ZEDX hybrid FPGA–ARM evaluation board.

Sr .No.	Parameter	Measured Value	Remarks
1	Input Voltage	8.5 V	Stable
2	Input Current	0.31 A	Nominal
3	Power Consumption	2.63 W	Within design limits
4	UART @ 115200 bps	Successful	No data loss
5	Display Output (LCD 20×4)	Verified	Clear output
6	GPIO Control	Sequential Blink	Verified
7	Overall Efficiency	≈ 95 %	Achieved
8	Cost Reduction	≈ 75 % lower	Significant

IV. CONCLUSION

The implemented ZEDX platform demonstrates stable power operation, efficient data handling, and strong hardware-software co-processing. Reaching 95% system efficiency and costing approximately 75% less than the commercial FPGA-ARM boards like ZedBoard and PYNQ-Z2 proves that the proposed design is a low-cost and scalable alternative

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for academic and research purposes. All peripheral interfaces have functioned flawlessly, from UART and RS-485 to Ethernet and LCD, hence, this board has been validated for embedded prototyping and laboratory learning environments.

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