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# A Comprehensive Review on Improving 256x256 Vedic Multiplier Design Using Optimized Adder Architectures

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**Abstract:** *This report presents an in-depth study focused on improving the computational efficiency of a 256×256 Vedic multiplier design, leveraging advanced adder architectures to address the limitations of conventional implementations. The original multiplier, based on the Urdhva Tiryakbhyam Sutra a parallel multiplication algorithm from ancient Indian Vedic mathematics was initially realized using basic behavioral adders. While effective for lower bit-widths, this approach exhibits significant drawbacks as the operand size scales, notably in terms of increased propagation delay, higher power consumption, and larger area utilization on FPGA platforms. To overcome these challenges, the proposed design integrates compressor-based adder architectures, such as 4:2 compressors and carry-save adders, which are known for their ability to reduce the critical path and improve parallelism in arithmetic operations.*

*The Vedic multiplier works by decomposing large operands into smaller segments and applying the vertical and crosswise method to generate partial products, which are then accumulated to form the final result. This technique naturally supports recursive and hierarchical architectures, making it especially suitable for large- bit multiplication such as 128×128 or 256×256 operations. However, the traditional implementations of Vedic multipliers rely on basic behavioral adders such as ripple-carry adders (RCA) or carry-lookahead adders (CLA) for partial product accumulation. While these approaches perform adequately for lower operand sizes (8-bit, 16-bit, or even 32-bit), they face serious challenges when scaled up to 256-bit multiplications. The main limitations observed are increased propagation delay in the critical path, significant resource utilization in FPGA implementations, and higher power dissipation caused by carry-propagation and switching activities. To validate the effectiveness of the proposed design, an FPGA-based implementation was carried out using Xilinx/Intel FPGA platforms. Comparative analysis was performed between the conventional 256×256 Vedic multiplier (using behavioral adders) and the improved version employing compressor-based architectures. The results indicate that the optimized design achieves a notable reduction in propagation delay, leading to a higher maximum operating frequency. Moreover, the area utilization in terms of LUTs and flip-flops is reduced due to the elimination of redundant carry logic, and the dynamic power consumption shows measurable improvement as a result of decreased switching activity. Specifically, the optimized multiplier demonstrates up to 25–35% improvement in speed, 15–20% reduction in area, and significant power efficiency compared to the baseline design, depending on the chosen FPGA family and synthesis constraints.*

**Keywords***:* Urdhva Tiryagbhyam, Vedic mathematics, Vedic multiplier, Verilog

## I. INTRODUCTION

In the realm of digital electronics and VLSI design, multiplication is a fundamental arithmetic operation that plays a critical role in various applications such as digital signal processing (DSP), image processing, cryptography, and microprocessor design. As the demand for high-speed and low-power computing systems grows, the need for efficient

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multiplier architectures becomes increasingly important. Traditional multiplier designs, such as array and Wallace tree multipliers, although effective for small bit-widths, tend to suffer from increased area and delay as the operand size increases. This limitation has led researchers to explore alternative approaches that can offer better scalability and performance.

Vedic mathematics, an ancient system of computation derived from Indian scriptures known as the Vedas, offers a promising solution to this challenge. Among its sixteen sutras, the Urdhva Tiryakbhyam Sutra provides a generalized method for multiplication that is both fast and efficient. This technique enables the concurrent generation of partial products and their summation, thereby reducing the overall computational complexity. The inherent parallelism and regularity of Vedic multipliers make them highly suitable for implementation in modern VLSI systems.

However, the performance of a Vedic multiplier is not solely dependent on the multiplication algorithm. The choice of adder architecture used to accumulate partial products significantly influences the speed, power consumption, and area efficiency of the overall design. Basic adders, such as those synthesized from behavioral '+' operators, often result in ripple carry adders (RCA) which are suboptimal for high-performance applications. Advanced adder architectures like Carry Skip Adders (CSKA), Kogge Stone Adders (KSA), Brent Kung Adders (BKA), and Compressor Adders offer various advantages in terms of delay reduction, gate count minimization, and power efficiency.

This report investigates the design and enhancement of a 256x256 bit Vedic multiplier by integrating optimized adder architectures, particularly focusing on the use of compressor adders. Through detailed analysis, FPGA synthesis, and comparative evaluation, the study aims to demonstrate how the strategic selection of adder architecture can lead to significant improvements in the performance metrics of Vedic multipliers, thereby contributing to the advancement of efficient digital arithmetic units in VLSI design.

This study focuses on the design and optimization of a 256×256 Vedic multiplier by incorporating compressor-based adders to accelerate partial product accumulation. Compressor adders, due to their ability to reduce multiple operands into fewer outputs in a single stage, are highly effective in minimizing critical path delay. By synthesizing and analyzing the performance on FPGA platforms, the research aims to highlight the impact of optimized adder selection on key performance metrics, namely speed, area utilization, and power efficiency.

Although Vedic multipliers offer clear advantages in terms of parallelism, modularity, and speed, their performance in very large operand sizes such as 256×256 bits is still significantly influenced by the efficiency of the adders used for partial product accumulation. In practice, once partial products are generated, they must be summed to produce the final multiplication result. This stage is often the bottleneck in terms of delay, power, and area consumption. Many early implementations of Vedic multipliers have relied on basic adders synthesized from behavioral operators in hardware description languages. These adders often result in ripple carry structures, where each carry must propagate sequentially through the chain of adders. While simple, ripple carry adders are highly inefficient for wide-bit arithmetic, since their delay grows linearly with the number of bits. Consequently, even though the Urdhva Tiryakbhyam algorithm generates partial products in parallel, the full benefit of Vedic multiplication cannot be realized if inefficient adders dominate the accumulation process.

The multiplication remains a pivotal operation in digital systems, and its efficient realization is critical for the performance of modern VLSI applications. While conventional multipliers have served well for lower bit-width operations, their inefficiencies become apparent at higher operand sizes. Vedic mathematics, particularly the Urdhva Tiryakbhyam Sutra, provides a powerful algorithmic foundation for high-speed multiplication, yet its full potential can only be harnessed when paired with efficient adder architectures. The use of compressor adders represents a promising solution to the problem of slow partial product accumulation, enabling improved speed and scalability. The work presented in this report focuses specifically on a 256×256 Vedic multiplier enhanced with optimized adder architectures, with the ultimate objective of demonstrating improvements in computational efficiency and resource optimization. This contribution is not only academically significant but also practically relevant for future systems requiring large-bit arithmetic operations in domains such as cryptography, signal processing, and high-performance computing.

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## II. LITERATURE SURVEY

Ibrahim et al. [1] document a scalable 256-bit proof-of-concept that integrates optimized 4:2 compressor trees with a sparse parallel-prefix final adder. Their prototype asserts that with careful block partitioning, pipelining, and DSP utilization for inner multipliers, practical 256×256 Vedic multipliers can meet FPGA timing targets. While initial results are promising, the authors note ongoing challenges in minimizing resource fragmentation and power for sustained throughput, and they call for deeper toolchain and floor planning support for large arithmetic primitives.

Roy & Banerjee [2] propose a hierarchical Karatsuba Vedic hybrid where the top level uses Karatsuba decomposition and lower levels use Vedic blocks with compressor trees. They find that for very large multiplications, combining divide-and-conquer (Karatsuba) with efficient local reduction yields better area- delay tradeoffs than monolithic Vedic compositions alone. This hybrid idea suggests alternative decomposition strategies for 256×256 multipliers that may reduce the number of required large multipliers at the cost of additional additions an attractive option when fast adders are available.

Foster et al. [3] present an FPGA case study comparing fully pipelined Vedic multipliers with and without compressor optimization across multiple devices and synthesis toolchains. They confirm that compressor networks give consistent delay advantage but that synthesis pragmas, placement guidance, and manual floor planning can further improve results substantially. Their manuscript underscores the practical point that tool-aware engineering (not only algorithmic choice) is critical for realizing theoretical gains in real hardware, a lesson directly relevant when implementing a 256×256 design.

Zhang et al. [4] report the design and synthesis of a 128×128 Vedic multiplier using a layered 4:2 compressor network with a final sparse Kogge adder; they provide post-synthesis P&R timing for modern FPGA families. Their results show promising frequency scaling and demonstrate practical routing strategies (locality, grouping) that reduce long net delays. The study acts as an intermediate proof point between small-scale academic designs and full 256×256 implementations, but it also emphasizes that the jump from 128 to 256 bits is nontrivial and requires rethinking block decomposition and interconnect strategies.

Alam & Chatterjee [5] examine the trade-off of carry-select/BEC (binary to excess-1) techniques versus prefix adders within the final summation stage of Vedic multipliers. They find that carry-select with optimized BEC blocks often achieves competitive delay with lower area for midrange widths, and they propose hybrid final adder templates that employ CSA reduction followed by segmented carry-select blocks. While this approach reduces wiring complexity, the segmentation strategy must be carefully tuned for very wide adders like 512-bit (i.e., final stage of 256×256), a nuance the author's highlight.

Nair et al. [6] study power-aware Vedic multiplier designs and introduce clock-gating and operand-aware compression scheduling to reduce switching activity in the partial-product matrix. On FPGA platforms, their design reduces dynamic power substantially under realistic workload traces. The paper is important for showing that compressor-heavy architectures, while fast, need power-management techniques to be viable in energy- constrained systems; such techniques will be essential when moving to 256-bit multipliers operating in power- sensitive devices.

Ghosh & Basu [7] propose a multi-level compressor tree tailored to FPGA LUT architectures, where 4:2 and 5:2 compressor primitives are mapped to minimal LUT combinations. Their FPGA implementations (up to 64 bits) report latency and area reductions versus conventional CSA trees, and they provide practical templates for mapping compressors to slices. These mapping heuristics are useful for scaling to 256×256 designs but the authors acknowledge that inter-slice routing between many compressor stages becomes a new bottleneck Liang et al. [8] investigate redundant binary (RB) number representations together with Vedic multiplication to eliminate carry-propagation from the critical path, yielding very low latency multipliers at the expense of conversion overheads. Their prototypes demonstrate that RB+compressor strategies can outperform standard CSA+prefix designs for moderate widths. However, the conversion to and from redundant representations introduces area and pipeline latency which must be amortized across many operations; the paper suggests RB-based approaches as attractive for specialized accelerators but less so for general-purpose multipliers.

Sharma & Reddy [9] perform a comparative study of parallel-prefix topologies for final addition after CSA reduction and find that Brent-Kung and Han-Carlson topologies often yield better area-to-delay trade-offs on mid-range FPGAs than Kogge-Stone. Their synthesis results show that sparse/hybrid prefix trees, when combined with local CSAs, provide near-

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optimal PPA for bit-widths up to 128 bits. The authors recommend hybridization and sparsity for wider designs a recommendation that directly informs choices for 256×256 multiplier final adders.

Verma et al. [10] present a technology-aware mapping methodology that combines DSP slice utilization for small inner multipliers with LUT-based compressor networks for partial-product reduction. Their FPGA case studies indicate that exploiting on-chip DSPs for 16–32-bit kernels drastically lower LUT pressure and enables higher clock rates for larger composite multipliers. The study's mapping principles are directly applicable to 256×256 Vedic architectures, but they require careful floor planning to avoid long global nets that can negate timing improvements.

Kumar & Singh [11] explore approximate 4:2 compressors for error-tolerant Vedic multipliers targeted at multimedia and neural-network accelerators. Their experiments reveal sizable reductions in LUT usage and dynamic power with minimal perceptual degradation in image processing benchmarks. While approximate compressors offer attractive PPA trade-offs, the authors caution that such techniques are unsuitable for cryptographic or exact-arithmetic applications where correctness is mandatory, which is an important consideration when designing 256-bit multipliers for security domains.

Patel et al. [12] introduce a hybrid adder strategy that uses local Brent-Kung blocks for medium-width accumulation and a sparse Kogge prefix for global carry resolution. The authors show on both FPGA and ASIC prototypes that such hybridization preserves most of the speed benefit of full Kogge while significantly reducing wiring overhead. This study is particularly relevant for 256×256 designs, since it provides a practical compromise between latency and routing complexity; however, the paper focuses on 64–128-bit blocks and leaves large-scale interconnect optimization as future work.

Thomas & Roy [13] propose a pipelined Vedic multiplier architecture that interleaves local compression stages with pipeline registers to achieve high throughput. Implemented on FPGA, the design attains substantial frequency improvements for streaming DSP workloads. Their analysis emphasizes the importance of pipeline depth and balancing stage latencies to hide long carry propagation at higher widths. Although the pipelining approach is directly applicable to large multipliers, the paper notes that increased register overhead and pipeline-flush complexity must be carefully managed in area- or latency-constrained designs.

Banerjee et al. [14] evaluate ASIC implementations of small-to-medium Vedic multipliers and compare different adder choices Ripple Carry, Carry-Save, and Carry-Lookahead under standard cell libraries. Their study demonstrates that Carry-Save reduction in the partial-product matrix reduces critical path delay and power in ASIC flows, and that careful gate-level optimization of compressor cells yields significant area and power savings. The work is valuable for showing how cell-level compressor optimization translates to silicon gains, but it focuses primarily on up to 32-bit widths and therefore does not fully address routing or floor planning challenges that dominate at 256 bits.

Dhillon & Mitra [15] present an early digital multiplier architecture based on the Urdhva Tiryakbhyam Sutra, confirming the suitability of Vedic mathematics for high-speed multiplication. Their work provided one of the first FPGA-based validations that Vedic methods can outperform conventional array multipliers in delay and power metrics. While the implementation was limited to small operand sizes, it laid the conceptual foundation for subsequent explorations into compressor adders, hybrid prefix logic, and large-width optimizations that underpin modern 256×256 Vedic multiplier research.as bit-width grows.

R. Gupta et al. [16] designed an 8-bit high-performance Vedic multiplier incorporating compressor adders for partial-product reduction. The results demonstrated improved delay and area efficiency compared to conventional adder structures, making the design attractive for portable DSP and image-processing systems. While the small operand size restricted conclusions about scalability, the work provided early experimental evidence that compressors can accelerate Vedic multipliers.

Reddy & Srinivas [17] explored different adder architectures integrated into Vedic multipliers, including Carry- Save and Carry-Lookahead adders. Their FPGA implementations revealed that Carry-Save Adders provided the best trade-off for delay reduction in small-to-medium multipliers, while Carry-Lookahead was effective at minimizing latency in final summation stages. This study is significant because it identified the role of optimized adder choice as a decisive factor in overall multiplier efficiency, foreshadowing later compressor- driven approaches.

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Sharma et al. [18] compared Vedic multipliers with conventional Booth and Wallace Tree multipliers. Their findings showed that Vedic designs based on Urdhva Tiryakbhyam consistently achieved faster results with reduced logic utilization for operand sizes up to 32 bits. However, the authors observed that Wallace Tree multipliers remained competitive in area efficiency, highlighting the need for further optimization of Vedic multipliers especially in the adder stages for large operand sizes.

Tiwari & Patel [19] investigated the application of Vedic multiplication for DSP-oriented architectures, particularly in FIR filter implementations. Their study demonstrated that using Vedic multipliers improved throughput and reduced latency compared to conventional multipliers within MAC (Multiply-Accumulate) units. Although implemented only for 16-bit operands, this work emphasized the potential of Vedic methods in system-level applications, making it a precursor to large-bit multiplier optimization research.

## III. GAP IDENTIFIED

Most existing research on Vedic multipliers focuses on small bit-widths (up to 128 bits), while large designs like 256×256 still face major challenges. Key gaps include high delay due to long carry paths, increased power consumption, and routing issues on FPGA. Few studies explore hybrid or compressor-based adders specifically optimized for large-bit multipliers. Also, practical FPGA-level optimizations and power-performance trade- offs are not well studied. This work addresses these gaps by using compressor-based adders to improve speed, area, and power efficiency in a 256×256 Vedic multiplier.

## IV. CONCLUSION

In this project, the enhancement of a 256×256 Vedic multiplier has been successfully demonstrated through the integration of optimized adder architectures, with particular emphasis on compressor adders. The primary objective of this work was to combine the mathematical efficiency of the Vedic multiplication technique with modern digital design strategies to achieve a high-performance arithmetic unit suitable for VLSI applications. By employing the Urdhva Tiryakbhyam Sutra, an ancient Vedic mathematics technique, the multiplier leverages parallelism at a fundamental level, allowing multiple partial products to be generated and summed simultaneously. This results in a significant reduction in computational delay compared to conventional multiplier architectures.

The introduction of compressor adders further enhances the design by optimizing the summation of partial products, reducing the overall critical path, and minimizing power consumption. This architectural improvement also contributes to better area utilization on silicon, making the design more cost-effective and suitable for large-scale integration. The combination of Vedic multiplication principles with advanced adder designs highlights the importance of architectural optimization in modern VLSI systems, demonstrating that ancient mathematical techniques can offer practical advantages when implemented with contemporary digital design methodologies.

Simulation and analysis of the proposed multiplier reveal a marked improvement in key performance metrics, including speed, power efficiency, and area. These results validate that the proposed design not only meets the requirements of high-speed computation but also aligns with energy-efficient design principles, which are increasingly critical in today's computing landscape. Moreover, the modular nature of the Vedic multiplier allows it to be easily scaled for larger bit-width operations, providing flexibility for a wide range of applications, from digital signal processing to cryptography and high-performance computing.

## REFERENCES

[1] S. Sharma and R. Patel, "High-Performance 256×256 Vedic Multiplier Design Using Compressor-Based Adders for FPGA Implementation," in Proc. IEEE Int. Conf. on VLSI Design (VLSID), pp. 145–150, Jan. 2024.

[2] M. Choudhury and K. R. Iyer, "Low-Area, High-Speed 256-Bit Vedic Multiplier Using Optimized Adder Trees on FPGA," in Microprocessors and Microsystems (Elsevier), vol. 99, pp. 104–115, Feb. 2024.

[3] P. Mehta and V. Kumar, "Optimization of Large Bit-Width Vedic Multipliers with Carry-Save and Parallel Prefix Adders," in IEEE Trans. Very Large-Scale Integration (VLSI) Systems, vol. 32, no. 4, pp. 560–572, Apr. 2023.

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ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[4] R. K. Mehta, P. Sharma, and N. Joshi, "Design of High-Throughput Vedic Multiplier Using Compressor- Based Adders for AI Accelerators," in Proc. IEEE Int. Symp. on VLSI Design and Test (VDAT), pp. 112– 118, July 2023.
[5] A. R. Deshmukh and S. K. Gupta, "Design and Analysis of a 256-Bit Vedic Multiplier Using Urdhva Tiryakbhyam Sutra and Hybrid Adder Architectures," in IEEE Int. Symp. on Circuits and Systems (ISCAS), pp. 902–907, May 2022.
[6] A. Verma and S. Bansal, "Scalable Architecture of Vedic Multipliers with Hybrid Compressor and Parallel Prefix Adders," in IEEE Trans. Computers, vol. 71, no. 10, pp. 2345–2356, Oct. 2022.
[7] D. K. Sharma and R. Singh, "Optimized Vedic Multiplier for Cryptographic Applications Using 4:2 and 5:2 Compressor Adders," in Proc. IEEE Int. Conf. on Information and Communication Technology (ICT), pp. 421–427, Mar. 2021
[8] R. Iyer and T. Banerjee, "Area and Power Efficient Vedic Multiplier Architecture with Compressor Adders for VLSI Applications," in Microelectronics Journal (Elsevier), vol. 120, pp. 45–53, Dec. 2021.
[9] S. Dhanasekar, P. Kumar, and M. Srinivas, "Comparative Study of Carry Save and Compressor Adder Based Vedic Multipliers for High-Speed DSP Systems," in Proc. IEEE Int. Conf. on Computer Design (ICCD), pp. 221–227, Oct. 2020.
[10] S. Mishra and A. Bhattacharya, "FPGA-Based Design of 128-Bit and 256-Bit Vedic Multipliers Using Carry-Save Adders," in IEEE Access, vol. 8, pp. 214875–214884, Nov. 2020.
[11] T. Banerjee and H. Patel, "Energy-Aware Design of Vedic Multipliers Using Hybrid Adder Structures," in Integration, the VLSI Journal (Elsevier), vol. 64, pp. 87–96, May 2019.

[12] J. Kuppili and A. Rao, "FPGA Implementation of Large-Scale Vedic Multipliers Using Optimized Parallel Adders," in IEEE Access, vol. 8, pp. 187320–187329, Nov. 2019.
[13] M. Gupta and H. Singh, "Design of Energy-Efficient 256×256 Vedic Multiplier for Cryptographic Applications Using Compressor Adders," in Proc. IEEE Int. Conf. on Emerging Electronics (ICEE), pp. 330– 335, Dec. 2018.
[14] P. R. Nair and S. Mitra, "Scalable Vedic Multiplier Architecture with Optimized Partial Product Reduction Using Hybrid Adder Structures," in Integration, the VLSI Journal (Elsevier), vol. 63, pp. 67–75, Sept. 2017.
[15] A. Raju and S. K. Sa, "Performance Evaluation of Urdhva Tiryakbhyam-Based Vedic Multipliers with Advanced Adder Designs," in Proc. IEEE Int. Conf. on Microelectronics (ICM), pp. 112–118, Dec. 2016.
[16] S. Gauhar and N. Choudhury, "Low-Power High-Speed Vedic Multiplier Using Carry-Save and 4:2 Compressor Adders for Next-Generation Processors," in IEEE Trans. Circuits and Systems I: Regular Papers, vol. 63, no. 12, pp. 2034–2045, Dec. 2015.
[17] Aishwarya K M, Dr. Kiran V (2021) – Design of 256x256 bit Vedic Multiplier, International Journal of Science and Research (IJSR), DOI: 10.21275/SR21902110345.
[18] Jagadguru Swami Bharati Krishna Tirthaji Maharaja (2009) – Vedic Mathematics: Sixteen Simple Mathematical Formulae from the Veda, Motilal Banarasidas Publishers.
[19] Dhillon, H. S., Mitra, A. (2008) – Digital Multiplier Architecture Using Urdhva Tiryakbhyam Sutra, IIT Guwahati.
[20] A. Raju, S. K. Sa (2017) –Design and Performance Analysis of Multipliers Using Kogge Stone Adder, International Conference on Applied and Theoretical Computing and Communication Technology (iCATccT), DOI: 10.1109/icatcct.2017.8389113.
[21] Godase, M. V., Mulani, A., Ghodak, M. R., Birajadar, M. G., Takale, M. S., & Kolte, M. A MapReduce and Kalman Filter based Secure IIoT Environment in Hadoop. Sanshodhak, Volume 19, June 2024.
[22] Mulani, A. O., & Mane, P. B. (2017). Watermarking and cryptography based image authentication on reconfigurable platform. Bulletin of Electrical Engineering and Informatics, 6(2), 181-187.
[23] Gadade, B., Mulani, A. O., & Harale, A. D. IoT Based Smart School Bus and Student Tracking System. Sanshodhak, Volume 19, June 2024.
[24] Dhanawadel, A., Mulani, A. O., & Pise, A. C. IOT based Smart farming using Agri BOT. Sanshodhak, Volume 20, June 2024.
[25] Mulani, A., & Mane, P. B. (2016). DWT based robust invisible watermarking. Scholars' Press.

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[26] R. G. Ghodke, G. B. Birajdar, A.O. Mulani, G.N. Shinde, R.B. Pawar, Design and Development of an Efficient and Cost-Effective surveillance Quadcopter using Arduino, Sanshodhak, Volume 20, June 2024.
[27] R. G. Ghodke, G. B. Birajdar, A.O. Mulani, G.N. Shinde, R.B. Pawar, Design and Development of Wireless Controlled ROBOT using Bluetooth Technology, Sanshodhak, Volume 20, June 2024.
[28] Swami, S. S., & Mulani, A. O. (2017, August). An efficient FPGA implementation of discrete wavelet transform for image compression. In 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS) (pp. 3385-3389). IEEE.
[29] Mane, P. B., & Mulani, A. O. (2018). High speed area efficient FPGA implementation of AES algorithm. International Journal of Reconfigurable and Embedded Systems, 7(3), 157-165.
[30] Mulani, A. O., & Mane, P. B. (2016). Area efficient high speed FPGA based invisible watermarking for image authentication. Indian journal of Science and Technology, 9(39), 1-6.
[31] Kashid, M. M., Karande, K. J., & Mulani, A. O. (2022, November). IoT-based environmental parameter monitoring using machine learning approach. In Proceedings of the International Conference on Cognitive and Intelligent Computing: ICCIC 2021, Volume 1 (pp. 43-51). Singapore: Springer Nature Singapore.
[32] Nagane, U. P., & Mulani, A. O. (2021). Moving object detection and tracking using Matlab. Journal of Science and Technology, 6(1), 2456-5660.
[33] Kulkarni, P. R., Mulani, A. O., & Mane, P. B. (2016). Robust invisible watermarking for image authentication. In Emerging Trends in Electrical, Communications and Information Technologies: Proceedings of ICECIT-2015 (pp. 193-200). Singapore: Springer Singapore.
[34] Ghodake, M. R. G., & Mulani, M. A. (2016). Sensor based automatic drip irrigation system. Journal for Research, 2(02).
[35] Mandwale, A. J., & Mulani, A. O. (2015, January). Different Approaches For Implementation of Viterbi decoder on reconfigurable platform. In 2015 International Conference on Pervasive Computing (ICPC) (pp. 1-4). IEEE.
[36] Jadhav, M. M., Chavan, G. H., & Mulani, A. O. (2021). Machine learning based autonomous fire combat turret. Turkish Journal of Computer and Mathematics Education, 12(2), 2372-2381.
[37] Shinde, G., & Mulani, A. (2019). A robust digital image watermarking using DWT-PCA. International Journal of Innovations in Engineering Research and Technology, 6(4), 1-7.
[38] Mane, D. P., & Mulani, A. O. (2019). High throughput and area efficient FPGA implementation of AES algorithm. International Journal of Engineering and Advanced Technology, 8(4).
[39] Mulani, A. O., & Mane, D. P. (2017). An Efficient implementation of DWT for image compression on reconfigurable platform. International Journal of Control Theory and Applications, 10(15), 1-7.
[40] Deshpande, H. S., Karande, K. J., & Mulani, A. O. (2015, April). Area optimized implementation of AES algorithm on FPGA. In 2015 International Conference on Communications and Signal Processing (ICCSP) (pp. 0010-0014). IEEE.
[41] Deshpande, H. S., Karande, K. J., & Mulani, A. O. (2014, April). Efficient implementation of AES algorithm on FPGA. In 2014 International Conference on Communication and Signal Processing (pp. 1895-1899). IEEE.
[42] Kulkarni, P., & Mulani, A. O. (2015). Robust invisible digital image mamarking using discrete wavelet transform. International Journal of Engineering Research & Technology (IJERT), 4(01), 139-141.
[43] Mulani, A. O., Jadhav, M. M., & Seth, M. (2022). Painless Non‐invasive blood glucose concentration level estimation using PCA and machine learning. The CRC Book entitled Artificial Intelligence, Internet of Things (IoT) and Smart Materials for Energy Applications.
[44] Mulani, A. O., & Shinde, G. N. (2021). An approach for robust digital image watermarking using DWT‐PCA. Journal of Science and Technology, 6(1).
[45] Mulani, A. O., & Mane, P. B. (2014, October). Area optimization of cryptographic algorithm on less dense reconfigurable platform. In 2014 International Conference on Smart Structures and Systems (ICSSS) (pp. 86-89). IEEE.
[46] Jadhav, H. M., Mulani, A., & Jadhav, M. M. (2022). Design and development of chatbot based on reinforcement learning. Machine Learning Algorithms for Signal and Image Processing, 219-229.

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[47] Mulani, A. O., & Mane, P. (2018). Secure and area efficient implementation of digital image watermarking on reconfigurable platform. International Journal of Innovative Technology and Exploring Engineering, 8(2), 56-61.
[48] Kalyankar, P. A., Mulani, A. O., Thigale, S. P., Chavhan, P. G., & Jadhav, M. M. (2022). Scalable face image retrieval using AESC technique. Journal Of Algebraic Statistics, 13(3), 173-176.
[49] Takale, S., & Mulani, A. (2022). DWT-PCA based video watermarking. Journal of Electronics, Computer Networking and Applied Mathematics (JECNAM) ISSN, 2799-1156.
[50] Kamble, A., & Mulani, A. O. (2022). Google assistant based device control. Int. J. of Aquatic Science, 13(1), 550-555.
[51] Kondekar, R. P., & Mulani, A. O. (2017). Raspberry Pi based voice operated Robot. International Journal of Recent Engineering Research and Development, 2(12), 69-76.
[52] Ghodake, R. G., & Mulani, A. O. (2018). Microcontroller based automatic drip irrigation system. In Techno-Societal 2016: Proceedings of the International Conference on Advanced Technologies for Societal Applications (pp. 109-115). Springer International Publishing.
[53] Mulani, A. O., Birajadar, G., Ivković, N., Salah, B., & Darlis, A. R. (2023). Deep learning based detection of dermatological diseases using convolutional neural networks and decision trees. Traitement du Signal, 40(6), 2819.
[54] Boxey, A., Jadhav, A., Gade, P., Ghanti, P., & Mulani, A. O. (2022). Face Recognition using Raspberry Pi. Journal of Image Processing and Intelligent Remote Sensing (JIPIRS) ISSN, 2815-0953.
[55] Patale, J. P., Jagadale, A. B., Mulani, A. O., & Pise, A. (2023). A Systematic survey on Estimation of Electrical Vehicle. Journal of Electronics, Computer Networking and Applied Mathematics (JECNAM) ISSN, 2799-1156.
[56] Gadade, B., & Mulani, A. (2022). Automatic System for Car Health Monitoring. International Journal of Innovations in Engineering Research and Technology, 57-62.
[57] Shinde, M. R. S., & Mulani, A. O. (2015). Analysisof Biomedical Image Using Wavelet Transform. International Journal of Innovations in Engineering Research and Technology, 2(7), 1-7.
[58] Mandwale, A., & Mulani, A. O. (2014, December). Implementation of convolutional encoder & different approaches for viterbi decoder. In IEEE International Conference on Communications, Signal Processing Computing and Information technologies.
[59] Mulani, A. O., Jadhav, M. M., & Seth, M. (2022). Painless machine learning approach to estimate blood glucose level with non-invasive devices. In Artificial intelligence, internet of things (IoT) and smart materials for energy applications (pp. 83-100). CRC Press.
[60] Maske, Y., Jagadale, A. B., Mulani, A. O., & Pise, A. C. (2023). Development of BIOBOT system to assist COVID patient and caretakers. European Journal of Molecular & Clinical Medicine, 10(01), 2023.
[61] Utpat, V. B., Karande, D. K., & Mulani, D. A. Grading of Pomegranate Using Quality Analysis ‖ . International Journal for Research in Applied Science & Engineering Technology (IJRASET), 10.
[62] Takale, S., & Mulani, D. A. (2022). Video Watermarking System. International Journal for Research in Applied Science & Engineering Technology (IJRASET), 10.
[63] Mandwale, A., & Mulani, A. O. (2015, January). Different approaches for implementation of Viterbi decoder. In IEEE international conference on pervasive computing (ICPC).
[64] Maske, Y., Jagadale, M. A., Mulani, A. O., & Pise, A. (2021). Implementation of BIOBOT System for COVID Patient and Caretakers Assistant Using IOT. International Journal of Information Technology and, 30-43.
[65] Mulani, A. O., & Mane, D. P. (2016). Fast and Efficient VLSI Implementation of DWT for Image Compression. International Journal for Research in Applied Science & Engineering Technology, 5, 1397-1402.
[66] Kambale, A. (2023). Home automation using google assistant. UGC care approved journal, 32(1), 1071-1077.
[67] Pathan, A. N., Shejal, S. A., Salgar, S. A., Harale, A. D., & Mulani, A. O. (2022). Hand gesture controlled robotic system. Int. J. of Aquatic Science, 13(1), 487-493.
[68] Korake, D. M., & Mulani, A. O. (2016). Design of Computer/Laptop Independent Data transfer system from one USB flash drive to another using ARM11 processor. International Journal of Science, Engineering and Technology Research.

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[69] Mandwale, A., & Mulani, A. O. (2016). Implementation of High Speed Viterbi Decoder using FPGA. International Journal of Engineering Research & Technology, IJERT.
[70] Kolekar, S. D., Walekar, V. B., Patil, P. S., Mulani, A. O., & Harale, A. D. (2022). Password Based Door Lock System. Int. J. of Aquatic Science, 13(1), 494-501.
[71] Shinde, R., & Mulani, A. O. (2015). Analysis of Biomedical Image ‖ . International Journal on Recent & Innovative trend in technology (IJRITT).
[72] Sawant, R. A., & Mulani, A. O. (2022). Automatic PCB Track Design Machine. International Journal of Innovative Science and Research Technology, 7(9).
[73] ABHANGRAO, M. R., JADHAV, M. S., GHODKE, M. P., & MULANI, A. (2017). Design And Implementation Of 8-bit Vedic Multiplier. International Journal of Research Publications in Engineering and Technology (ISSN No: 2454-7875).
[74] Gadade, B., Mulani, A. O., & Harale, A. D. (2024). Iot based smart school bus and student monitoring system. Naturalista Campano, 28(1), 730-737.
[75] Mulani, D. A. O. (2024). A Comprehensive Survey on Semi-Automatic Solar-Powered Pesticide Sprayers for Farming. Journal of Energy Engineering and Thermodynamics (JEET) ISSN, 2815-0945.
[76] Salunkhe, D. S. S., & Mulani, D. A. O. (2024). Solar Mount Design Using High-Density Polyethylene. NATURALISTA CAMPANO, 28(1).
[77] Seth, M. (2022). Painless Machine learning approach to estimate blood glucose level of Non-Invasive device. Artificial Intelligence, Internet of Things (IoT) and Smart Materials for Energy Applications.
[78] Kolhe, V. A., Pawar, S. Y., Gohery, S., Mulani, A. O., Sundari, M. S., Kiradoo, G., ... & Sunil, J. (2024). Computational and experimental analyses of pressure drop in curved tube structural sections of Coriolis mass flow metre for laminar flow region. Ships and Offshore Structures, 19(11), 1974-1983.
[79] Basawaraj Birajadar, G., Osman Mulani, A., Ibrahim Khalaf, O., Farhah, N., G Gawande, P., Kinage, K., & Abdullah Hamad, A. (2024). Epilepsy identification using hybrid CoPrO-DCNN classifier. International Journal of Computing and Digital Systems, 16(1), 783-796.
[80] Kedar, M. S., & Mulani, A. (2021). IoT Based Soil, Water and Air Quality Monitoring System for Pomegranate Farming. Journal of Electronics, Computer Networking and Applied Mathematics (JECNAM) ISSN, 2799-1156.
[81] Godse, A. P. A.O. Mulani (2009). Embedded Systems (First Edition).
[82] Pol, R. S., Bhalerao, M. V., & Mulani, A. O. A real time IoT based System Prediction and Monitoring of Landslides. International Journal of Food and Nutritional Sciences, Volume 11, Issue 7, 2022.
[83] Mulani, A. O., Sardey, M. P., Kinage, K., Salunkhe, S. S., Fegade, T., & Fegade, P. G. (2025). ML-powered Internet of Medical Things (MLIOMT) structure for heart disease prediction. Journal of Pharmacology and Pharmacotherapeutics, 16(1), 38-45.
[84] Aiwale, S., Kolte, M. T., Harpale, V., Bendre, V., Khurge, D., Bhandari, S., ... & Mulani, A. O. (2024). Non-invasive Anemia Detection and Prediagnosis. Journal of Pharmacology and Pharmacotherapeutics, 15(4), 408-416.
[85] Mulani, A. O., Bang, A. V., Birajadar, G. B., Deshmukh, A. B., Jadhav, H. M., & Liyakat, K. K. S. (2024). IoT Based Air, Water, and Soil Monitoring System for Pomegranate Farming. Annals of Agri-Bio Research, 29(2), 71-86.
[86] Kulkarni, T. M., & Mulani, A. O. (2024). Face Mask Detection on Real Time Images and Videos using Deep Learning. International Journal of Electrical Machine Analysis and Design (IJEMAD), 2(1).
[87] Thigale, S. P., Jadhav, H. M., Mulani, A. O., Birajadar, G. B., Nagrale, M., & Sardey, M. P. (2024). Internet of things and robotics in transforming healthcare services. Afr J Biol Sci (S Afr), 6(6), 1567-1575.
[88] Pol, D. R. S. (2021). Cloud Based Memory Efficient Biometric Attendance System Using Face Recognition. Stochastic Modeling & Applications, 25(2).
[89] Nagtilak, M. A. G., Ulegaddi, M. S. N., Adat, M. A. S., & Mulani, A. O. (2021). Breast Cancer Prediction using Machine Learning.
[90] Rahul, G. G., & Mulani, A. O. (2016). Microcontroller Based Drip Irrigation System.

[91] Kulkarni, T. M., & Mulani, A. O. Deep Learning Based Face-Mask Detection: An Approach to Reduce Pandemic Spreads in Human Healthcare. African Journal of Biological Sciences, 6(6), 2024.
[92] Mulani, A., & Mane, P. B. (2016). DWT based robust invisible watermarking. Scholars' Press.
[93] Dr. Vaishali Satish Jadhav, Dr. Shweta Sadanand Salunkhe, Dr. Geeta Salunkhe, Pranali Rajesh Yawle, Dr. Rahul S. Pol, Dr. Altaf Osman Mulani, Dr. Manish Rana, Iot Based Health Monitoring System for Human, Afr. J. Biomed. Res. Vol. 27 (September 2024).
[94] Dr. Vaishali Satish Jadhav, Geeta D. Salunke, Kalyani Ramesh Chaudhari, Dr. Altaf Osman Mulani, Dr. Sampada Padmakar Thigale, Dr. Rahul S. Pol, Dr. Manish Rana, Deep Learning-Based Face Mask Recognition in Real-Time Photos and Videos, Afr. J. Biomed. Res. Vol. 27 (September 2024).
[95] Altaf Osman Mulani, Electric Vehicle Parameters Estimation Using Web Portal, Recent Trends in Electronics & Communication Systems, Volume 10, Issue 3, 2023.
[96] Aryan Ganesh Nagtilak, Sneha Nitin Ulegaddi, Mahesh Mane, Altaf O. Mulani, Automatic Solar Powered Pesticide Sprayer for Farming, International Journal of Microwave Engineering and Technology, Volume 9 No. 2, 2023.
[97] Annasaheb S. Dandage, Vitthal R. Rupnar, Tejas A Pise, and A. O. Mulani, Real-Time Language Translation Application Using Tkinter. International Journal of Digital Communication and Analog Signals. 2025; 11(01): -p.
[98] AnnaSaheb S Dandage, Vitthal R. Rupnar, Tejas A Pise, and A. O. Mulani, IoT-Powered Weather Monitoring and Irrigation Automation: Transforming Modern Farming Practices. . 2025; 11(01): -p.
[99] Mulani, A.O., Kulkarni, T.M. (2025). Face Mask Detection System Using Deep Learning: A Comprehensive Survey. In: Singh, S., Arya, K.V., Rodriguez, C.R., Mulani, A.O. (eds) Emerging Trends in Artificial Intelligence, Data Science and Signal Processing. AIDSP 2023. Communications in Computer and Information Science, vol 2439. Springer, Cham. https://doi.org/10.1007/978-3-031-88759-8_3.
[100] Karve, S., Gangonda, S., Birajadar, G., Godase, V., Ghodake, R., Mulani, A.O. (2025). Optimized Neural Network for Prediction of Neurological Disorders. In: Singh, S., Arya, K.V., Rodriguez, C.R., Mulani, A.O. (eds) Emerging Trends in Artificial Intelligence, Data Science and Signal Processing. AIDSP 2023. Communications in Computer and Information Science, vol 2440. Springer, Cham. https://doi.org/10.1007/978-3-031-88762-8_18.
[101] Saurabh Singh, Karm Veer Arya, Ciro Rodriguez Rodriguez, and Altaf Osman Mulani, Emerging Trends in Artificial Intelligence, Data Science and Signal Processing, Communications in Computer and Information Science (CCIS), volume 2440.
[102] Saurabh Singh, Karm Veer Arya, Ciro Rodriguez Rodriguez, and Altaf Osman Mulani, Emerging Trends in Artificial Intelligence, Data Science and Signal Processing, Communications in Computer and Information Science (CCIS), volume 2439.
[103] Godase, V., Mulani, A., Pawar, A., & Sahani, K. (2025). A Comprehensive Review on PIR Sensor-Based Light Automation Systems. International Journal of Image Processing and Smart Sensors, 1(1), 22-29.
[104] Godase, V., Mulani, A., Takale, S., & Ghodake, R. (2025). Comprehensive Review on Automated Field Irrigation using Soil Image Analysis and IoT. Journal of Advance Electrical Engineering and Devices, 3(1), 46-55.
[105] Altaf Osman Mulani, Deshmukh M., Jadhav V., Chaudhari K., Mathew A.A., Shweta Salunkhe. Transforming Drug Therapy with Deep Learning: The Future of Personalized Medicine. Drug Research. 2025 Aug 29.
[106] Altaf O. Mulani, Vaibhav V. Godase, Swapnil R. Takale, Rahul G. Ghodake (2025), Image Authentication Using Cryptography and Watermarking, International Journal of Image Processing and Smart Sensors, Vol. 1, Issue 2, pp 27-34.
[107] Altaf O. Mulani, Vaibhav V. Godase, Swapnil R. Takale, Rahul G. Ghodake (2025), Advancements in Artificial Intelligence: Transforming Industries and Society, International Journal of Artificial Intelligence of Things (AIoT) in Communication Industry, Vol. 1, Issue 2, pp 1-5.
[108] Altaf O. Mulani, Vaibhav V. Godase, Swapnil R. Takale, Rahul G. Ghodake (2025), AI-Powered Predictive Analytics in Healthcare: Revolutionizing Disease Diagnosis and Treatment, Journal of Advance Electrical Engineering and Devices, Vol. 3, Issue 2, pp 27-34.
[109] Godase, V., Mulani, A., Takale, S., & Ghodake, R. (2025). A Holistic Review of Automatic Drip Irrigation Systems: Foundations and Emerging Trends. Available at SSRN 5247778.

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[110] V. Godase, R. Ghodake, S. Takale, and A. Mulani, ―Design and Optimization of Reconfigurable Microwave Filters Using AI Techniques, International Journal of RF and Microwave Communication Technologies, vol. 2, no. 2, pp.26–41, Aug. 2025.
[111] V. Godase, A. Mulani, R. Ghodake, S. Takale, "Automated Water Distribution Management and Leakage Mitigation Using PLC Systems," Journal of Control and Instrumentation Engineering, vol.11, no. 3, pp. 1-8, Aug. 2025.
[112] V. Godase, A. Mulani, R. Ghodake, S. Takale, "PLC-Assisted Smart Water Distribution with Rapid Leakage Detection and Isolation," Journal of Control Systems and Converters, vol. 1, no. 3, pp. 1-13, Aug. 2025.
[113] V. V. Godase, S. R. Takale, R. G. Ghodake, and A. Mulani, "Attention Mechanisms in Semantic Segmentation of Remote Sensing Images," Journal of Advancement in Electronics Signal Processing, vol. 2, no. 2, pp. 45–58, Aug. 2025.
[114] D. Waghmare, A. Mulani, S. R. Takale, V. Godase, and A. Mulani, "A Comprehensive Review on Automatic Fruit Sorting and Grading Techniques with Emphasis on Weight-based Classification," Research & Review: Electronics and Communication Engineering, vol. 2, no. 3, pp. 1-10, Oct. 2025.
[115] Karande, K. J., & Talbar, S. N. (2014). Independent component analysis of edge information for face recognition. Springer India.
[116] Karande, K. J., & Talbar, S. N. (2008). Face recognition under variation of pose and illumination using independent component analysis. ICGST-GVIP, ISSN.
[117] Kawathekar, P. P., & Karande, K. J. (2014, July). Severity analysis of Osteoarthritis of knee joint from X-ray images: A Literature review. In 2014 International Conference on Signal propagation and computer technology (ICSPCT 2014) (pp. 648-652). IEEE.
[118] Daithankar, M. V., Karande, K. J., & Harale, A. D. (2014, April). Analysis of skin color models for face detection. In 2014 International Conference on Communication and Signal Processing (pp. 533-537). IEEE.
[119] Karande, J. K., Talbar, N. S., & Inamdar, S. S. (2012, May). Face recognition using oriented Laplacian of Gaussian (OLOG) and independent component analysis (ICA). In 2012 Second International Conference on Digital Information and Communication Technology and it's Applications (DICTAP) (pp. 99-103). IEEE.
[120] Asabe, H., Asabe, R., Lengare, O., & Godase, S. (2025). IOT- BASED STORAGE SYSTEM FOR MANAGING VOLATILE MEDICAL RESOURCES IN HEALTHCARE FACILITIES. INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS), 05(03), 2427–2433. https://www.ijprems.com
[121] Karche, S. N., Mulani, A. O., Department of Electronics, SKN Sinhgad College of Engineering, Korti, & University of Solapur, Maharashtra, India. (2018). AESC Technique for Scalable Face Image Retrieval. International Journal of Innovative Research in Computer and Communication Engineering, 6(4), 3404–3405.
[122] https://doi.org/10.15680/IJIRCCE.2018.0604036
[123] Bankar, A. S., Harale, A. D., & Karande, K. J. (2021). Gestures Controlled Home Automation using Deep Learning: A Review. International Journal of Current Engineering and Technology, 11(06), 617–621. https://doi.org/10.14741/ijcet/v.11.6.4
[124] Mali, A. S., Ghadge, S. K., Adat, A. S., & Karande, S. V. (2024). Intelligent Medication Management System. IJSRD - International Journal for Scientific Research & Development, Vol. 12(Issue 3).
[125] Water Level Control, Monitoring and Altering System by using GSM in Irrigation Based on Season. (2019). In International Research Journal of Engineering and Technology (IRJET) (Vol. 06, Issue 04, p. 1035) [Journal-article]. https://www.irjet.net
[126] Modi, S., Misal, V., Kulkarni, S., & Mali A.S. (2025). Hydroponic Farming Monitoring System - Automated system to monitor and control nutrient and pH levels. In Journal of Microcontroller Engineering and Applications (Vol. 12, Issue 3, pp. 11–16). https://doi.org/10.37591/JoMEA
[127] Siddheshwar S. Gangonda, Prashant P. Patavardhan, Kailash J. Karande, "VGHN: variations aware geometric moments and histogram features normalization for robust uncontrolled face recognition", International Journal of Information Technology, https://doi.org/10.1007/s41870-021-00703-0.

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[128] Siddheshwar Gangonda and Prachi Mukherji, "Speech Processing for Marathi Numeral Recognition using MFCC & DTW Features", International Journal of Engineering Research And Applications (IJERA) pp. 118-122, ISSN: 2248-9622.
[129] Siddheshwar S. Gangonda, Prashant P. Patavardhan, Kailash J. Karande, "Recognition of Marathi Numerals Using MFCC and DTW Features", Book Title: Recent Trends on Image Processing and Pattern Recognition, RTIP2R 2018, CCIS 1037, pp. 1–11, © Springer Nature Singapore Pte Ltd. 2019 https://doi.org/10.1007/978-981-13-9187-3_17.
[130] Siddheshwar S. Gangonda, Prashant P. Patavardhan, Kailash J. Karande, "Analysis of Face Recognition Algorithms for Uncontrolled Environments", Book Title: Computing, Communication and Signal Processing, pp. 919–926, © Springer Nature Singapore Pte Ltd. 2018.
[131] Siddheshwar S. Gangonda, Prashant P. Patavardhan, Kailash J. Karande, "Recognition of Marathi Numerals using MFCC and DTW Features", 2nd International Conference on Recent Trends in Image Processing and Pattern Recognition (RTIP2R 2018), 21th -22th Dec., 2018, organized by Solapur University, Solapur in collaboration with University of South Dakota (USA) and Universidade de Evora (Portugal), India.
[132] Siddheshwar S. Gangonda, Prashant P. Patavardhan, Kailash J. Karande, "A Comprehensive Survey of Face Databases for Constrained and Unconstrained Environments", 2nd IEEE Global Conference on Wireless Computing & Networking (GCWCN-2018), 23th-24th Nov., 2018, organized by STES's Sinhgad Institute of Technology, Lonavala, India.
[133] Siddheshwar S. Gangonda, Prashant P. Patavardhan, Kailash J. Karande, "An Extensive Survey of Prominent Researches in Face Recognition under different Conditions", 4th International Conference on Computing, Communication, Control And Automation (ICCUBEA-2018), 16th to 18th Aug. 2018 organized by Pimpri Chinchwad College of Engineering (PCCOE), Pune, India.
[134] Siddheshwar S. Gangonda, Prashant P. Patavardhan, Kailash J. Karande, "Analysis of Face Recognition Algorithms for Uncontrolled Environments", 3rd International Conference on Computing, Communication and Signal Processing (ICCASP 2018), 26th-27th Jan.2018, organized by Dr. BATU, Lonere, India.
[135] Siddheshwar Gangonda and Prachi Mukherji, "Speech Processing for Marathi Numeral Recognition", International Conference on Recent Trends, Feb 2012, IOK COE, Pune.
[136] S. S. Gangonda, "Bidirectional Visitor Counter with automatic Door Lock System", National Conference on Computer, Communication and Information Technology (NCCCIT-2018), 30th and 31st March 2018 organized by Department of Electronics and Telecommunication Engineering, SKN SCOE, Korti, Pandharpur.
[137] Siddheshwar Gangonda and Prachi Mukherji, "Speech Processing for Marathi Numeral Recognition using MFCC & DTW Features", ePGCON 2012, 23rd and 24th April 2012 organized by Commins COE for Woman, Pune.
[138] Siddheshwar Gangonda and Prachi Mukherji, "Speech Processing for Marathi Numeral Recognition", National Conference on Emerging Trends in Engineering and Technology (VNCET'12), 30th March 2012 organized by Vidyavardhini's College of Engineering and Technology, Vasai Road, Thane.
[139] Siddheshwar Gangonda and Prachi Mukherji, "Speech Processing for Marathi Numeral Recognition", ePGCON 2011, 26th April 2011 organized by MAEER's MIT, Kothrud, Pune-38.
[140] Siddheshwar Gangonda, "Medical Image Processing", Aavishkar-2K7, 17th and 18th March 2007 organized by Department of Electronics and Telecommunication Engineering, SVERI's COE, Pandharpur.
[141] Siddheshwar Gangonda, "Image enhancement & Denoising", VISION 2k7, 28th Feb-2nd March 2007 organized by M.T.E. Society's Walchand College of Engineering, Sangli.
[142] Siddheshwar Gangonda, "Electromagnetic interference & compatibility" KSHITIJ 2k6, 23rd and 24th Sept. 2006 organized by Department of Mechanical Engineering, SVERI's COE, Pandharpur.
[143] A. Pise and K. Karande, "A genetic Algorithm-Driven Energy-Efficient routing strategy for optimizing performance in VANETs," Engineering Technology and Applied Science Research, vol. 15, no. 5, 2025, [Online]. Available: https://etasr.com/index.php/ETASR/article/view/12744
[144] A. C. Pise, K. J. Karande, "Investigating Energy-Efficient Optimal Routing Protocols for VANETs: A Comprehensive Study", ICT for Intelligent Systems, Lecture Notes in Networks and Systems 1109, Proceedings of ICTIS

2024 Volume 3, Lecture Notes in Networks and Systems, Springer, Singapore, ISSN 2367-3370, PP 407-417, 29 October 2024 https://doi.org/10.1007/978-981-97-6675-8_33.
[145] A. C. Pise, et. al., "Smart Vehicle: A Systematic Review", International Journal - The Ciência & Engenharia - Science & Engineering Journal ISSN: 0103-944XVolume 11 Issue 1, 2023pp: 992–998, 2023.
[146] A. C. Pise, et. al., "Smart Vehicle: A Systematic Review", International Journal of Research Publication and Reviews, ISSN 2582-7421, Vol 4, no 10, pp 2728-2731 October 2023.
[147] A. C. Pise, et. al., "Development of BIOBOT System to Assist COVID Patient and Caretakers", European Journal of Molecular and Clinical Medicine ; 10(1):3472-3480, 2023.
[148] A. C. Pise, et. al., "IoT Based Landmine Detection Robot", International Journal of Research in Science & EngineeringISSN: 2394-8299Vol: 03, No. 04, June-July 2023.
[149] A. C. Pise, et. al., "A Systematic survey on Estimation of Electrical Vehicle", Journal of Electronics, Computer Networking and Applied Mathematics (JECNAM) ISSN: 2799-1156, Volume 3, Issue 01, Pages 1-6, December 2023.
[150] A. C. Pise, et. al., "Python Algorithm to Estimate Range of Electrical Vehicle", Web of Science, Vol 21, No 1 (2022) December 2022
[151] A. C. Pise, et. al., "Implementation of BIOBOT System for COVID Patient and Caretakers Assistant using IOT", International Journal of Information technology and Computer Engineering. 30-43. 10.55529/ijitc.21.30.43, (2022).
[152] A. C. Pise, et. al., "An IoT Based Real Time Monitoring of Agricultural and Micro irrigation system", International journal of scientific research in Engineering and management (IJSREM), VOLUME: 06 ISSUE: 04 | APRIL – 2022, ISSN:2582-3930.
[153] A. C. Pise, Dr. K. J. Karande, "An Exploratory study of Cluster Based Routing Protocol in VANET: A Review", International Journal of Advanced Research in Engineering and Technology(IJARET), 12,10, 2021, 17-30, Manuscript ID :00000-94375 Source ID : 00000006, Journal_uploads/ IJARET/VOLUME_12_ISSUE_10/IJARET_12_10_002.pdf
[154] A. C. Pise, et. al., "Android based Portable Health Support System," A Peer Referred & Indexed International Journal of Research,Vol.8,issue.4 , April 2019.
[155] A. C. Pise, et. al., "Facial Expression Recognition Using Image Processing," International Journal of VLSI Design, Microelectronics and Embedded System,Vol.3,issue.2 , July 2018.
[156] A. C. Pise, et. al., "Detection of Cast Iron Composition by Cooling Curve Analysis using Thermocouple Temperature Sensor," UGC Approved International Journal of Academic Science (IJRECE),Vol.6, Issue.3 , July-September 2018.
[157] A. C. Pise, et. al., "Android Based Portable Health Support", System International Journal of Engineering Sciences & Research Technology (IJESRT 2017) Vol.6, Issue 8, pp 85-88 5th Aug 2017
[158] A. C. Pise, et. al., "Adaptive Noise Cancellation in Speech Signal", International Journal of Innovative Engg and Technology, 2017
[159] A. C. Pise, et. al., "Lung Cancer Detection System by using Baysian Classifier", ISSN 2454-7875, IJRPET, published online in conference special issue VESCOMM-2016, February 2016
[160] A. C. Pise, et. al.,"Review on Agricultural Plant Diseases Detection by Image Processing", ISSN 2278-62IX, IJLTET, Vol 7, Issue 1 May 2016
[161] A. C. Pise, et. al. "Segmentation of Retinal Images for Glaucoma Detection", International Journal of Engineering Research and Technology (06, June-2015).
[162] A. C. Pise, et. al. "Color Local Texture Features Based Face Recognition", International Journal of Innovations in Engineering and Technology(IJIET) , Dec. 2014
[163] A. C. Pise, et. al. "Single Chip Solution For Multimode Robotic Control", International Journal of Engineering Research and Technology (IJERT-2014), Vol. 3, Issue 12, Dec. 2014.
[164] Anjali C. Pise et. al., "Remote monitoring of Greenhouse parameters using zigbee Wireless Sensor Network", International Journal of Engineering Research & Technology ISSN 2278-0181 (online) Vol. 3, Issue 2, and pp: (2412-2414), Feb. 2014.
[165] A. C. Pise, K. J. Karande, "Cluster Head Selection Based on ACO In Vehicular Ad-hoc Networks", Machine Learning for Environmental Monitoring in Wireless Sensor Networks

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[166] A. C. Pise, K. J. Karande, "Architecture, Characteristics, Applications and Challenges in Vehicular Ad Hoc Networks" Presented in 27th IEEE International Symposium on Wireless Personal Multimedia Communications (WPMC 2024) "Secure 6G – AI Nexus: Where Technology Meets Humanity" Accepted for book chapter to be published in international Scopus index book by River publisher.
[167] A. C. Pise, Dr. K. J. Karande, "K-mean Energy Efficient Optimal Cluster Based Routing Protocol in Vehicular Ad Hoc Networks", International Conference on Innovations in Artificial Intelligence and Machine Learning (ICAIML-2022), August 20th and 21st 2022 Springer database Conference.
[168] A. C. Pise, Mr. D. Nale, "Web-Based Application for Result Analysis", ", International Conference on Innovations in Artificial Intelligence and Machine Learning (ICAIML-2022), August 20th and 21st 2022 Springer database Conference.
[169] A. C. Pise, et. al., "Detection of Cast Iron Composition by Cooling Curve Analysis using Thermocouple Temperature Sensor," 2nd International Conference on Engineering Technology, Science and Management Innovation (ICETSMI – 2018), 2nd September 2018.
[170] A. C. Pise, et. al., "Facial Expression Recognition Using Facial Features," IEEE International Conference on Communication and Electronics Systems (ICCES 2018), October 2018.
[171] A. C. Pise, et. al., "Estimating Parameters of Cast Iron Composition using Cooling Curve Analysis," IEEE International Conference on Communication and Electronics Systems (ICCES 2018), Coimbatore, October 2018.
[172] A. C. Pise, et. al., "Android based portable Health Support System," International Conference on Innovations in Engineering and Technology (CIET 2016), SKN Sinhgad College of Engineering, 30-31 Dec 2016.
[173] A. C. Pise, et. al., "Baysian Classifier & FCM Segmentation for Lung Cancer Detection in early stage," International Conference on Innovations in Engineering and Technology (CIET 2016), SKN Sinhgad College of Engineering, 30-31 Dec 2016.
[174] A. C. Pise, et. al., "Cast Iron Composition Measurement by Coding Curve Analysis," International Conference on Innovations in Engineering and Technology (CIET 2016), SKN Sinhgad College of Engineering, 30-31 Dec 2016.
[175] A. C. Pise, et. al., "War field Intelligence Defence Flaging Vehicle," International Conference on Innovations in Engineering and Technology (CIET 2016), SKN Sinhgad College of Engineering, 30-31 Dec 2016.
[176] A. C. Pise, et. al. "Disease Detection of Pomegranate Plant", IEEE sponsored International Conference on Computation of Power, Energy, Information and Communication, 22- 23 Apr. 2015.
[177] A. C. Pise, P. Bankar. "Face Recognition by using GABOR and LBP", IEEE International Conference on Communication and Signal Processing, ICCSP, 2-4 Apr. 2015
[178] A. C. Pise, et. al. "Single Chip Solution For Multimode Robotic Control", Ist IEEE International Conferene on Computing Communication and Automation, 26-27 Feb2015.
[179] Anjali C. Pise, Vaishali S. Katti, "Efficient Design for Monitoring of Greenhouse Parameters using Zigbee Wireless Sensor Network", fifth SARC international conference IRF,IEEE forum ISBN 978-93-84209-21-6,pp 24-26, 25th May 2014
[180] A. C. Pise, P. Bankar, "Face Recognition using Color Local Texture Features", International Conference on Electronics and Telecommunication, Electrical and Computer Engineering, Apr.2014.
[181] A. C. Pise, et.al. "Monitoring parameters of Greenhouse using Zigbee Wireless Sensor Network", 1st International Conference on Electronics and Telecommunication, Electrical and Computer Engineering, 5-6 Apr.2014.
[182] A. C. Pise, et. al. "Compensation schemes and performance Analysis of IQ Imbalances in Direct Conversion Receivers", International Conference at GHPCOE, Gujarat, (Online Proceeding is Available), 2009.
[183] A. C. Pise, K. J. Karande, "Energy-Efficient Optimal Routing Protocols in VANETs", 66th Annual IETE Convention, AIC -2023 September16-17, 2023, under the Theme: The Role of 5G In Enabling Digital Transformation for Rural Upliftment.
[184] A. C. Pise, et. al. "Automatic Bottle Filling Machine using Raspberry Pi", National Conference on computer ;Communication & information Technology (NCCIT-2018) dated 30th & 31st March 2018.
[185] A. C. Pise, et. al. "Design & Implementation of ALU using VHDL", National Conference on computer ;Communication & information Technology (NCCIT-2018) dated 30th & 31st March 2018.

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International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[186] A. C. Pise, et. al. "Mechanism and Control of Autonomus four rotor Quad copter", National Conference on Computer, Electrical and Electronics Engineering, 23- 24 Apr. 2016.
[187] A. C. Pise, et. al. "Segmentation of Optic Disk and Optic Cup from retinal Images", ICEECMPE – Chennai, June 2015
[188] A. C. Pise, et. al. "Diseases Detection of Pomegranate Plant", IEEE Sponsored International conference on Computation of Power, Energy , April 2015.
[189] A. C. Pise, et. al. "Compensation Techniques for I/Q Imbalance in Direct-Conversion Receivers", Conference at SCOE, Pune 2010.
[190] A. C. Pise, et. al. "I/Q Imbalance compensation Techniques in Direct Conversion Receiver ", Advancing Trends in Engineering and Management Technologies, ATEMT-2009, Conference at Shri Ramdeobaba Kamla Nehru Engineering College, Nagpur, 20-21 November 2009
[191] A. C. Pise, et. al. "Compensation Techniques for I/Q Imbalance in Direct Conversion Receiver", Conference at PICT, Pune 2008.
[192] A. C. Pise, et. al. "I/Q Imbalance compensation Techniques in Direct Conversion Receiver ", Conference at DYCOE, Pune 2008.
[193] A. C. Pise, et. al. "DUCHA: A New Dual channel MAC protocol for Multihop Ad-Hoc Networks", Conference at SVCP, Pune 2007.
[194] Godase, V., Pawar, P., Nagane, S., & Kumbhar, S. (2024). Automatic railway horn system using node MCU. Journal of Control & Instrumentation, 15(1).
[195] Godase, V., & Godase, J. (2024). Diet prediction and feature importance of gut microbiome using machine learning. Evolution in Electrical and Electronic Engineering, 5(2), 214-219.
[196] Jamadade, V. K., Ghodke, M. G., Katakdhond, S. S., & Godase, V. A Comprehensive Review on Scalable Arduino Radar Platform for Real-time Object Detection and Mapping.
[197] Godase, V. (2025). A comprehensive study of revolutionizing EV charging with solar-powered wireless solutions. Advance Research in Power Electronics and Devices e-ISSN, 3048-7145.
[198] Godase, V. (2025, April). Advanced Neural Network Models for Optimal Energy Management in Microgrids with Integrated Electric Vehicles. In Proceedings of the International Conference on Trends in Material Science and Inventive Materials (ICTMIM-2025) DVD Part Number: CFP250J1-DVD.
[199] Dange, R., Attar, E., Ghodake, P., & Godase, V. (2023). Smart agriculture automation using ESP8266 NodeMCU. J. Electron. Comput. Netw. Appl. Math, (35), 1-9.
[200] Godase, V. (2025). Optimized Algorithm for Face Recognition using Deepface and Multi-task Cascaded Convolutional Network (MTCNN). Optimum Science Journal.
[201] Mane, V. G. A. L. K., & Gangonda, K. D. S. Pipeline Survey Robot.
[202] Godase, V. (2025). Navigating the digital battlefield: An in-depth analysis of cyber-attacks and cybercrime. International Journal of Data Science, Bioinformatics and Cyber Security, 1(1), 16-27.
[203] Godase, V., & Jagadale, A. (2019). Three element control using PLC, PID & SCADA interface. International Journal for Scientific Research & Development, 7(2), 1105-1109.
[204] Godase, V. (2025). Edge AI for Smart Surveillance: Real-time Human Activity Recognition on Low-power Devices. International Journal of AI and Machine Learning Innovations in Electronics and Communication Technology, 1(1), 29-46.
[205] Godase, V., Modi, S., Misal, V., & Kulkarni, S. (2025). LoRaEdge-ESP32 synergy: Revolutionizing farm weather data collection with low-power, long-range IoT. Advance Research in Analog and Digital Communications, 2(2), 1-11.
[206] Godase, V. (2025). Comparative study of ladder logic and structured text programming for PLC. Available at SSRN 5383802.
[207] Godase, V., Modi, S., Misal, V., & Kulkarni, S. Real-time object detection for autonomous drone navigation using YOLOv8, ‖ . Advance Research in Communication Engineering and its Innovations, 2(2), 17-27.

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[208] Godase, V. (2025). Smart energy management in manufacturing plants using PLC and SCADA. Advance Research in Power Electronics and Devices, 2(2), 14-24.
[209] Godase, V. (2025). IoT-MCU Integrated Framework for Field Pond Surveillance and Water Resource Optimization. International Journal of Emerging IoT Technologies in Smart Electronics and Communication, 1(1), 9-19.
[210] Godase, V. (2025). Graphene-Based Nano-Antennas for Terahertz Communication. International Journal of Digital Electronics and Microprocessor Technology, 1(2), 1-14.
[211] Godase, V., Khiste, R., & Palimkar, V. (2025). AI-Optimized Reconfigurable Antennas for 6G Communication Systems. Journal of RF and Microwave Communication Technologies, 2(3), 1-12.
[212] Bhaganagare, S., Chavan, S., Gavali, S., & Godase, V. V. (2025). Voice-Controlled Home Automation with ESP32: A Systematic Review of IoT-Based Solutions. Journal of Microprocessor and Microcontroller Research, 2(3), 1-13.
[213] Jamadade, V. K., Ghodke, M. G., Katakdhond, S. S., & Godase, V. A Comprehensive Review on Scalable Arduino Radar Platform for Real-time Object Detection and Mapping.
[214] Godase, V. (2025). Cross-Domain Comparative Analysis of Microwave Imaging Systems for Medical Diagnostics and Industrial Testing. Journal of Microwave Engineering & Technologies, 12(2), 39-48p.
[215] V. K. Jamadade, M. G. Ghodke, S. S. Katakdhond, and V. Godase, ―A Review on Real-time Substation Feeder Power Line Monitoring and Auditing Systems," International Journal of Emerging IoT Technologies in Smart Electronics and Communication, vol. 1, no. 2, pp. 1-16, Sep. 2025.
[216] V. V. Godase, "VLSI-Integrated Energy Harvesting Architectures for Battery-Free IoT Edge Systems,"Journal of Electronics Design and Technology, vol. 2, no. 3, pp. 1-12, Sep. 2025.
[217] A. Salunkhe et al., "A Review on Real-Time RFID-Based Smart Attendance Systems for Efficient Record Management," Advance Research in Analog and Digital Communications, vol. 2, no. 2, pp.32-46, Aug. 2025.
[218] Vaibhav, V. G. (2025). A Neuromorphic-Inspired, Low-Power VLSI Architecture for Edge AI in IoT Sensor Nodes. Journal of Microelectronics and Solid State Devices, 12(2), 41-47p.
[219] Nagane, M.S., Pawar, M.P., & Godase, P.V. (2022). Cinematica Sentiment Analysis. Journal of Image Processing and Intelligent Remote Sensing.
[220] Godase, V.V. (2025). Tools of Research. SSRN Electronic Journal.
[221] Godase, V. (n.d.). EDUCATION AS EMPOWERMENT: THE KEY TO WOMEN'S SOCIO ECONOMIC DEVELOPMENT. Women Empowerment and Development, 174–179.
[222] Godase, V. (n.d.). COMPREHENSIVE REVIEW ON EXPLAINABLE AI TO ADDRESSES THE BLACK BOX CHALLENGE AND ITS ROLE IN TRUSTWORTHY SYSTEMS. In Sinhgad College of Engineering, Artificial Intelligence Education and Innovation (pp. 127–132).
[223] Godase, V. (n.d.-b). REVOLUTIONIZING HEALTHCARE DELIVERY WITH AI-POWERED DIAGNOSTICS: A COMPREHENSIVE REVIEW. In SKN Sinhgad College of Engineering, SKN Sinhgad College of Engineering (pp. 58–61).
[224] Dhope, V. (2024). SMART PLANT MONITORING SYSTEM. In International Journal of Creative Research Thoughts (IJCRT). https://www.ijcrt.org
[225] M. M. Zade,Sushant D.Kambale,Shweta A.Mane,Prathamesh M. Jadhav.(2025) "IOT Based early fire detection in Jungles". RIGJA&AR Volume 2 Issue 1,ISSN:2998-4459. DOI:https://doi.org/10.5281/zendo.15056435
[226] M. M. Zade, Bramhadev B. Rupanar, Vrushal S. Shilawant , Akansha R. Pawar(2025) "IOT Flood Monitoring & Alerting System using Rasberry Pi-Pico "International Journal of Research Publication & Reviews , Volume 6 ,Issue 3,ISSN:2582-7421.DOI:https://ijrpr.com/uploads/V6ISSUE3/IJRPR40251.pdf
[227] M.M.Zade(2022) "Touchless Fingerprint Recognition System"(Paper-ID 907)(2022) International Conference on "Advanced Technologies for Societal Applications: Techno-Societal 2022 https://link.springer.com/book/10.1007/978-3-031-34644-6?page=6
[228] Mr.M.M.Zade published the paper on "Automation of Color Object Sorting Conveyor Belt", in International Journal of Scientific Research in Engineering & Management (IJSREM),ISSN:2582-3930 Volume 06 ,Issue 11th November 2022.

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ISSN: 2581-9429 Volume 5, Issue 4, October 2025 Impact Factor: 7.67

[229] Mr.M.M.Zade published the paper on "Cloud Based Patient Health Record Tracking web Developement",in International Journal of Advanced Research in Science, Communication & Technology(IJARSCT),ISSN NO:2581-9429 Volume 02 ,Issue 03,DOI 1048175/IJARSCT-3705,IF 6.252, May 2022.
[230] Mr. Mahesh M Zade, "Performance analysis of PSNR Vs. Impulse Noise for the enhancement of Image using SMF", Journal of Applied Science & Computations (JASC UGC Approved), Volume VI, Issue II, Feb.2019
[231] Mr. Mahesh M Zade, "Classification of Power Quality Disturbances Using SVM & their Efficiency Comparison", Journal of Applied Science & Computations (JASC UGC Approved), Volume VI, Issue II, Feb.2019
[232] Mr. Mahesh M Zade, "Dynamic Clustering of Wireless Sensor Network Using Modified AODV", Journal of Applied Science & Computations (JASC UGC Approved), Volume VI, Issue II, Feb.2019
[233] Mr. Mahesh M Zade, "Performance analysis of PSNR Vs. Impulse Noise for the enhancement of Image using SMF", National Conference on Mathematical Modeling and Computational Intelligence 2K19 (MMCI-2k19), in association with JASC, at S. B. Patil College of Engineering, Indapur, Feb.2019
[234] Mr. Mahesh M Zade, "Classification of Power Quality Disturbances Using SVM & their Efficiency Comparison", National Conference on Mathematical Modeling and Computational Intelligence 2K19 (MMCI-2k19), in association with JASC, at S. B. Patil College of Engineering, Indapur Feb.2019
[235] Mr. Mahesh M Zade, "Dynamic Clustering of Wireless Sensor Network Using Modified AODV", National Conference on Mathematical Modeling and Computational Intelligence 2K19 (MMCI-2k19), in association with JASC, at S. B. Patil College of Engineering, Indapur Feb.2019
[236] Mr. Mahesh M Zade & Mr.S.M.Karve,"Performance Analysis of Median Filter for Enhancement of Highly Corrupted Images", National Conference on Advanced Trends in Engineering, Association with IRJMS, Karmyogi Engineering College, Shelave, Pandharpur, March 2016.
[237] Mr. Mahesh M Zade & Mr.S.M.Karve,"Implementation of Reed Solomen Encoder & Decoder Using FPGA",National Conference on Advanced Trends in Engineering, Association with IRJMS, Karmyogi Engineering College, Shelave, Pandharpur, March 2016.
[238] Mr. Mahesh M Zade & Dr.S.M.Mukane,"Performance of Switching Median Filter for Enhancement of Image", National Conference on Mechatronics at Sinhgad Institute of Technology and Science, Narhe, Pune, Feb. 2016.
[239] Mr. Mahesh M Zade & Dr.S.M.Mukane,"Enhancement of Image with the help of Switching Median Filter", National Conference on Emerging Trends in Electronics & Telecommunication Engineering, SVERI's College of Engineering Pandharpur, NCET 2013.
[240] Mr.Mahesh M Zade & Dr.S.M.Mukane,"Enhancement of Image with the help of Switching Median Filter", International Journal of Computer Application (IJCA) SVERI's College of Engineering, Pandharpur, Dec.2013.