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Design of An Automated Car Washing System with Verilog HDL

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Abstract: *Automation remains at the forefront of technological innovation, enabling the efficient control of processes without direct human involvement This project presents an advanced automated car washing system utilizing Field Programmable Gate Arrays (FPGAs) programmed in Verilog HDL.The system provides washing services that are rapid, convenient, and effective. A flow chart for controlling an automated car washing system with four working modes and implemented with a custom mode option is given. The resulting compact design minimizes power consumption and effectively addresses other major issues. These comprehensive optimizations meet stringent performance, area, and power requirements, elevating the operational efficiency of automated car washing systems. Furthermore, the design is synthesized and implemented using Xilinx's ISE Design Suite.*

Keywords: ISE Design Suite

I. INTRODUCTION

Car washing is a critical aspect of vehicle maintenance, preventing rust, oxidation, and fine scratches, which can degrade the vehicle's appearance and longevity. Traditional car washing methods, while effective often involve high water consumption, substantial manual labor, and inconsistent cleaning quality. As the need for more efficient and sustainable solutions grows, modern car wash systems have evolved into automated, contact-based, and touch-free options, offering a variety of programs such as prewashing, waxing, drying, and polishing. Despite these advancements, existing systems still face challenges, including high operational costs, inefficiency in integrating new technologies, and increased system complexity.

Automation has emerged as a solution to these challenges, providing efficient, eco-friendly, and high-quality car washing. Technologies like Field- Programmable Gate Arrays (FPGAs) offer an ideal platform for implementing such systems. FPGAsallow for flexible, reconfigurable designs that can be updated with minimal effort, leading to reduced resource consumption and improved performance. These systems can offer different modes for car washing, such as prewashing, water washing, waxing, drying, and inspection, ensuring a more personalized and thorough cleaning process. However, traditional systems often lack the flexibility to easily incorporate new features or technologies.

The motivation for this project arises from the growing demand for more sustainable, efficient, and customizable car washing solutions. Traditional methods consume too much water, are labour- intensive, and often fail to meet modern environmental standards. To address these issues, this project proposes an FPGA-based automated car washing system designed using Verilog HDL. The main objectives are to develop a system that optimizes power, area, and timing for greater efficiency, and to validate the system's functionality through simulations and implementation on Spartan-6 FPGA hardware. The goal is to deliver a scalable, eco- friendly, and efficient solution that improves both performance and customer satisfaction while minimizing resource consumption.

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II. METHODOLOGY

Overview of the Car Wash Control Flow

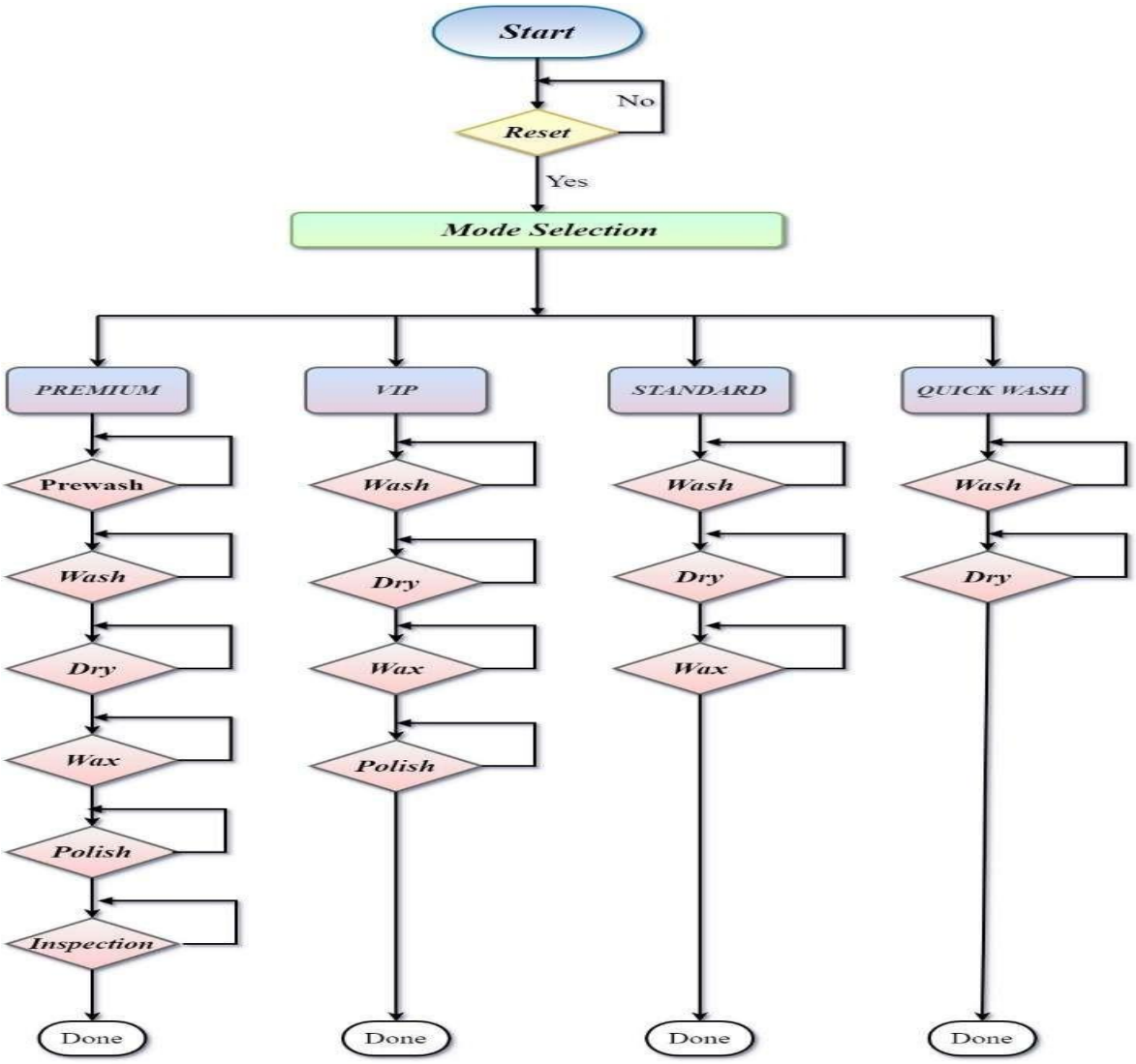

Fig.1. A control flowchart of the car washing system

The car washing system supports four modes:

1. VIP
2. Extra Foam
3. Standard
4. Low Cost

Mode Switching:

The system requires stopping the current mode before activating a new one. This ensures the process is sequential and avoids conflicts

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Key Operational States for All Modes:

1. Foaming:

o Foam is sprayed over the car to ensure complete coverage.

o Foam is applied using nozzles around the vehicle.

2. Washing:

o Foam is stopped, and clean water is supplied to rinse the vehicle thoroughly.

3. Waxing:

o A layer of wax is applied to protect the car's surface.

4. Drying:

o Blow valves activate for a short duration to dry the vehicle.

5. Finishing:

o Concludes the process and resets the system, preparing it for the next operation.

Control Mechanism:

• The Ready Block:

o Monitors various system parameters, such as:

 User input for mode selection.

 Presence of foam, wax, or alarms.

o It ensures the system's readiness before starting or switching processes.

• Sequential Operation:

o Each mode progresses through the same steps(Foam→ Water → Wax → Dry → Finish) but may differ in intensity or application level based on the mode chosen (e.g., more foam for "Extra Foam" mode).

III. IMPLEMENT DESIGN

The Car Washing System module uses a finite state machine (FSM) to control the various phases of the car wash process based on the selected mode. The FSM transitions between states (IDLE, PRE_WASH, WASH, DRY, WAX, POLISH, INSPECTION, COMPLETE) and controls output signals (prewash, washing, drying, waxing, polishing, inspection, done) according to mode- specific time durations.

Inputs:

• clk: Clock signal to synchronize state transitions.

• reset: Resets the FSM.

• mode_select: 3-bit input to select the car wash mode (VIP, Standard, Quick, Premium).

Outputs:

• Signals for each phase (pre_wash, washing, drying, waxing, polishing, inspection, done).

Internal Registers:

• Parameters define the duration for each phase, encoded in clock cycles (e.g., t1, t2, t3, etc.).

Time Duration Parameters:

Each phase is assigned a specific time duration in clock cycles:

• t1:200cycles

• t2:300cycles

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• t3:400cycles
• t4:500cycles
• t5:600cycles
• t6:200cycles
• t7:100cycles

Mode-specific Time Durations:
• VIP Mode(3'b001):
o No pre-wash, wash for t1 (200 cycles), dry for t2 (300 cycles), wax for t3 (400 cycles), polish for t4 (500 cycles), no inspection.
The time durations for each phase are set based on the selected mode, ensuring that each phase lasts the designated number of clock cycles.

IV. SIMULATION RESULT

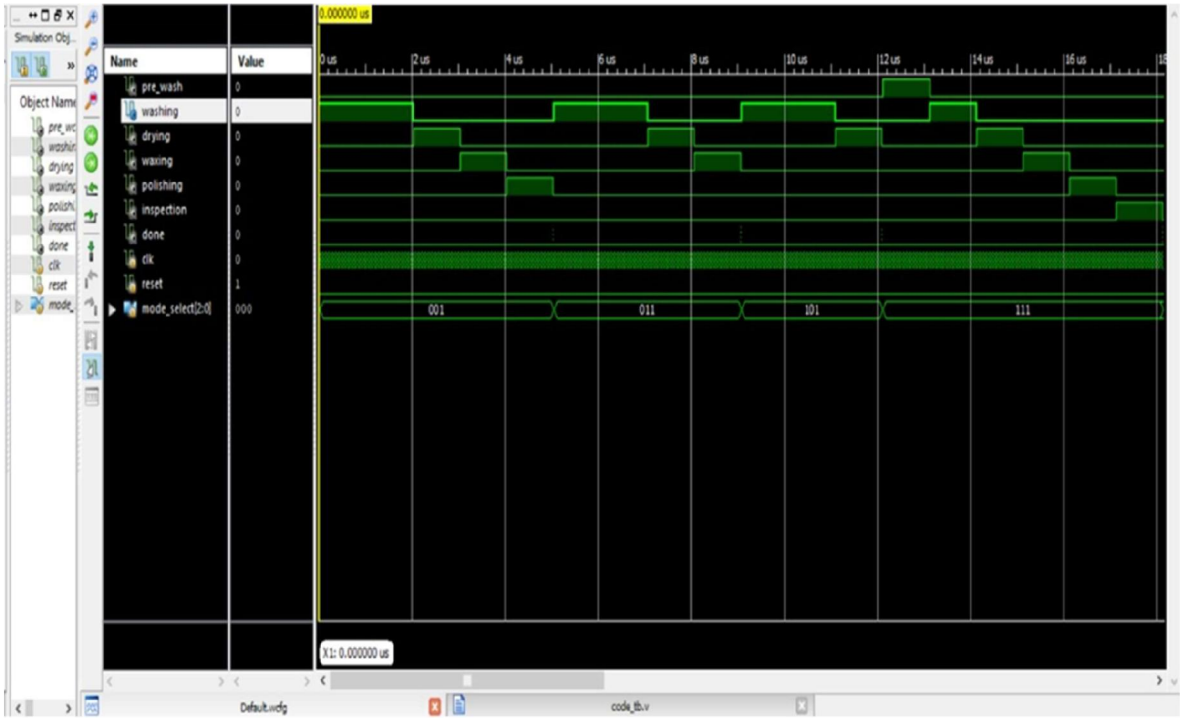

Fig.2.SIMULATIONWAVEFORM

The fig 2 shows the behaviour of a multi-stage process over time, with specific control signals for each stage (prewash, washing, drying, waxing, polishing, inspection, done). The clock (clk) signal provides the timing reference, while the reset signal initializes the system. Initially, the reset signal is high, keeping all stages inactive. When the mode_select[2:0] bus changes from 000 to 111, activating the pre_wash ,washing ,waxing, polishing, and inspection stages sequentially. The done signal indicate the end of the entire process .This process will repeat to all the other modes which will activate there respective states.

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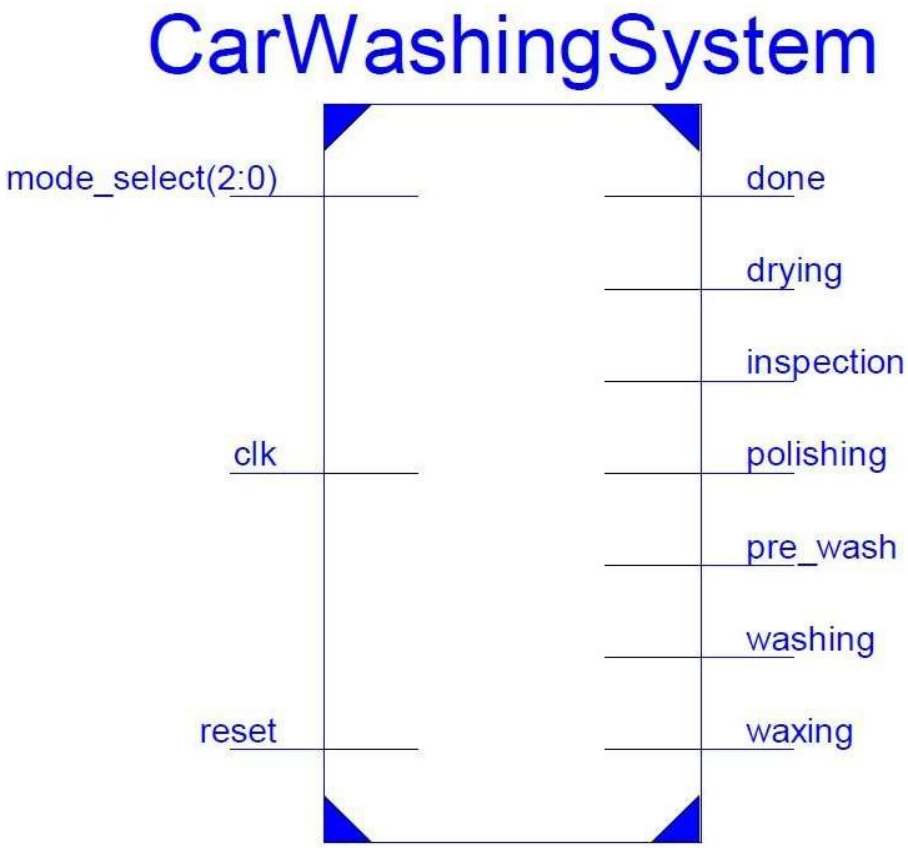

Fig. 3. Model of the car washing system

Fig. 3 shows the top module of the design for the automated car washing system. The top module is a crucial component that acts as the gateway for inputs and outputs, as well as managing the internal operations of the processor. A processor is a device that executes a series of instructions to carry out specific tasks.

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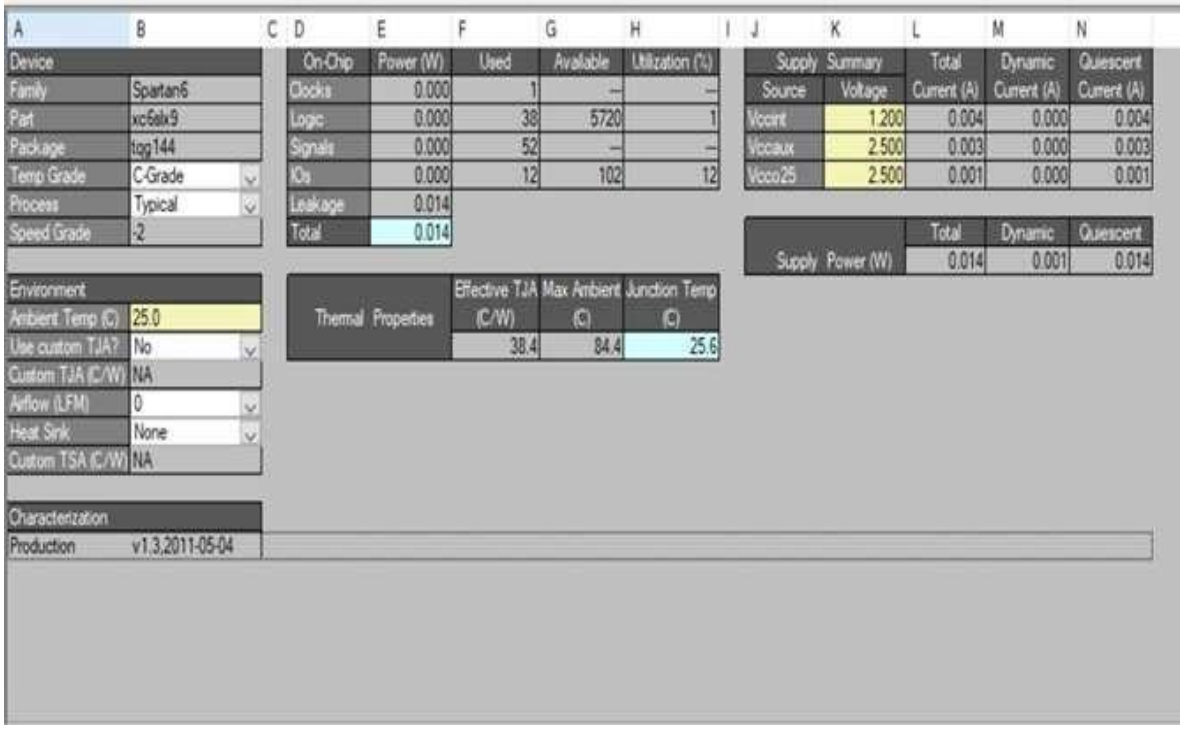

Device	
Family	Spartan6
Part	xc6slx9
Package	tqg144
Temp Grade	C-Grade
Process	Typical
Speed Grade	-2

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	–	–
Logic	0.000	38	5720	1
Signals	0.000	52	–	–
IOs	0.000	12	102	12
Leakage	0.014			
Total	0.014			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.004	0.000	0.004
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.001	0.000	0.001

Supply Power (W)	Total	Dynamic	Quiescent
	0.014	0.001	0.014

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Heat Sink	None
Custom TSA (C/W)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	38.4	84.4	25.6

Characterization	
Production	v1.3,2011-05-04

Figure 4. Power Report

Figure 4 gives an estimation of the power, which is 0.014 W.

```
All values displayed in nanoseconds (ns)

--------------------------------------------------------------------------------
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.016ns (frequency: 199.362MHz)
  Total number of paths / destination ports: 238 / 19
--------------------------------------------------------------------------------
Delay:               5.016ns (Levels of Logic = 4)
  Source:            timer_6 (FF)
  Destination:       state_FSM_FFd1 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: timer_6 to state_FSM_FFd1
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             2    0.525    0.954  timer_6 (timer_6)
     LUT4:I1->O           4    0.235    0.912  state_FSM_FFd6-In1_SW0 (N01)
     LUT6:I4->O           6    0.250    0.876  state_FSM_FFd6-In21 (state_FSM_FFd6-In2)
     LUT6:I5->O           1    0.254    0.682  state_FSM_FFd1-In1 (state_FSM_FFd1-In1)
     LUT6:I5->O           1    0.254    0.000  state_FSM_FFd1-In3 (state_FSM_FFd1-In)
     FDC:D                     0.074           state_FSM_FFd1
    ----------------------------------------
    Total                      5.016ns (1.592ns logic, 3.424ns route)
                                       (31.7% logic, 68.3% route)

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Figure 5. Delay Analysis of the Design

Figure 5 gives an estimation of delay analysis, which is 5.01 ns for the design of the automatic car washing system.

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Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	19	11,440	1%	
Number used as Flip Flops	19			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	38	5,720	1%	
Number used as logic	37	5,720	1%	
Number using O6 output only	17			
Number using O5 output only	10			
Number using O5 and O6	10			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	12	1,430	1%	
Number of MUXCYs used	12	2,860	1%	
Number of LUT Flip Flop pairs used	38			
Number with an unused Flip Flop	25	38	65%	
Number with an unused LUT	0	38	0%	
Number of fully used LUT-FF pairs	13	38	34%	
Number of unique control sets	1			
Number of slice register sites lost to control set restrictions	1	11,440	1%	
Number of bonded IOBs	12	102	11%	

Figure 6. Area Consumption from Design Summary

Figure 6 gives an estimation of the area used by the design of the automated car washing system.

	Existing Project		Proposed Project	
	Used	Available	Used	Available
LUTs as Logic	34	53200	38	5720
LUTs as memory	0	17400	0	1440
Slice Registers	23	106400	19	11440
Registers as flipflops	23	106400	19	11440
Slice LUTs	34	53200	38	5720

Figure 7. The area comparison between the existing and proposed project

IV. CONCLUSION

In the future, the automated car washing systems will be increasingly used as they combine a number of advantages such as saving time and money, easily operated system, profitability, rapid washing process, high-quality cleaning of hard-to-reach places such as grille, wheels and others and others. The complex programmable logic devices and field programmable gate array are widely used in the modern world. They are a modern and promising way in the design of various electromechanical objects and systems. Based on the developed flow chart of the proposed car washing system, the control program has been designed in ISE Design Suite software though the language Verilog HDL. The

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implemented control allows a choice of four regimes depending on the money placed and the method of washing. The obtained simulation tests for the individual operating modes of the carwashing system prove the operability of the design model

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