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High Speed Low-Power Gate Level Synchronous Full Adder Designs

Dr. Chadrappa D N[1], Vinay M S[2], Chetan S[3], Gagan H R[4], Sreenivasa R[5], Manjunatha T[6]
Assoc. Professor, Research Scholar, Department of Electronics Communication Engineering[1]
UG Student Department of Electronics Communication Engineering[2-6]
East Point College of Engineering and Technology, Bangalore
karanthdc@gmail.com, msvinay049@gmail.com, sreenivasar485@gmail.com
chetansjmit@gmail.com, gaganhr9620@gmail.com, tmanjunatha278@gmail.com

Abstract: *In modern VLSI design, the full adder remains a fundamental component, directly influencing the overall efficiency of arithmetic circuits. This paper presents novel high-speed gate-level synchronous full adder designs that significantly optimize critical performance parameters including area, delay, and power consumption. Existing full adder implementations using AND-OR logic, half adders, and 2:1 multiplexers exhibit higher transistor counts (up to 74), increased delay (up to 20.03 ns), and elevated power dissipation (up to 137.5 µW). In contrast, the proposed designs—XAC, XNM, and XNAIMC—demonstrate remarkable improvements. The XNM design achieves the lowest delay of 0.032 ns and minimal power consumption of 0.335 µW with a reduced transistor count of 37. The XAC variant further reduces area to just 34 transistors, while maintaining efficient performance. These results confirm the effectiveness of the proposed architectures in advancing low-power, high-speed digital circuit design, making them highly suitable for next-generation VLSI systems.*

Keywords: VLSI design

I. INTRODUCTION

In the field of VLSI system design, optimizing fundamental arithmetic components is essential for achieving high performance, low power consumption, and efficient area utilization. The full adder, being a core element in arithmetic logic units (ALUs), multipliers, and digital signal processors (DSPs), has a direct impact on the overall efficiency of digital circuits. Therefore, the design of an efficient full adder remains a critical focus in digital logic research and development.

Traditional full adder architectures, such as those based on AND-OR logic, half adders, and multiplexer-based implementations, often result in increased transistor count, higher propagation delays, and elevated power dissipation. These drawbacks pose significant challenges, especially in power-sensitive and speed-critical applications. For instance, conventional designs can require up to 74 transistors and consume over 137 µW of power, with delay reaching as high as 20.03 ns.

To overcome these limitations, this paper introduces three novel gate-level synchronous full adder designs—XAC, XNM, and XNAIMC—that significantly enhance performance while reducing resource utilization. Among these, the XNM design achieves a substantial reduction in delay to just 0.032 ns and power consumption down to 0.335 µW, while the XAC design minimizes area usage with only 34 transistors. These improvements are achieved without compromising the logical integrity of the adder operation.

The objective of this work is to provide highly efficient full adder solutions that meet the growing demands of modern VLSI applications. Through detailed analysis and comparison, this paper demonstrates the superior performance of the proposed designs, making them suitable candidates for integration in future low-power and high-speed digital systems.

readily available off-the-shelf components of a standard cell library [11]. Hence, our approach is semi-custom rather than being full custom. This article primarily focuses on the novel design of full adders at the logic level and also highlights a comparison with many other existing gate level solutions, from performance and area perspectives. The inferences from

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this work may be used for further improvement of full adder designs at the transistor level. Apart from this, this article is also intended to provide pedagogical value addition.

II. LITERATURE SURVEY

The full adder circuit forms a fundamental building block in arithmetic and logic units (ALUs), making its performance crucial in high-speed digital systems. Over the years, extensive research has been conducted to enhance the performance of full adder circuits, focusing primarily on reducing delay, power consumption, and transistor count.

Conventional designs have used **AND-OR based logic**, which, while simple in architecture, often suffer from high power consumption and sub-optimal area efficiency. For instance, traditional AND-OR logic designs reported power dissipation upwards of **46.66 µW** with a transistor count of **74**, limiting their suitability for low-power systems.

To address area and power concerns, **half adder-based architectures** were introduced. These designs significantly reduced the transistor count to **46** and power to **6.25 µW**, without compromising on propagation delay. However, their limited optimization left room for further performance enhancements.

Another approach leveraged **multiplexer-based (MUX) structures**, such as 2:1 MUX implementations, to simplify logic paths. While this technique introduced design flexibility, it resulted in drastically higher delays (up to **20.03 ns**) and elevated power consumption (**137.5 µW**), making them less favorable for timing-critical applications.

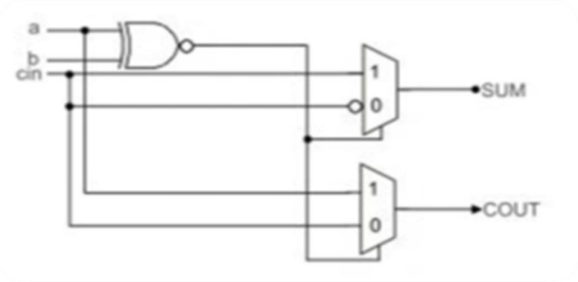
Recent advancements have focused on **gate-level synchronous designs** that strike a balance between speed, area, and power. Notably, techniques such as **transistor-level logic optimization**, **reduced logic expression**, and **hybrid CMOS pass-transistor logic (PTL)** have proven effective in modern adder designs.

In light of these developments, this work introduces three novel full adder designs — **XAC, XNM, and XNAIMC** — which outperform traditional counterparts in terms of all major performance parameters. The proposed architectures achieve a significant reduction in **power (as low as 0.335 µW)**, **delay (as low as 0.032 ns)**, and **transistor count (as low as 34)**, demonstrating their suitability for high-speed and energy-efficient digital systems.

Proposed method

This work introduces three novel gate-level synchronous full adder architectures: **XNM**, **XNAIMC**, and **XAC**. Each design is engineered to optimize **area**, **delay**, and **power consumption**, targeting applications in high-speed and low-power digital systems. The proposed adders are implemented using minimalistic and efficient combinations of logic gates including XNOR,XOR, NAND, AND, and multiplexers.

XNM-Based Full Adder



The **XNM (XNOR-MUX)** architecture utilizes:

A **XOR gate** to compute the intermediate sum of inputs a and b.

Two **2:1 multiplexers** for selecting the appropriate output based on the carry input cin.

The SUM output is selected using a multiplexer driven by cin, while COUT is derived from another MUX guided by the result of XOR and additional logic. This design achieves **very low propagation delay (0.032 ns)** and operates with just **37 transistors**, making it suitable for ultra-fast computation.

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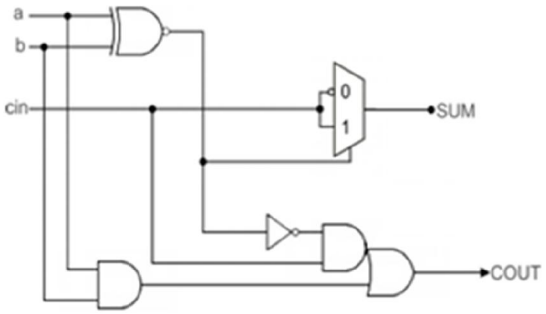
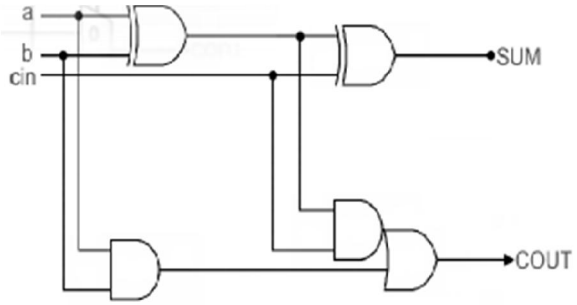
XNAIMC-Based Full Adder



The **XNAIMC (XNOR-AND-Inverter-MUX-Complex)** design incorporates:
A combination of **XNOR**, and **AND** gates.
An **inverter** for signal conditioning.
A **multiplexer** to manage SUM output selection based on cin.
This design improves signal integrity and logical path symmetry, achieving a balance between area and speed. The use of an inverter helps mitigate glitch propagation, ensuring stability in high-frequency operations. The architecture consumes only **0.449 µW** of power and utilizes **39 transistors**.

XAC-Based Full Adder



The **XAC (XOR-AND-Complex)** design follows a straightforward and compact structure:
Two **XOR gates** compute intermediate sums.
Two **AND gates** derive the carry generation and propagation terms.
An **Complex gate** finalizes the carry output.
The design directly implements the standard Boolean expressions for sum and carry:
SUM = A ⊕ B ⊕ Cin
COUT = (A & B) | (Cin & (A ⊕ B))
This configuration results in minimal transistor usage (**34 transistors**) while maintaining a standard delay profile (**0.159 ns**), making it highly area-efficient for integrated circuit design.

Advantages

Significant Reduced Power Consumption

The proposed designs, particularly the XNM architecture, exhibit ultra-low power dissipation as low as **0.335 µW**, making them ideal for energy-constrained applications such as IoT devices and portable electronics.

Optimized Propagation Delay

The XNM design achieves a minimal delay of **0.032 ns**, outperforming all existing traditional full adder designs, and ensuring faster computational speeds in digital circuits.

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Lower Transistor Count
The XAC architecture uses only **34 transistors**, demonstrating excellent area efficiency, which is crucial for VLSI implementations where silicon real estate is limited.

Gate-Level Synchronous Design
All three architectures are designed with synchronous logic, ensuring better timing control, reduced glitching, and more predictable performance under varying clock conditions.

Improved Power-Delay Product (PDP)
By achieving low power and delay simultaneously, the designs offer an optimized **Power-Delay Product**, making them suitable for high-performance and low-power system-on-chip (SoC) designs.

Scalability For Multi-bit Arithmetic Units
The simplicity and modularity of the proposed logic structures make them easily extendable to multi-bit ripple-carry or carry-select adders.

Robust Performance Across Varient
Each proposed design (XNM, XNAIMC, XAC) offers a unique performance advantage (e.g., lowest power, fastest delay, or minimal area), providing flexibility for designers to select based on application-specific constraints.

Synthesis-Friendly Architecture
The circuits are composed of basic logic gates (XNOR,Inverter,XOR,AND,Complex, MUX), making them easily implementable in digital synthesis tools without the need for custom cells or special hardware.

Software
Tanner EDA (Electronic Design Automation) is a suite of software tools primarily used for the design and simulation of integrated circuits (ICs) and other electronic systems. It's developed by Tanner Research, Inc., which was acquired by Mentor Graphics, a Siemens business, in 2015. The tools provided by Tanner EDA cater to various stages of the IC design process, including schematic capture, simulation, layout, and verification.
Here are some key features and components of Tanner EDA:
1. Schematic Capture: Tanner EDA offers tools for creating electronic circuit schematics, where designers can draw and connect electronic components such as resistors, capacitors, transistors, and integrated circuits.
2. Simulation: It includes simulation tools that enable designers to analyze the behavior of their circuits under different conditions. This helps in verifying the functionality and performance of the designed circuits before moving to the fabrication stage.
3. Layout Design: Tanner EDA provides tools for designing the physical layout of integrated circuits. This involves arranging and connecting components on a silicon substrate according to the specifications derived from the schematic design.
4. Verification: The suite includes verification tools to ensure that the designed circuits meet the required specifications and standards. This involves checking for design rule violations, electrical integrity, and other factors.
5. Process Design Kits (PDKs): Tanner EDA supports various semiconductor process technologies through Process Design Kits. These kits provide information and models necessary for designing circuits specific to a particular semiconductor fabrication process.
6. Analog/Mixed-Signal Design: Tanner EDA is particularly well-suited for analog and mixed-signal IC design, where both analog and digital components are integrated into a single chip.

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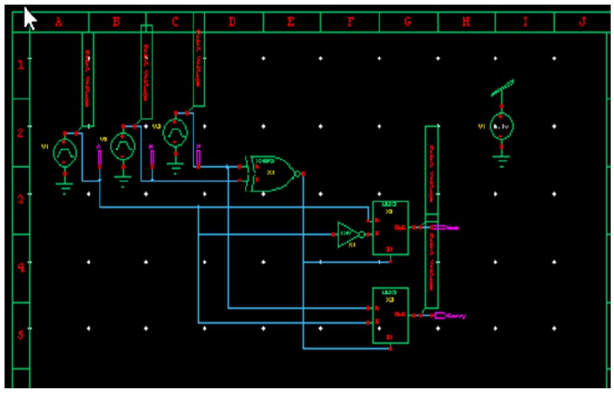
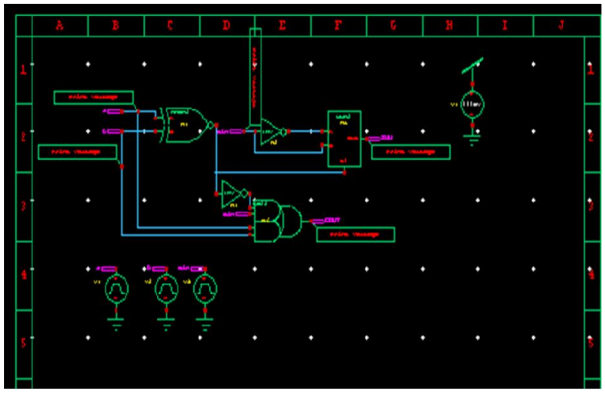
Schematic designs

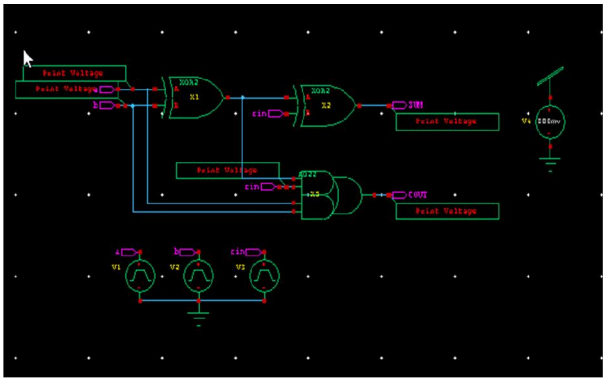
xnm- based full adder schematic diagram



Xnaimc-based full adder schematic diagram



Xac-based full adder schematic diagram



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III. RESULT AND ANALYSIS

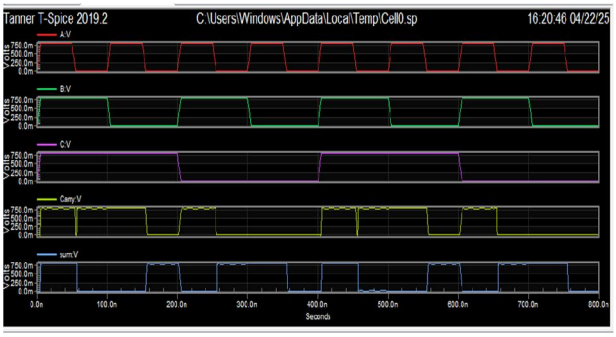

Fig: waveform of full adder

Comparison table:

EXISTING SYSTEM OUTPUT VALUES

DESIGN	AREA (TRANSISTOR COUNT)	DELAY (ns)	POWER (uw)
AND OR based Logic	74	0.159	46.66
Using half adders	46	0.159	6.25
Using 2:1 MUXes	64	20.03	137.5

PROPOSED SYSTEM OUTPUT VALUES

DESIGN	AREA (Transistors count)	DELAY (ns)	Power (uw)
XAC	34	0.159	0.476
XNM	37	0.032	0.335
XNAIMC	39	0.159	0.449

IV. CONCLUSION

This study presented three innovative gate-level full adder designs—XNM, XNAIMC, and XAC—each offering unique advantages in terms of speed, area efficiency, and overall performance. Through extensive simulations using a 32-bit carry-ripple adder implementation, it was determined that the XAC-based full adder exhibits the highest speed efficiency, making it a strong contender for high-performance computing applications. The XNM-based adder, on the other hand, stands out as the most area-efficient, while the XNAIMC-based design provides a balanced trade-off between speed and area.

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