IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 5, Issue 7, June 2025
Impact Factor: 7.67

Study of Drain Characteristics of N-Channel MOSFET with Varying Impurity Concentration - A Comparative Study

Arnab Debnath[1], Arpan Yadav[2], Palasri Dhar[3], Koushik Pal[4], Anurima Majumdar[5]
Department of Electronics and Communications Engineering
Guru Nanak Institute of Technology, Sodepur, India[1-5]
Corresponding author: palasri.dhar@gnit.ac.in

Abstract: *In this work, n-channel MOSFETs of varying Boron doping profiles, using Silvaco TCAD tools namely Athena and Atlas, have been analysed. The fabrication of nMOS has been done through a series of fabrication steps, which include wafer selection with appropriate orientation and phosphorus doping, oxide diffusion, boron-implantation for p-well formation, polysilicon deposition, phosphorus-implantation for heavily doped n+- regions, aluminium-deposition for source/drain contact and extraction of unused materials. All of these steps have been performed through the Athena tool. Afterward, Atlas performs several simulations to deduce the transfer characteristics curves (the I_D-V_{GS} curves). Performance parameters of MOSFETs of varying doping profiles, such as Threshold Voltage (V_{TH}), Trance-conductance, and channel length modulation have been compared. These simulation-based analyses provide a better understanding of an nMOS device's fabrication process and a clearer physical insight into its characteristic curves and performance parameters.*

Keywords: Doping, Threshold Voltage, trance-conductance, channel length modulation

I. INTRODUCTION

As metal-oxide-semiconductor field-effect transistors (MOSFETs) continue to scale into the nanometer regime, precise control over device electrostatics becomes increasingly critical. Among the many design parameters influencing MOSFET behaviour, the substrate doping concentration plays a pivotal role in defining threshold voltage, junction capacitances, and short-channel effects. This makes it a crucial lever in device optimization, especially for analog and low-power digital applications where performance is highly sensitive to such variations.

The I_D-V_{GS} characteristic of an NMOSFET describes the relationship between the gate-to-source voltage and the resulting drain current, serving as a fundamental measure of gate control over channel formation. This curve encapsulates key physical processes within the device and provides a basis for extracting essential performance parameters.

Threshold voltage (V_{TH}) denotes the minimum gate voltage required to induce strong inversion and enable significant conduction.

Transconductance (g_m), defined as the derivative of drain current with respect to gate voltage, quantifies the device's gain and sensitivity to gate control.

Channel length modulation (λ) captures the variation of drain current with drain voltage in the saturation region, reflecting the impact of effective channel shortening.

All these parameters are directly influenced by the substrate doping profile, which alters the electrostatic landscape within the device and thereby modulates its overall electrical behaviour.

The simulation workflow is implemented using Silvaco TCAD, comprising several integrated tools.

Deck Build serves as the primary interface for writing and managing simulation scripts, offering a command-line-driven environment for running both process and device simulations.

DOI: 10.48175/IJARSCT-28079

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 7, June 2025 Impact Factor: 7.67

Athena is utilized for process simulation, enabling the modelling of fabrication steps such as ion implantation, diffusion, and oxidation to generate physically accurate device structures. These structures are then passed to Atlas, the device simulator, which numerically solves the fundamental semiconductor equations to obtain electrical characteristics under various biasing conditions.

Finally, Tony Plot provides a graphical interface for post-processing and visualizing simulation results, including doping profiles and I_D–V_{GS} curves. This modular toolchain allows for precise evaluation of how substrate doping influences nMOSFETsbehaviour.

This study presents a detailed investigation of nMOSFETsI_D-V_{GS}characteristics under systematically varied substrate doping concentrations. The aim is to extract and analyse the resulting shifts in V_{TH}, changes in g_m, and modulation of drain current due to λ. By correlating doping-induced electrostatic shifts with these key parameters, the work contributes to a deeper understanding of how substrate engineering can be used to tune device performance for advanced CMOS technologies.

II. METHODOLOGY

This study investigates the impact of substrate doping concentration on the electrical characteristics of NMOSFETs by analysing the I_D-V_{GS} behaviour. Key performance parameters—threshold voltage (V_{TH}), transconductance (g_m), and channel length modulation (λ)—are extracted using analytical techniques from simulated transfer characteristics. The following texts outlines the methodology of obtaining device structure, simulation setup, and parameter extraction.

2.1 Device Structure and Doping Profile

An NMOSFET structure is considered for this study to isolate substrate doping effects from short-channel phenomena such as velocity saturation and DIBL. The device parameters are as follows:

Channel length (L): 0.7 µm
Channel width (W): 1 µm
Gate oxide thickness (t_{ox}): 0.00999929 µm = 10 nm
Gate material: n^+ polysilicon (work function = 4.17 eV)
Source/drain implant parameters:
Implant species: Arsenic (n-type)
Dose: 5 x 10^{15} cm^{-2}
Substrate doping (p-type): Varied across 1×10^{12}, 8×10^{12}, and 15×10^{12} cm^{-3}
Drain-Source Voltage (V_{DS}) = 0.1V
Body terminal is tied to ground (V_{BS} = 0 V).
All simulations are performed at room temperature (T = 300 K).

2.2 Parameter extraction and techniques

1. Threshold Voltage (V_{TH})

The threshold voltage is the gate voltage at which a strong inversion layer forms at the semiconductor-oxide interface. It is defined as:

$V_{TH}=V_{FB}+2\phi_F+\sqrt{(2\epsilon_S qN_A 2\phi_F)}/C_{ox}$

Where:

$V_{FB}=\phi_{MS}-Q_{ox}/C_{ox}$: Flat-band voltage
$\phi F=kT/q\ln(N_A/ni)$: Fermi potential
ϵ_S: Permittivity of the semiconductor
q: Elementary charge
N_A: Substrate doping concentration (p-type)
$C_{OX}=\epsilon_{ox}/t_{ox}$: Oxide capacitance per unit area

As substrate doping N_A increases, ϕ_F increases, resulting in a higher V_{TH}.

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429 Volume 5, Issue 7, June 2025 Impact Factor: 7.67

2. Drain Current (I_D) Equations and Regions of Operation

The drain current depends on V_{GS}, V_{DS}, and device geometry. Ignoring short-channel effects and assuming constant mobility, the drain current equations are:

Cutoff Region: $V_{GS} < V_{TH}$

$I_D = 0$

Linear (Triode) Region: $V_{GS}>V_{TH}$, $V_{DS}<V_{GS}-V_{TH}$

$I_D=\mu nCox(W/L)[(V_{GS}-V_{TH})V_{DS}-V_{DS}^2/2]$

Saturation Region: $V_{GS}>V_{TH}$, $V_{DS}\geq V_{GS}-V_{TH}$

$I_D=0.5\mu nCox(W/L)(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$

Where:

μ_n: Electron mobility

W, L: Width and length of the channel

λ: Channel length modulation parameter

3. Transconductance (g_m)

Transconductance quantifies how effectively the gate voltage controls the drain current. It is defined as the partial derivative of $I_D$with respect to V_{GS}, holding V_{DS} constant:

In the Saturation Region:

$g_m=\partial I_D/\partial V_{GS}=\mu_n C_{ox}(W/L)(V_{GS}-V_{TH})$

As substrate doping increases:

Mobility μ_n tends to **decrease** due to impurity scattering.

V_{TH} increases, reducing $V_{GS}-V_{TH}$

Hence, **g_m typically degrades** with increasing substrate doping.

4. Channel Length Modulation (λ)

Channel length modulation describes the increase in drain current in saturation due to effective shortening of the channel as drain voltage increases. It is modeled by the term $(1+\lambda V_{DS})$ in the saturation equation. To extract λ, one typically analyzes the slope of the I_D-V_{GS}curve in the saturation region:

$\lambda=1/I_D(\partial I_D/\partial V_{DS})_{sat}$

Physically, λ increases with:

Shorter channel lengths

Higher substrate doping, due to steeper electric fields and reduced depletion width control

While λ is often small for long-channel devices, it becomes a significant factor in modern, scaled transistors and is sensitive to substrate doping due to its influence on the depletion region depth near the drain.

III. RESULTS AND ANALYSIS

The following results were obtained from TCAD simulations for each device structure:

Transfer characteristics: I_D-V_{GS} at V_{DS} = 0.1 V

Extracted parameters:

Threshold Voltage (V_{TH})

Transconductance (g_m)

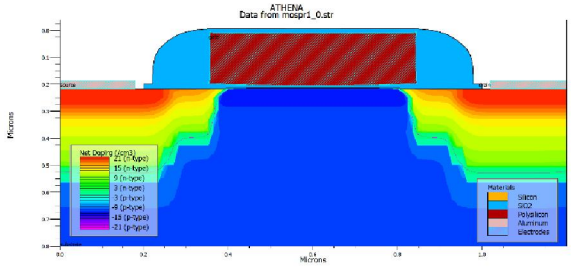
Channel Length Modulation parameter (λ)

These metrics are used to assess how substrate doping concentration alters the nMOSFET's switching behavior and analog performance.

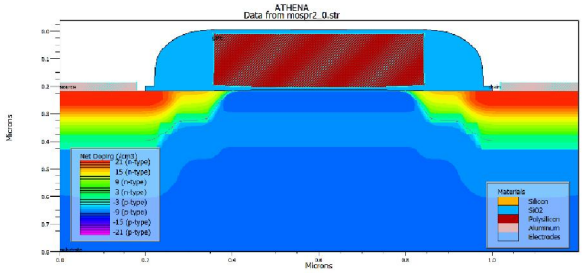
3.1 Device Structures and Doping Profiles

Three NMOSFET devices were designed, differing only in their substrate doping concentrations:

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 5, Issue 7, June 2025
Impact Factor: 7.67



Structure obtained at doping concentration $1\times10^{12}cm^{-3}$



Structure obtained at doping concentration $8\times10^{12}cm^{-3}$

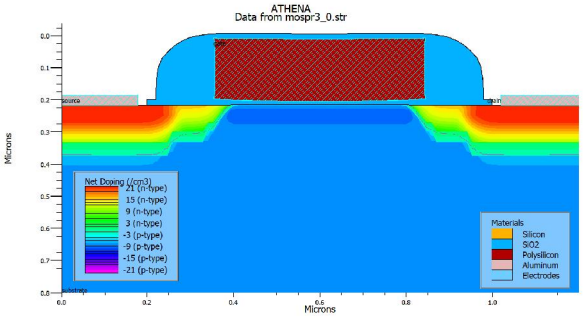


Fig 1: Structure obtained at doping concentration $15\times10^{12}cm^{-3}$

	Substrate Doping (N_A)	Description
1	$1\times10^{12}cm^{-3}$	Lightly doped; deeper depletion region, thinner bulk body
2	$8\times10^{12}cm^{-3}$	Moderately doped; balanced profile
3	$15\times10^{12}cm^{-3}$	Heavily doped; shallower depletion region, narrower body

As doping increases, the substrate becomes more conductive, reducing depletion width and increasing bulk potential.

3.2 Transfer Characteristics

The I_D-V_{GS} curves for all three structures are plotted on a single graph for direct visual comparison.

DOI: 10.48175/IJARSCT-28079

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 5, Issue 7, June 2025
Impact Factor: 7.67

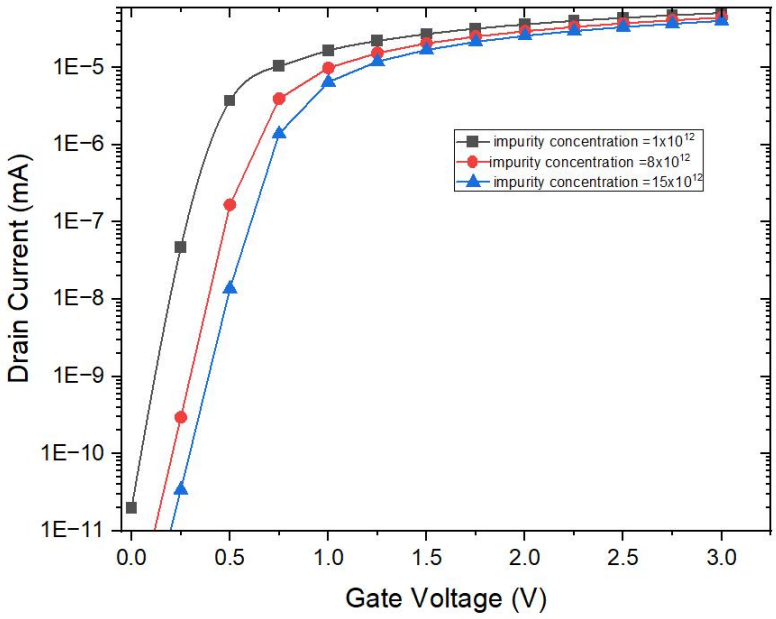


Fig 2 :Obtained I_D-V_{GS} curves of differently doped MOSFETs

Observations:

The **turn-on point shifts to the right** as doping increases — a clear indication of increasing threshold voltage (V_{TH}).

Drain current magnitude at a fixed V_{GS} reduces with doping — implying degradation in carrier mobility and reduced effective gate overdrive.

The **slope of the curve (g_m)** becomes progressively shallower in higher-doped substrates.

3.3 Comparison of Extracted Parameters

The parameters were quantitatively extracted from the transfer and output characteristics. Below is a comparative table:

Parameter	1	2	3
V_{TH} (V)	0.310478	0.534386	0.650756
g_m (μS)	0.000268858	0.00023928	0.000218765
λ (V^{-1})	0.152795	0.131034	0.115279

Interpretation:

Threshold Voltage increases due to higher surface potential and depletion charge required to invert the channel.

Transconductance decreases due to both reduced gate overdrive and degraded carrier mobility at higher doping levels.

Channel Length Modulation intensifies slightly with doping, indicating increased susceptibility to output conductance due to stronger electric fields near the drain.

IV. CONCLUSION

This study presented a detailed analysis of the impact of substrate doping concentration on the electrical characteristics of NMOSFETs through the investigation of their I_D–V_{GS} behaviour. Three device structures were simulated, differing only in their substrate doping levels: 1×10^{12}, 8×10^{12}, and 15×10^{12} cm^{-3}. The results clearly demonstrate that variations in doping significantly influence critical performance parameters, including threshold voltage (V_{TH}), transconductance (g_m), and channel length modulation (λ).

DOI: 10.48175/IJARSCT-28079

IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 5, Issue 7, June 2025
Impact Factor: 7.67

An increase in substrate doping concentration was observed to cause a systematic rise in the threshold voltage. This behaviour aligns with theoretical expectations based on MOS electrostatics, wherein a higher acceptor concentration increases the depletion charge and surface potential, thereby requiring a larger gate voltage to achieve strong inversion. Consequently, the V_{TH} for the highest doped structure was substantially higher than that of the lightly doped counterpart. While beneficial for reducing off-state leakage in digital applications, this increase in V_{TH} also reduces the effective gate overdrive, which directly impacts transconductance.

Transconductance was found to degrade with higher doping concentrations. This reduction in g_m is attributed to decreased carrier mobility—resulting from enhanced impurity scattering—as well as a reduction in gate overdrive due to the elevated V_{TH}. Since transconductance is directly related to the amplification and switching speed of the device, this trend indicates that heavily doped substrates may not be optimal for high-performance or analog applications.

Similarly, channel length modulation, represented by the parameter λ, increased moderately with substrate doping. The enhanced electric fields in the high-doping regimes compress the depletion region near the drain, leading to a stronger modulation of the effective channel length and, hence, increased output conductance. This behaviour further contributes to a decline in intrinsic gain, which is a key concern in analog circuit design.

Overall, the results emphasize the complex trade-offs introduced by substrate doping. While high doping provides tighter V_{TH} control and suppresses leakage—crucial for low-power digital circuits—it simultaneously degrades transconductance and increases channel length modulation, both of which are detrimental for analog and high-speed logic performance. Thus, the choice of doping concentration must be guided by application-specific priorities, balancing between power efficiency and performance requirements.

Looking ahead, this work can be extended in multiple directions. Future studies may include an analysis of short-channel effects such as drain-induced barrier lowering (DIBL), punch-through, and velocity saturation under varying doping conditions. Additionally, evaluating the impact of substrate doping on process variation sensitivity and long-term reliability phenomena like negative bias temperature instability (NBTI) and hot carrier injection (HCI) would be valuable. For analog and RF applications, further exploration of derived metrics such as intrinsic gain, unity-gain bandwidth, and noise figure could yield deeper insights. Moreover, incorporating advanced materials like high-κ gate dielectrics and metal gate stacks would allow assessment of how these modern enhancements interact with substrate doping profiles. Finally, investigating temperature-dependent behaviour would help evaluate device robustness across thermal extremes.

In conclusion, this work provides a foundational understanding of how substrate doping influences MOSFET electrical behaviour, offering practical insights for device engineers, circuit designers, and process technologists working at advanced technology nodes.

REFERENCES

[1]. ATLAS and ATHENA User's Manuals, 2018. Comprehensive guides for device and process simulation used throughout this study. Available at: https://www.silvaco.com

[2]. Y. Taur & T. H. Ning, Fundamentals of Modern VLSI Devices, 2nd Ed. An authoritative reference for modern MOSFET theory and design.

[3]. Das, A. & Kumar, M. J. "Workfunction Engineering for Threshold Voltage Control in Nanoscale CMOS." IEEE Transactions on Electron Devices, vol. 62, no. 7, 2015.

[4]. S. M. Sze & K. K. Ng, Physics of Semiconductor Devices, 3rd Ed. This work provided theoretical grounding for concepts like channel modulation and transconductance.

[5]. "TCAD Simulation of NMOSFETs with Various Gate Materials." A collection of comparative case studies and parameter variation results. Accessible at: https://www.researchgate.net

[6]. 6.720J Integrated Microelectronic Devices. Lecture notes and problem sets used to validate theoretical assumptions. Available at: https://ocw.mit.edu