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Detecting Power and Synchrinization Failure

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Abstract: *The project is designed to develop a system to detect the synchronization failure of any external supply source to the power grid on sensing the abnormalities in frequency and voltage. Further the project can be enhanced by using power electronic devices to isolte the grid from the erring supply source by sensing cycle by cyck deviation for more sophisticated means of detection.*

Keywords: Islanding, Grid, Voltage Variation, Frequency Variation, Active methods, Passive methods

I. INTRODUCTION

This project presents the development of a microcontroller based islanding detection for grid connected inverter with under/over voltage and under/over frequency islanding detection. The system is based on a microcontroller from Atmel 8051 family. The microcontroller monitors the under/over voltage derived from a set of comparators and under/over frequency from by the interrupt program for the utility grid and the processed value of voltage and frequency for timing ON/OFF the relay between a grid connected inverter and the utility grid. The project would alternatively use a variable frequency generator representing the inverter using 555-timer for changing the frequency while a standard variae shall be used to vary the input voltage for achieving the test conditions by a lamp load being driven from the microcontroller output as stated above. The microcontroller used in the project is of 8051 family which is of 8 bit. The power supply consists of a step down transformer 230/12V, which steps down the voltage to 12V AC. This is converted to DC using a Bridge rectifier. The ripples are removed using a capacitive filter and it is then regulated to +5V using a voltage righter 7805 which is required for the operation of the microcontroller and other components.

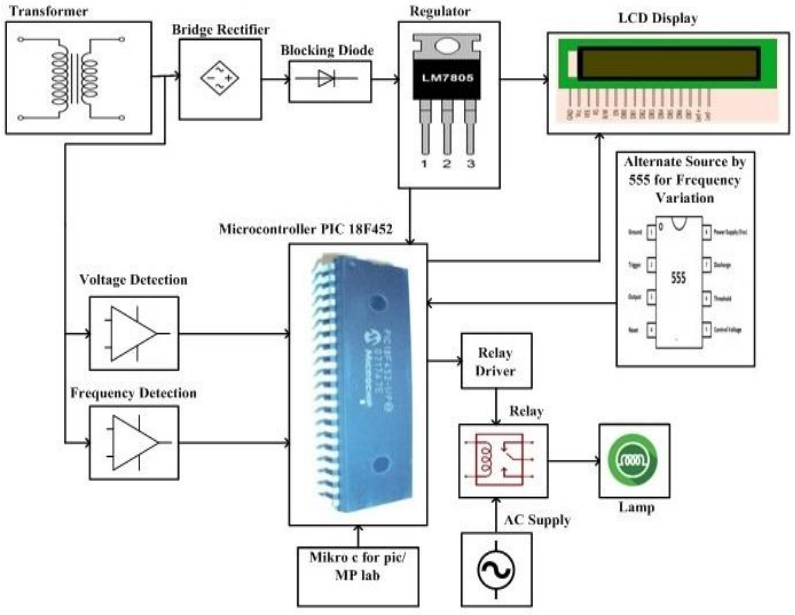

Fig. 1.Block Diagram of detecting power & Synchronization Failure

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1.1 Power Supply Block

A. Transformer

Transformers convert AC electricity from one voltage to another with a little loss of power. Step-up transformers increase voltage, step-down transformers reduce voltage. Most power supplies use a step-down transformer to reduce the dangerously high vokage to a safer low voltage. In this we are considering a 230/12V transformer.

B. Voltage Regulator 7805

The LM78XX/LM78XXA series of three-terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a Wide range of applications. Each type employs internal current limiting, thermal shutdown and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output Current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

C. Rectifier

A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), current that flows in only one direction, a process known as rectification. The output from the transformer is fed to the rectifier. It converts A.C. into pulsating D.C. The rectifier may be a half wave or a full wave rectifier. In this project, a bridge rectifier is used because of its merits like good stability and full wave rectification.

D. Filter

Capacitive filter removes ripples from the output of rectifier and smoothens the D.C. Output received from this filter is constant until the mains voltage and load is maintained constant. However, if either of the two is varied, D.C. voltage received at this point changes. Therefore a regulator is applied at the output stage. This filter is also used in circuits where the power-supply ripple frequency is not critical and can be relatively high

1.2 Microcontroller AT89S52

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density non volatile memory technology and is compatible with the industry standard 80C51 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional non volatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost effective solution to many embedded control applications.

II. FEATURES

- Compatible with MCS-51 Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
- Endurance: 10,000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes • Interrupt Recovery from Power-down Mode
- Watchdog Timer

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- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option

2.1 Pin Configurations of AT89S52

A. Pin Description

- **VCC:** Supply voltage.
- **GND:** Ground
- **Port ():** Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TIL inputs. When Is are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, PO has internal pull ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.
- **Port 1:** Port 1 wan R-bx bidirectional 1/0 port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When is are written to Port 1 pins, they are pulled high by the interned pull ups and can be used as inputs. As inputs, Port I pas that are externally being pulled bow will source current (III.) because of the internal pull-ups. In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P10/12) and the timer counter 2.0iger put (PL 1/12EX)
- **Port 2:** Port 2 an 8-b* bidirectional I/O port with internal pull ups. The Port 2 output buffers can sink/source four TTT inputs. When Is are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs. Port 2 pins that are externally being pulled low will source current (IL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVXDPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-ba addresses (MOVXRD), Port 2 emits the contents of the P2 Special Function Register.
- **Port 3:** Port 3 an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can unk/source four TTL inputs. When Is are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (III) because of the pull-ups.
- **RST:** Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the defauk state of bit DISRTO, the RESET HIGH out feature is enabled.
- **ALE/PROG:** Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.
- In normal operation, ALE is emiated at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE puse is skipped during each access to external data memory,

A. Program Store Enable (PSPN) s the read strobe to extemal program memory When the ATW552 * executing code from external program memory, PSEN in activated twice sich michie tyck, except dat two PSEN activations are skipped during each access to external data memory.

B. EA/VPP:

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory bcations starting at 0000H up to FFFFH. Note, however, that if lock bi 1 is programmed, EA will be intemally

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latched on reset. EA shoukl be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming.

- **XTALI:** Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
- **XTAL2:** Output from the inverting oscillator amplifier

2.2 Oscillator Characteristics

XTALI and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTALI is driven as shown in Figure 6.2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal cbcking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to skep while all the on chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. They on-chip RAM and Special Function Registers retain their vabes until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to is normal operating level held active long enough to allow the oscillator to restart and stabilize.

Liquid crystal display (LCD) has material which combines the properties of both liquid and crystaks. They have a temperature range within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an order form similar to crystal. For an 8-bit data bus, the display requires a +5V supply plus 11 I/O lines. For a 4-bit data bus it only requires the supply lines plus seven extra lines. When the LCD display is not enabled, data lines are tri-state which means they are in a state of high impedance (as though they are disconnected) and this means they do not interfere with the operation of the microcontroller when the display is not being addressed.

555 Timer

The 555 Timer IC is an integrated circuit (chip) implementing a variety of timer and multi vibrator applications. The IC was designed by Hans R. Camenzind in 1970 and brought to market in 1971 by Sinetics (later acquired by Philips). The original name was the SE555 (metal cany/NE555 (plastic DIP) and the part was described as "The IC Time Machine"

Usage

The connection of the pins is as follows:
Pin Name Purpose
GND
Ground, low level (0 V)
2 TRIG OUT rises, and interval starts, when this input falls below 1/3 Vcc.
3 OUT this output is driven to +Ver or GND.
4 RESET A timing interval may be interrupted by driving this input to GND.
5 CTRL "Control access to the internal voltage divider (by defauk, 2/3 Voc).
16 THR The interval ends when the voltage at THR is greater than at CTRL
7 DIS Open collector output; may discharge a capacitor between intervals.
8 V+. Vac Positive supply voltage is usually between 3 and 15 V

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III. CONCLUSION

This paper gives brief idea about indicator which senses the abnormalities in voltage as well as in frequency so as to detect the synchronization failure of any external supply source to the power grid. This type of indicators are much needed in most crowded EHV substations where number of voltage levels, number of sources, number of power transformers and number of load lines are existing. In short it will be beneficial in case of complicated substation because at present the facility available is FTR i.e. Frequency Trip Relay and UFR i.e. Under Frequency Relay which performance function of directly disconnection of particular feeder which may cause sudden rise of voltage on system bus. Also there is a chance for the power system to get imbalance in the absence of such indications and automatic disconnection i.e. islanding..

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