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Cascaded H-Bridge Multilevel Inverter Topology with a Smaller Number of Power Electronic Switching Components

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Abstract: *This topic presents a seven level cascaded H- Bridge MLI based on a Multilevel DC Link (MLDCL) topology and a single full bridge inverter to reduce the no. of power electronics switching devices required by its conventional counterpart. Normally, inverter produces square wave ac output and so it is called as two-level inverter. Compared to two-level inverter, MLI's having high efficiency since they produce accurate sinusoidal output. Cascaded H-Bridge MLI consists of separate full bridge inverters which are connected to individual dc sources for producing different levels in the output voltage. This type is advantageous because, it does not require additional clamping diodes and balancing capacitors as in the case of diode-clamped and flying capacitor types respectively. The unique feature of MLI is, "the more the number of output voltage levels, the less the harmonic content in it." But, if the number of output voltage level is increased, it requires more number of switches which leads to complex complexity. Therefore, the proposed topology introduces a Multilevel DC link using half bridge cells connected to separate DC source which produces the staircase DC voltage and a single H-Bridge inverter to invert that DC voltage to staircase ac output. Thus, the MLDCL inverter significantly reduces the switch count. Multi carrier based PWM is used to operate the switching devices in such a manner so as to achieve good fundamental output with low switching losses. MATLAB/SIMULINK is used to verify the performance of the proposed.*

Keywords: Multilevel Inverter Topology

I. INTRODUCTION

Normally, inverters are used to convert dc input to ac output. Inverters are mainly classified into, two level inverter and multilevel inverter. The voltage source inverters produce an output voltage or current with levels either "0" or "±Vdc" (square wave output). They are known as two level inverters. To produce a quality output voltage or current waveform with less amount of ripple content, they require high switching frequency along with various pulse width modulation (PWM) strategies. In high power high voltage application, these 2 level inverters, however have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. Moreover, the semiconductor switching devices should be used in such a manner as to avoid problems associated with their series- parallel combination that are necessary to obtain capability of handling high voltages and currents. The recent advancement in power electronics has initiated to improve the level of inverter to satisfy the need of medium voltage high power application without the need of transformer which leads to the invention of multilevel inverters (MLI).

These inverter topologies can generate high quality voltage waveform with power semiconductor switches operating at a frequency near the fundamental. It significantly reduces the harmonic problem with reduced voltage stresses across the switch. These limitations can be overcome by using MLI. Compared to 2 level inverter, MLI are having high efficiency since it produce accurate sinusoidal (staircase) output using different levels in the output voltage. This paper focuses on cascaded H-bridge type MLI which is advantageous than other 2 types. A Seven level cascaded H-Bridge Multilevel Inverter based on a multilevel DC link (MLDCL) topology and a single full bridge inverter to reduce the no. of power electronic switching devices required by its conventional counterpart. Normally, inverter produces square wave AC output and so it is called as two level inverter. Compared to two level inverter, Multilevel inverters (MLI's) are having

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high efficiency since they produce accurate sinusoidal (Staircase) output. Cascaded H Bridge Multilevel Inverter consists of separate full bridge inverters which are connected to individual DC source for producing different level in the output voltage. This type is advantageous because, it does not require additional clamping diodes and balancing capacitors as in the case of diode-clamped and flying capacitor types respectively. The unique feature of MLI is, "The more the number of output voltage levels, the less the harmonic content in it." But, if the number of output voltage level is increased, it requires more number of switches which leads to circuit complexity. Therefore, the proposed topology introduces a Multilevel DC link using half bridge cells connected to separate DC source which produces a staircase DC voltage and a single H-Bridge inverter to invert that DC voltage to staircase AC output. Thus, the MLDCL inverter significantly reduces the switch count. Multi Carrier based Pulse Width modulation technique is used to operate the switching devices in such a manner so as to achieve good fundamental output voltage with low switching losses. MATLAB/SIMULINK is used to verify the performance of the proposed model.

1.1 Background

Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.

1.2 Need

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application.

II. OBJECTIVES

A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel inverter can be briefly summarized as follows.

- **Staircase waveform quality:**

Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.

- **Common-mode (CM) voltage:**

Multilevel inverters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies.

- **Input current:**

Multilevel inverters can draw input current with low distortion.

- **Switching frequency:**

Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

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Table 1: Comparison of MLI

CONVERTER TYPE	DIODE CLAMPED	FLYING CAPACITOR	CASCADED H-BRIDGE	PROPOSED MLDCL
Main Switches	(m-1)*2	(m-1)*2	(m-1)*2	m+3
Main Diodes	(m-1)*2	(m-1)*2	(m-1)*2	m+3
Clamping Diodes	(m-1)* (m- 2)	0	0	0
Balancing Capacitors	0	(m-1)* (m- 2)/2	0	0

From this table, we can compare the existing MLI; the new MLDCL inverters can significantly reduce the switchcount as well as the no of gate drivers as the no of voltage level increases. Also, it does not require additional clamping diodes and balancing capacitors as in the case of DCML and FCML type inverters. So it can be seen roughly half the no. of components can be eliminated as 'm' increases. The convectional 7-level CHBMLI requires (m-1)*2= (7-1)*2=12 switching devices. But the proposed CHBMLI inverter requires only m+3= (7+3) =10 switches. Therefore, this proposed type is more advantageous since the no. of switching devices is greatly decreased from (m-1)*2 (convectional) to m+3 (MLDCLI) even if the no. of levels of output voltage are increased.

Pulse width modulation-It is generally accepted that the performance of the inverter with any switching strategies, can be related to the harmonic contents of its output voltage. Power electronic researches have always studied much novel control technique to reduce harmonics in such waveforms. Up-to-date there are many techniques, whichare applied to inverter topologies. One of the most widely utilized strategies for controlling the AC output of power electronic converters is the technique known as PWM. This vary the duty cycle of inverter switches at a high frequency to achieve a target average low frequency output voltage or current. Similar to two level inverter, there are different types of modulation techniques adopted for MLI.

Sinusoidal PWM (SPWM) is one of the primitive techniques, which are used to suppress harmonics presented in quasi-square wave. In this method, the sinusoidal reference waveform of each phase and a periodic triangular carrier wave are compared and the intersections points determine the commutation instants of the associated inverter leg switches. In multilevel case, SPWM technique uses carrier disposition PWM (CDPWM) where modulation is achieved by m-1 triangular carriers where m is the no. of voltage levels. These carriers are arranged so that they fully occupy continuous bands in the range of – (m-1) Vdc/2 to (m- 1)Vdc/2. A single sinusoidal reference is then comparedwith these carriers to determine the switched voltage level.

Therefore, for our 7-level CHBMLI, 6 triangular carriers are required which occupy the continuous bands in the range of -3Vdc to +3Vdc. The degree of freedom for this CDPWM technique is,

$$Ma = 2 \times Ar/ (m-1) \times Ac.$$

Where, 'Ar' represents the reference waveform amplitude. 'Ac' represents the carrier waveform amplitude. 'm' denotes the no. of levels

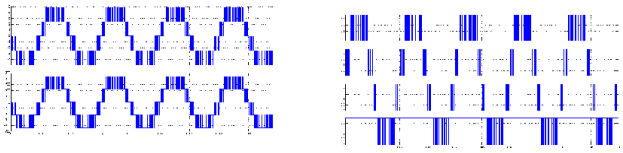

Chart -1: Output of MLI

For producing 7 level output voltage, the CHBMLI requires 3 single phase full bridge inverters which are connected in series as shown in circuit diagram in above fig. these 3 inverter bridges are connected to 3 independent dc sources which are having equal amplitude and therefore it is called is (symmetrical MLI). If the input dc sources are of different amplitudes, then it is called as ASMLI.

The harmonics present in the output voltage can be analyzed in terms of Total Harmonic Distortion (THD) by performing Fast Fourier Transform (FFT) analysis using MATLAB. In this topology, the no. of output phase voltage levels is defines by m=2s+1, where S is the no. of dc sources. The convectional 7- level CHBMLI requires 2(m-1)= 2(7-1)= 12 switches. The main advantage of this CHBMLI topology is that the total harmonic distortion (THD) present in the output voltage gets

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decreased if the no. of output voltage level is increased greatly. But there is a difficulty to achieve this, that is, it requires more no. of switching devices to generate more no. of levels. This leads to circuit complexity and more cost. A better solution to this problem is MLDCL topology.

III. Conclusion

Both the convectional 7-Level CHBML inverter and the proposed cascaded H-bridge MLDCL topology was simulated and it is concluded that for producing the same 7-Level output voltage, the proposed MLDCL inverter requires only 10 switches whereas the convectional type requires 12 switches. This difference will be larger if the no. of output voltage level is further increased. Therefore, the proposed cascaded H-Bridge MLDCL topology can eliminate roughly half the no. of switches, their gate drivers compared with the exiting cascaded MLI counterparts. Despite a higher total VA rating of the switches, the cascaded MLDCL inverters are cost less due to the savings from the eliminated gate drivers. This can be developed by interfacing renewable energy resources for providing DC supply to the proposed inverter circuit. Solar cells, wing energy generators, fuel cells, etc. can be interfaced with this MLDCL inverter to obtain high efficiency and also with low cost.

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