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Design of Low-Power High Performance 2–4 and 4–16 Mixed-Logic Line Decoders

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Abstract: *This brief presents a blended rationale plan technique for line decoders, consolidating transmission door rationale, pass semiconductor double worth rationale, and static reciprocal metal-oxide semiconductor (CMOS). Two epic geographies are introduced for the 2–4 decoder: a 14transistor geography pointing on limiting semiconductor tally and force dissemination and a 15transistor geography pointing on high force postpone execution. Both ordinary and altering decoders are actualized for each situation, yielding an aggregate of four new plans. Moreover, four new 4–16 decoders are planned by utilizing blended rationale 2–4 pre decoders joined with standard CMOS post decoder. All proposed decoders have full-swinging ability and diminished semiconductor check contrasted with their traditional CMOS partners. At long last, an assortment of similar zest recreations at 32 nm shows that the proposed circuits present a huge improvement in force and postponement, outflanking CMOS in practically all cases.*

I. Introduction

Very large scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. Over the past decade, power consumption of VLSI chips has constantly been increasing. Moore's Law drives VLSI technology to continuous increases in transistor densities and higher clock frequencies. The trends in VLSI technology scaling in the last few years show that the number of on-chip transistors increase about 40% every year. The operating frequency of VLSI systems increases about 30% every year. Although capacitances and supply voltages scale down meanwhile, power consumption of the VLSI chips is increasing continuously. On the other hand, cooling systems cannot improve as fast as the power consumption increases. Therefore in the very close future chips are expected to have limitations of cooling system and solving this problem will be expensive and inefficient. The main objective of Analysis of low power high performance 2-4 and 4-16 mixed line logic decoders is to reduce the power consumption. The power consumption can be reduced by minimizing the transistor count by using mixed logic design when compared to CMOS logic design. We design 2-4 and 4-16 decoders using mixed logic as well as CMOS logic and compare the results between them. In VLSI systems there is a trade-off between three parameters those are power, area and speed. To obtain better results in two parameters the third parameter should be negligible. Here we are designing low power and high performance decoders individually. So in order to design a low power and area

II. Existing System

2.1 Decoder

In digital systems, instructions as well as numbers are conveyed by means of binary levels or pulse trains. A decoder is a logic circuit that converts an N-bit binary input code into M output lines such that only one output line is activated for each one of the possible combinations of inputs. The decoder identifies or recognizes or detects a code. The N inputs can be a 0 or a 1, there are 2^N possible input combinations or codes. For each of input combination only one of the M outputs will be active (HIGH), all other outputs will remain inactive (LOW). Some decoders are designed to produce active LOW output, while all the other outputs remain HIGH.

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2.2 2–To-4 Decoder using CMOS Technology

In this paper, a 2-to-4 Decoder has been designed to reduce power consumption and surface area using 65nm, 45nm and 32nm complementary- metal- oxide semiconductor technology, which is then analysed and comparative study has been done in account of the silicon surface area and power consumption. The proposed 2-to-4 Decoder using 32nm CMOS technology gives better results in terms of power and surface area as compare to 45nm and 65nm COMS technologies. The 2- to-4 decoder circuit size is 14.3 µm2 and typical power consumption is 0.172 µW at 32nm CMOS technology [2] –[5].

Comparison of proposed 2-to-4 Decoder is based on the performance parameters like surface area and power dissipation to achieve better performance using CMOS process by Micro wind 3.1 in 32nm, 45nm and 65nm technology. The proposed 2-to-4 Decoder circuit shown in figure 3, uses four 2-bit AND and two NOT logic gates.

A. Drawbacks

In this mainly disadvantage of the project different of technologies and different design construction

2.3 Low Power CMOS Full Adders Using Pass Transistor Logic

The efficiency of a system mainly depends on the performance of internal components present in the system. The internal components should be designed in such a way that they consume low power with high speed. Lot of components is in circuits including full adder. This is mainly used in processors. A new Pass transistor full adder circuit is implemented in this paper. The main idea is to introduce the design of high performance and based pass transistor full adders which acquires less area and transistor count. The high performance of pass transistor low power full adder circuit is designed, and the simulation has been carried out on Tanner EDA Tool. The result shows that the proposed full adder is an efficient full adder cell with least MOS transistor count that reduces the high-power consumption and increases the speed. In this paper CMOS full adder circuits are designed to reduce the power and area and to increase the speed of operation in arithmetic application. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem [1]- [17],

III. Proposed System

Transmission gate logic (TGL) can efficiently implement AND/OR gates , thus it can be applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 3.1(a) and (b), respectively. They are full swinging, but not restoring for all input combinations. Regarding PTL, there are two main circuit styles: those that use nMOS only pass transistor circuits, like CPL, and those that use both nMOS and pMOS pass transistors, like DPL and DVL. The style we consider in this work is DVL, which preserves the full swing operation of DPL with reduced transistor count . The 2-input DVL AND/OR gates are shown in Fig. 4.1(c) and (d), respectively. They are full swinging but non-restoring, as well.

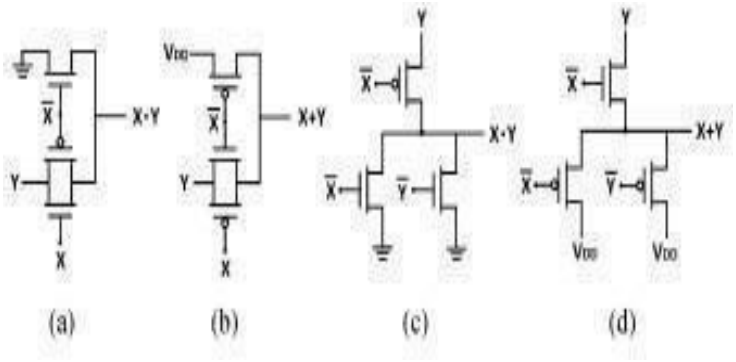

Figure. 3.1: Three-transistor AND/OR gates considered in this work. (a) TGL AND gate. (b) TGL OR gate. (c) DVL AND gate. (d) DVL OR gate.

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Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors. Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, i.e. the fact that they do not have balanced input loads. As shown in Fig.4.1, we labeled the 2 gate inputs X and Y . In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output.

We will refer to X and Y as the control signal and propagate signal of the gate, respectively. Using a complementary input as the propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A B) or implication (A + B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND(AB) or OR (A + B) function, either choice is equally efficient. Finally, when implementing the NAND (A + B) or NOR (A B) function, either choice results to a complementary propagate signal, perforce.

IV. RTL Simulation and Results

The simulation results regarding power, PDP and delay are shown in Tables III– V, respectively. Each of the proposed designs will be compared to its conventional counterpart.Specifically,2–4LPand2–4HParecomparedto20T,2–4LPIand2–4HPI are compared to inverting 20T, 4–16LP and 4–16HP are compared to 104T and finally, 4–16LPI and 4–16HPI are compared to inverting 104T. According to the obtained results,2–4LP presents 9.3% less power dissipation than CMOS20T, while introducing a cost of 26.7% higher delay and 15.7% higher PDP. On the other hand, 2–4HP outperforms CMOS20T in all aspects, reducing power, delay, and PDP by 8.2%, 4.3%, and 15.7%, respectively. Both of our inverting designs, 2–4LPI and 2–4HPI, outperform CMOS 20T inverting in all aspects as well. Specifically, 2–4LPI reduces power, delay, and PDP by 13.3%, 11%, and 25% respectively, while 2–4HPI does so by 11.2%, 13.2%, and 25.7%. Regarding the 4–16 simulations, the obtained results are similar. The 4–16LPI decoder, presents 6.4% lower power dissipation with the cost of 17.9%higher delay and 1.9% higher PDP than CMOS 104T. The rest of the decoders, namely, 4– 16LP, 4–16HP, and4–16HPI, present better results than corresponding CMOS decoders in all cases, which can be summarized.

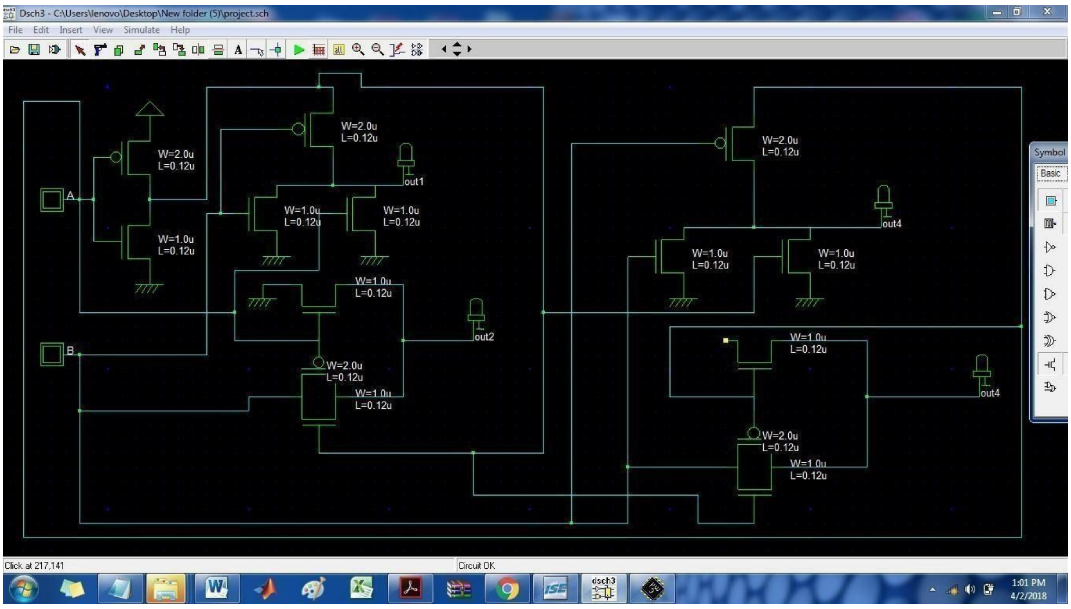

Figure 4.1 (a): Architecture

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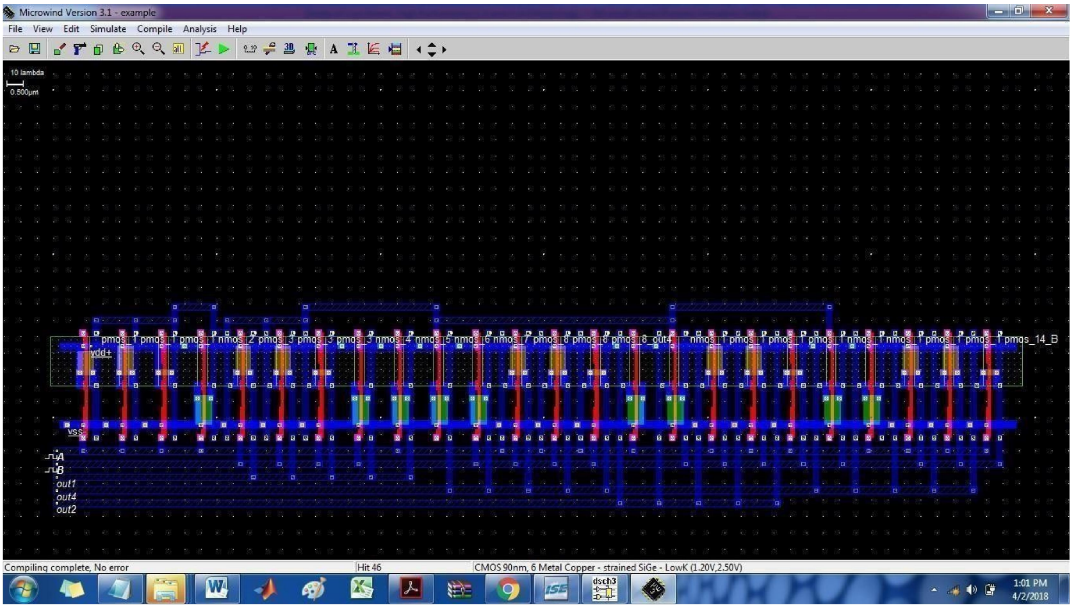

Figure 4.1(b) : Layout diagram

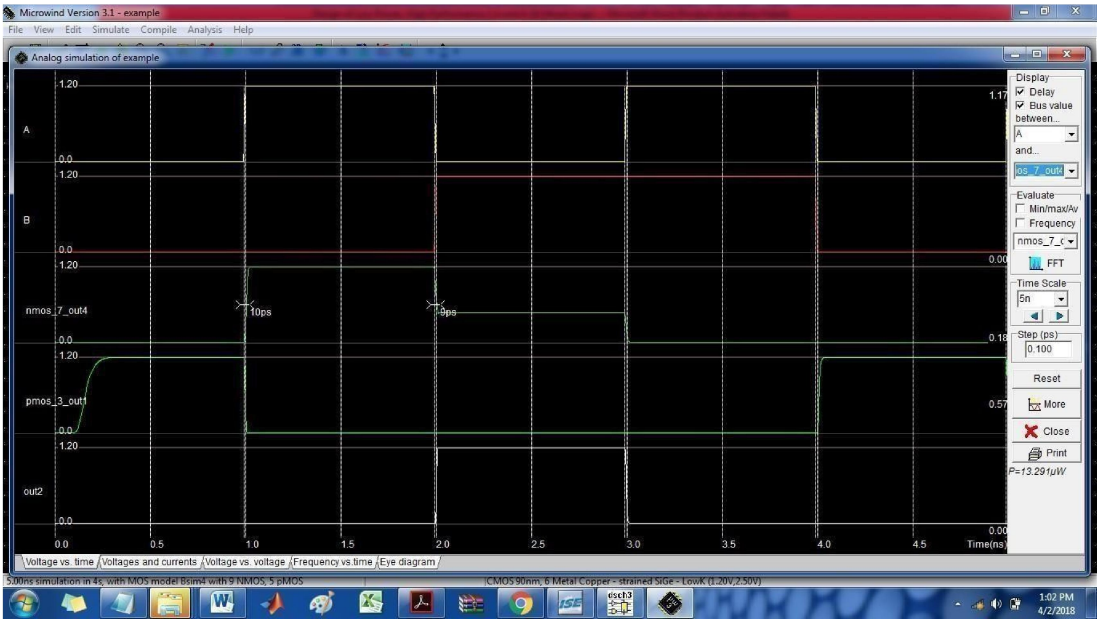

Figure 4.1(c): Waveforms FIGURE 7.1: Output for 14 transistor 2-4 line decoder

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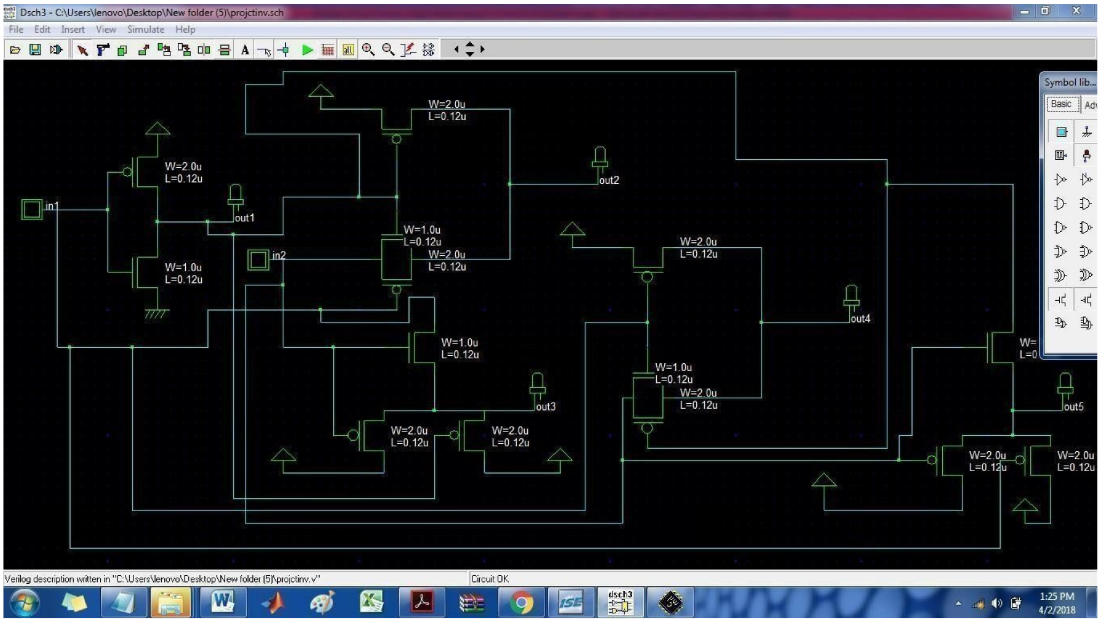

Figure 4.2(a): Architecture

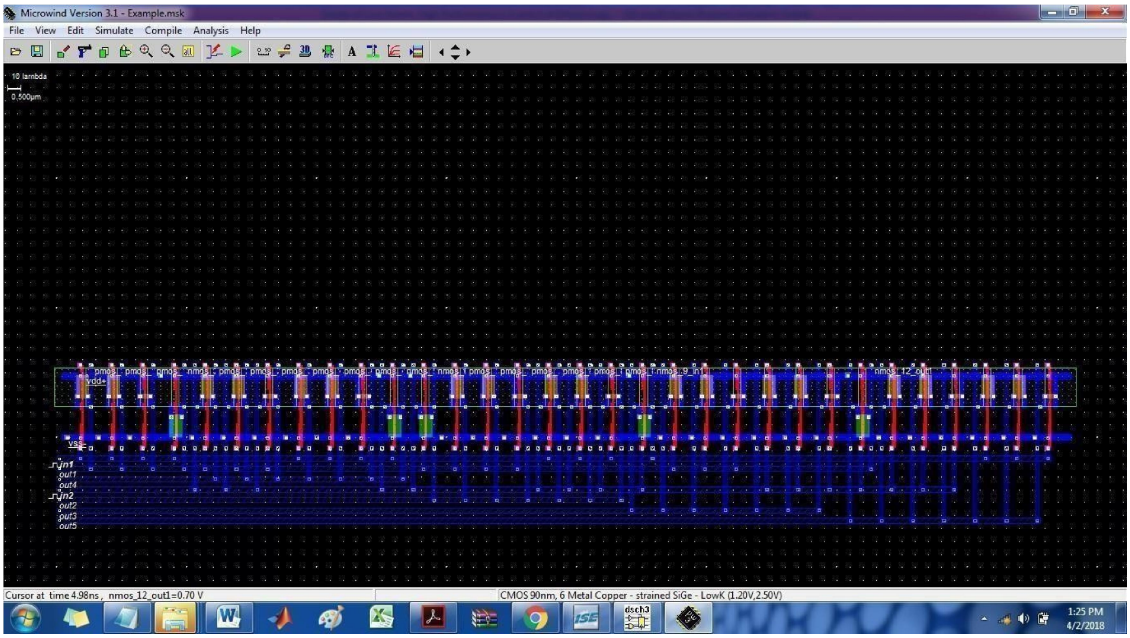

Figure 4.2(b): Layout diagram

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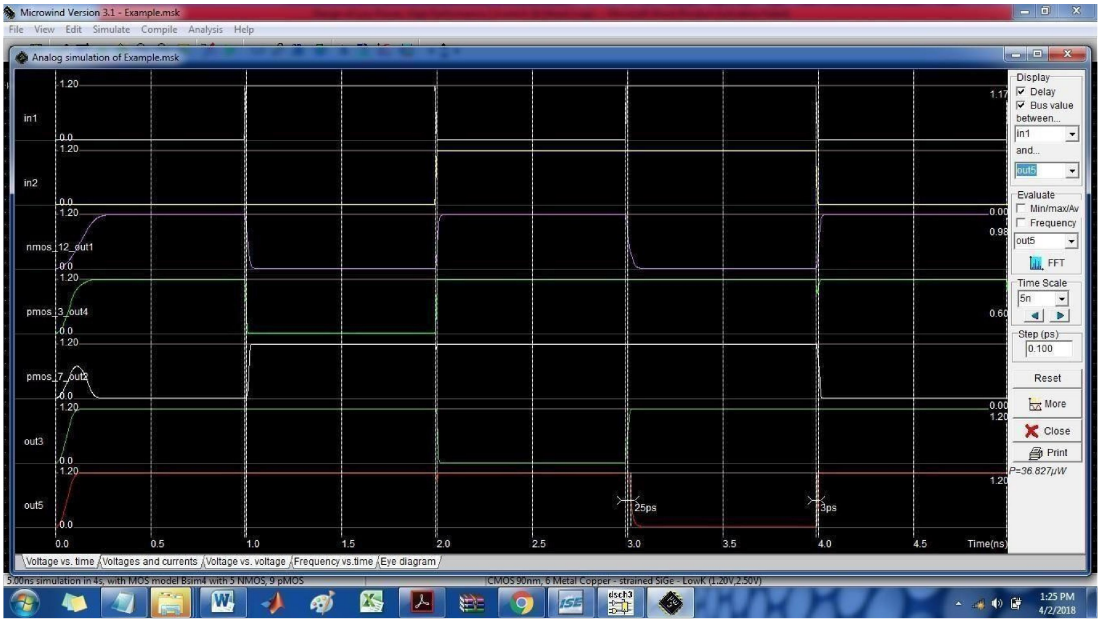

Figure 4.2(c): Waveforms

Figure 4.2: The output for 14 transistor 2-4 line decoder

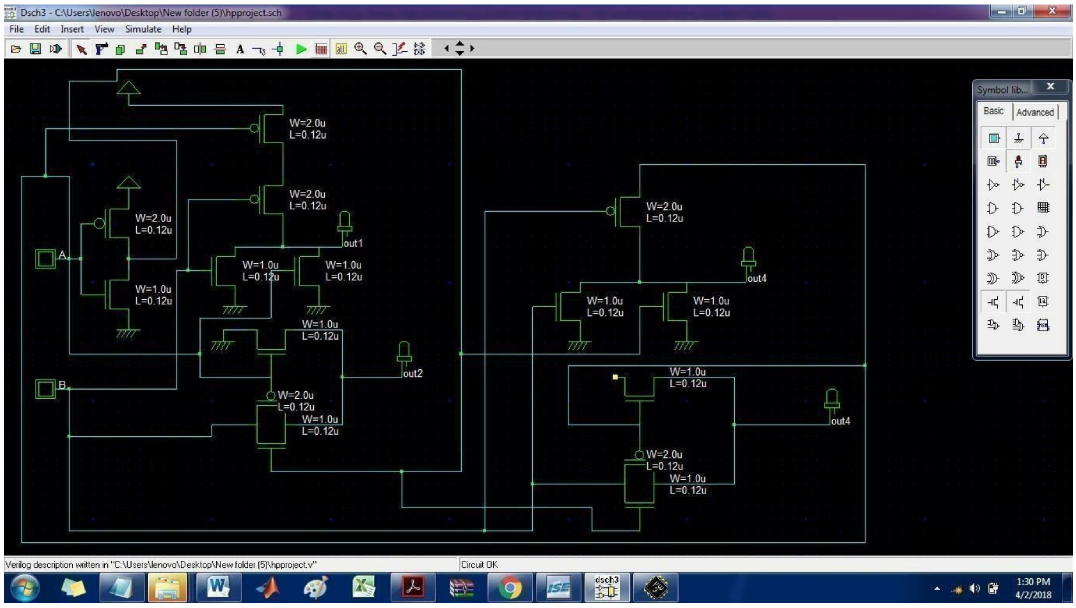

Figure 4.3 (a): Architecture

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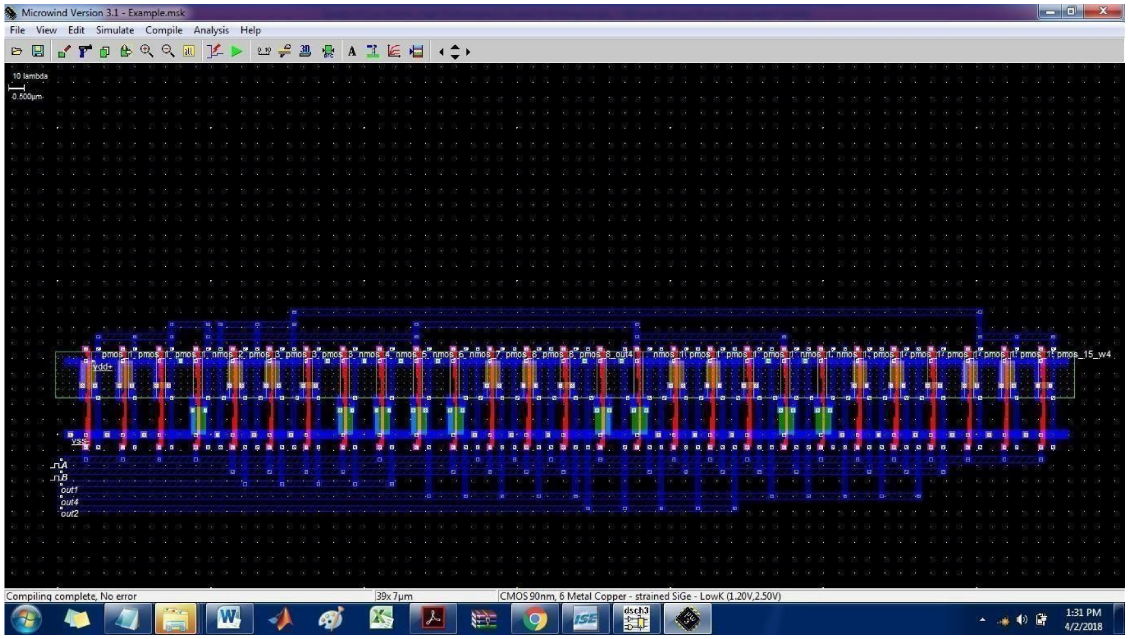

Figure 4.3 (b): Layout diagram

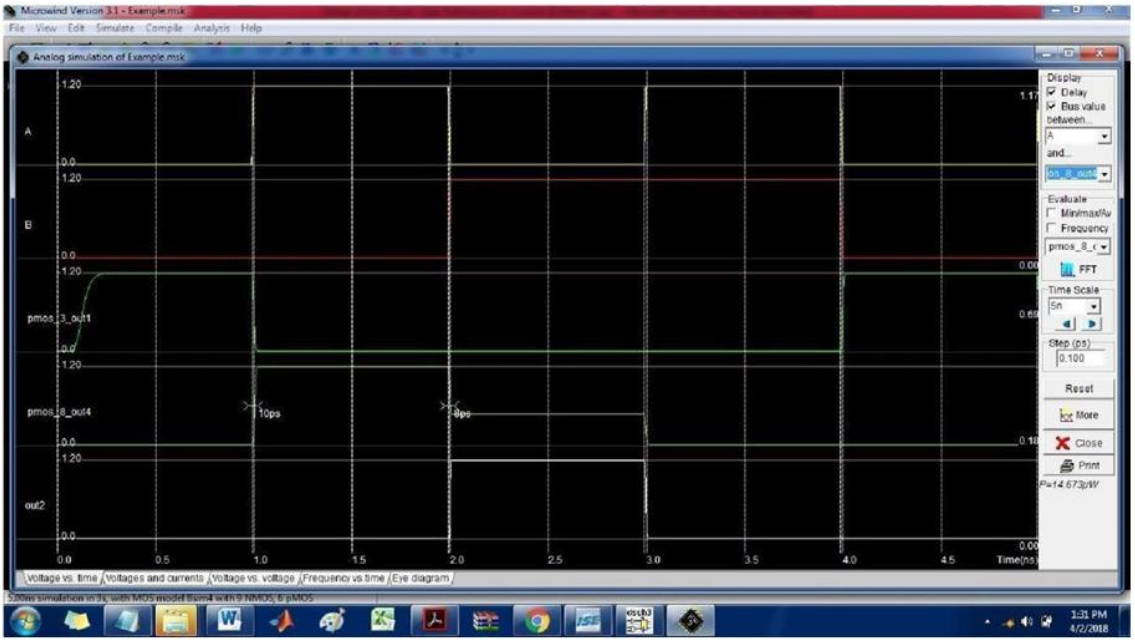

Figure 4.3 (c): Waveforms

Figure 4.3: The output for 2-4 mixed logic line decoder

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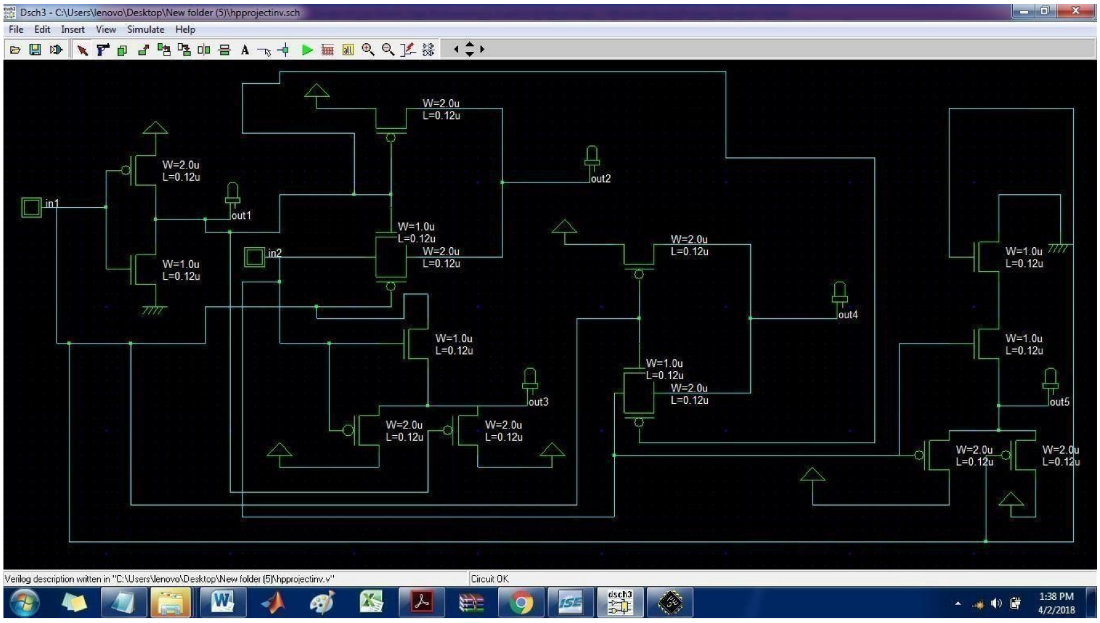

Figure 4.4 (a): Architecture

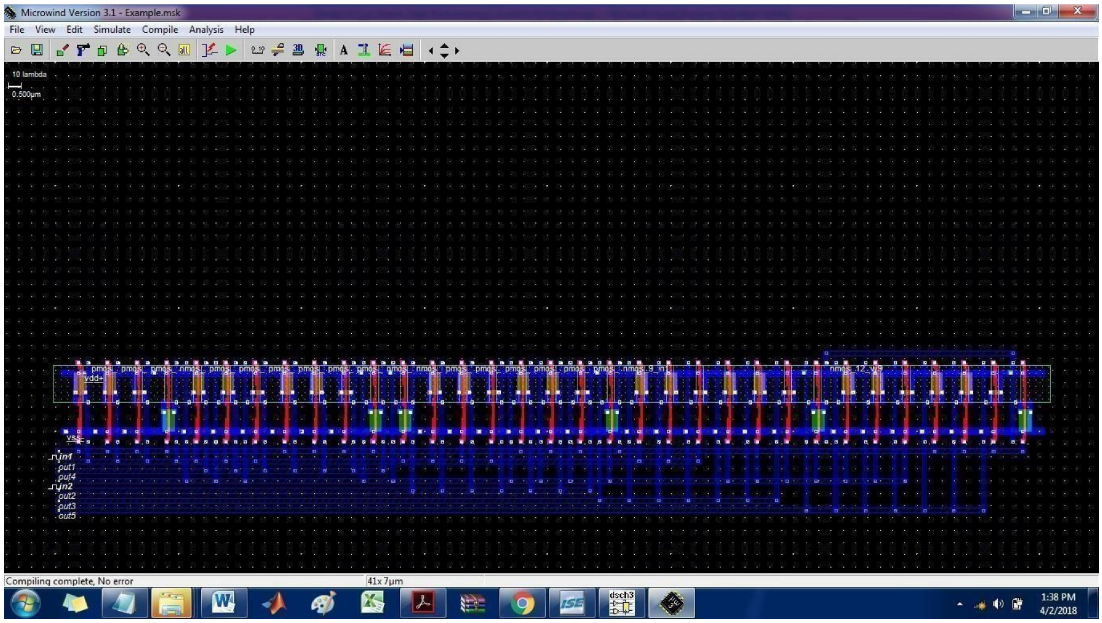

Figure 4.4 (b): Layout diagram

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Figure 4.4 (c) : Waveforms

Figure:4.4: Output for 4-16 mixed logic line decoder

V. CONCLUSION

This brief has presented an effective blended rationale plan for decoder circuits, joining TGL, DVL and static CMOS. By utilizing this approach, we created four new 2–4 line decoder geographies, in particular 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer diminished semiconductor tally and improved force defer execution comparable to ordinary CMOS decoders. Besides, four new 4–16 line decoder geographies were introduced, to be specific 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, acknowledged by utilizing the blended rationale 2-4 decoders as pre disentangling circuits, joined with post decoders actualized in static CMOS to give driving ability. An assortment of near flavor reenactments was performed at 32 nm, checking, as a rule, an unmistakable preferred position for the proposed plans. The 2–4LP and 4–16LPI geographies are generally appropriate for applications where region and force minimization is of essential concern. The 2–4LPI, 2–4HP, and 2–4HPI, just as the comparing 4–16 geographies (4–16LP, 4–16HPI, and 4–16HP), end up being reasonable and all-around productive plans; hence, they can adequately be utilized as building blocks in the plan of bigger decoders, multiplexers, and other combinational circuits of fluctuating execution prerequisites. Additionally, the introduced decreased semiconductor tally and low force attributes can profit both mass CMOS and SOI plans too. The acquired circuits are to be executed on format level, making them reasonable for standard cell libraries and RTL plan.

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