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A Extensive Review of Recent Technologies and Trends in Low-Power VLSI Design

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Abstract: *The demand for energy-efficient electronic devices has driven significant advancements in low-power Very-Large-Scale Integration (VLSI) design. This paper presents a Extensive review of the recent technologies and trends that have emerged to address the challenges associated with power utilization in VLSI circuits. The review covers a broad spectrum of innovations, including advanced transistor technologies such as FinFETs, Gate-All-Around (GAA) FETs, and Silicon-on-Insulator (SOI), which offer improved power efficiency. It also explores cutting-edge power enhance techniques like Dynamic Voltage and Frequency Scaling (DVFS), power gating, and Multi-Threshold CMOS (MTCMOS), highlighting their impact on reducing both dynamic and leakage power. Further, the paper examines energy-efficient architectures, including Near-Threshold Computing (NTC), approximate computing, and asynchronous circuits, which promise substantial power savings. The fusing of machine learning and AI in power optimization and the development of advanced Electronic Design Automation tools are also discussed as emerging trends. Finally, the paper considers future directions, including the potential of 3D Integrated Circuits (3D ICs), quantum and neuromorphic computing, and post-CMOS technologies, to revolutionize low-power VLSI design. This review provides a critical exploration of the actual state of the art and offers comprehensions into the future trajectory of low-power VLSI, making it a valuable resource for researchers and practitioners in the field.*

Keywords: Low-Power Vlsi Design, DVFS, Power gating , Near-Threshold Computing, Machine Learning and AI

I. INTRODUCTION

A. Overview of Low-Power VLSI Design

VLSI design talk about the process of fabricating integrated circuits by integrating millions of transistors onto a single chip. As electronic devices become more ubiquitous and their applications expand into areas like IoT, wearables, and mobile computing, therefore low-power VLSI design has grown exponentially. Low-power design is key for extending battery life, reducing heat dissipation, and enabling sustainable technology.

B. Motivation for Low-Power Design

The drive for low-power VLSI stems from the increasing need for portable and energy-efficient devices. This need is further amplified by environmental concerns and the restrictions of battery technology. Efficient power management directly impacts device performance, cost, and longevity.

C. Objective and Scope of the Review

The purpose of this review is to provide a detailed review of recent advancements in low-power VLSI design. The paper explores the latest technologies, methodologies, and trends, offering a critical analysis of their impact and future potential.

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II. METHODOLOGY

A. Literature Search and Selection Criteria

FinFET technology emerged as a solution to the limitations of planar transistors, particularly in controlling short-channel effects and reducing leakage currents. The three-dimensional structure of FinFETs imparts better gate control over the channel, leading to improved performance at lower power levels. Research has concentrated on optimizing FinFET design for ultra-low-power applications. For example, multi-gate FinFETs have been explored to further enhance power efficiency. Studies show that FinFETs can perform remarkable power savings match up to traditional CMOS technology [4][5].

GAA FETs are an evolution of FinFETs, where the gate material completely surrounds the channel, offering even better electrostatic control. This architecture is specifically encouraging for scaling down to sub-5nm technologies. Research has concentrated on the fabrication and performance analysis of GAA FETs. Experimental results indicate that GAA FETs can reduce power consumption by up to 50% compared to FinFETs, creating them most suitable for next-generation low-power applications [7].

SOI technology reduces parasitic capacitance, resulting in lower power dissipation. SOI-based devices are particularly effective in high-performance computing and mobile applications. The use of fully depleted SOI (FD-SOI) has shown to further reduce leakage currents and improve power efficiency. FD-SOI is gaining traction in applications need both high performance and low power [8][9].

DVFS is a well-established technique that adjusts the voltage and frequency of a processor based on workload demands, thereby minimising power utilization during periods of low computational demand. Recent research has focused on adaptive DVFS algorithms that leverage machine learning to predict workload patterns and optimize power usage dynamically. These techniques have been significantly effective in multicore processors, achieving power reductions of up to 40% [10].

Power gating minimizes leakage power by turning off the power to inactive sections of a chip. This technique is crucial in systems-on-chip (SoCs), where different components are used intermittently. Research has focused on fine-grained power gating approaches that allow for much precise control over power states, leading to significant reductions in leakage power, particularly during idle periods [11].

MTCMOS technology uses transistors with varying threshold voltages to balance power consumption and performance. High-threshold transistors reduce leakage, while low-threshold transistors maintain performance. Recent studies have concentrated on optimizing the threshold voltage selection process to maximize power savings without compromising performance. MTCMOS has been successfully implemented in various low-power designs, achieving leakage power reductions of up to 30% [12].

NTC operates transistors at voltages near their threshold voltage, significantly reducing dynamic power. While this can lead to performance degradation, it offers substantial energy savings in applications where power efficiency is paramount. Research in this area has focused on mitigating the performance trade-offs associated with NTC through architectural innovations and error correction techniques [13][14].

Approximate computing reduces power by allowing for controlled errors in computation, which is acceptable in applications like image processing or machine learning where exact precision is not always necessary. Recent work has explored the effort of approximate adders and multipliers that significantly minimizes power utilisation with minimal impact on output quality [15].

Asynchronous circuits operate without a global clock, reducing power associated with clock distribution and synchronization. This approach is particularly beneficial in ultra-low-power and energy-harvesting applications. Research has concentrated on optimizing asynchronous design methodologies to improve power efficiency and reliability[16][17].

Machine learning functions are being used to optimize power consumption during both design and runtime. These algorithms can predict optimal power states and configurations based on workload patterns. Studies have shown that

ML-driven power management can improve efficiency by dynamically adjusting power settings in reaction to changing workloads [18][19].

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AI-driven Electronic Design Automation tools are being developed to automate the design process and optimize power utilization more effectively than traditional methods. These tools leverage AI to identify and mitigate power bottlenecks early in the design process, reducing design time and improving power efficiency[20].

3D ICs involve stacking multiple layers of circuits vertically, which reduces interconnect lengths and thereby power consumption. This approach allows for more efficient use of chip area. Research has concentrated on overcoming challenges related to heat dissipation and manufacturing scalability. Despite these challenges, 3D ICs have demonstrated up to 50% reduction in power consumption in prototype systems[21].

Beyond CMOS technologies, like spintronics and photonics, offer new pathways to reduce power consumption in future VLSI systems. These approaches could significantly replace traditional semiconductor-based designs in certain applications. Early research in spintronics and photonics has shown promise in achieving lower power utilization while maintaining or enhancing performance. However, commercial viability remains a significant challenge[22][23].

Quantum computing and neuromorphic computing represent potential future directions for VLSI, offering fundamentally different approaches to computation that could drastically reduce power consumption. While these approaches are still in their origins, they provide exciting possibilities for the future of low-power design, particularly in specialized applications such as AI and machine learning [24].

B. Organization of the Review

The paper is arranged into sections that cover advanced transistor technologies, power optimization techniques, energy-efficient architectures, machine learning in VLSI, and emerging trends. Each section provides a synthesis of recent research, followed by a comparative analysis and discussion.

III. ADVANCED TRANSISTOR TECHNOLOGIES

A. FinFETs and Gate-All-Around (GAA) FETs

FinFETs have become the industry standard for advanced nodes due to their superior control over short-channel effects and reduced leakage currents. GAA FETs, a further evolution, offer even better electrostatic control by surrounding the channel with the gate material. These technologies are pivotal in achieving reduced power utilisation while maintaining high performance.

Key Studies: Recent research has demonstrated the effectiveness of GAA FETs in reducing power consumption by up to 50% compared to traditional planar transistors.

B. Silicon-on-Insulator (SOI)

SOI technology reduces parasitic capacitance, thereby lowering power dissipation. The thin insulating layer in SOI devices minimizes leakage currents, making them ideal for low-power applications.

Key Studies: SOI-based designs have been shown to achieve significant power savings, particularly in high-performance computing and mobile applications.

C. Emerging Transistor Technologies

Beyond FinFETs and GAA FETs, materials like graphene and carbon nanotubes are being inspected for their possible to further lower power utilisation while enhancing performance.

Key Studies: Experimental devices using carbon nanotubes have demonstrated ultra-low power consumption, but challenges in manufacturing scalability remain

IV. POWER OPTIMIZATION TECHNIQUES

A. Dynamic Voltage and Frequency Scaling (DVFS)

DVFS is a widely adopted technique that adjusts the voltage and frequency of a processor based on workload demands. This technique allows for potential power savings during periods of low computational demand.

Key Studies: Recent implementations of DVFS in multicore processors have achieved up to 40% reduction in power utilization without compromising performance.

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B. Power Gating

Power gating require turning off the power to inactive sections of a chip, thereby reducing leakage power. This technique is especially effective in systems-on-chip (SoCs) where different components are used intermittently.

Key Studies: Research has exhibit that power gating can reduce leakage power by up to 70%, particularly in idle states.

C. Multi-Threshold CMOS (MTCMOS)

MTCMOS technology uses transistors with many different threshold voltages to power consumption and balance performance. High-threshold transistors reduce leakage, while low-threshold transistors maintain performance.

Key Studies: MTCMOS has been successfully implemented in various low-power designs, offering up to 30% reduction in leakage power.

V. ENERGY-EFFICIENT ARCHITECTURES

A. Near-Threshold Computing (NTC)

NTC operates transistors at voltages near their threshold voltage, significantly reducing dynamic power. While this can conduct to performance degradation, it offers substantial energy savings in applications where power efficiency is paramount.

Key Studies: Recent NTC implementations have achieved energy reductions of over 70% in specific low-power applications, although with a trade-off in processing speed.

B. Approximate Computing

Approximate computing reduces power by allowing for controlled errors in computation, which is acceptable in certain applications like image processing or machine learning where exact precision is not always necessary.

Key Studies: Studies have exhibits that approximate computing can lower power utilization by 50% or more, depending on the application.

C. Asynchronous Circuits

Unlike traditional synchronous circuits that rely on a global clock, asynchronous circuits operate without a global clock, reducing power associated with clock distribution and synchronization.

Key Studies: Asynchronous designs have demonstrated power savings of up to 30%, particularly in low-power and ultra-low-power applications.

VI. MACHINE LEARNING AND AI IN LOW-POWER DESIGN

A. Application of Machine Learning

Machine learning functions are being used to optimize power consumption during both design and runtime. These algorithms can predict optimal power states and configurations based on workload patterns.

Key Studies: ML-driven power management has been exhibits to improve power efficiency by up to 20% in complex VLSI systems.

B. AI-Driven EDA Tools

AI-driven Electronic Design Automation tools are being developed to automate the design process and optimize power utilisation more effectively than traditional methods.

Key Studies: AI-driven EDA tools have reduced design time and improved power efficiency by identifying and mitigating power bottlenecks early in the design process.

VII. EMERGING TECHNOLOGIES AND FUTURE DIRECTIONS

A. 3D Integrated Circuits (3D ICs)

3D ICs involve stacking multiple layers of circuits vertically, which reduces interconnect lengths and thereby power consumption. This 3D ICs technology too allows for more efficient use of chip area.

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Key Studies: 3D ICs have demonstrated up to 50% redction in power consumption in prototype systems, although challenges in heat dissipation and manufacturing remain.

B. Quantum and Neuromorphic Computing

Quantum computing and neuromorphic computing represent potential future directions for VLSI, offering fundamentally different approaches to computation that could drastically reduce power consumption.

Key Studies: While still in experimental stages, quantum computing research suggests significant energy savings for certain types of computations, while neuromorphic designs aim to mimic the brain's energy-efficient processing.

C. Beyond CMOS

Beyond CMOS technologies, such as spintronics and photonics, are being explored as alternatives to traditional semiconductor-based designs. These technologies could offer new pathways to reducing power consumption in future VLSI systems.

Key Studies: Early research in spintronics and photonics has shown promise in reducing power while maintaining or even enhancing performance, although commercial viability is still a challenge.

VIII. COMPARATIVE ANALYSIS

A. Performance vs. Power Trade-offs

Each technology and methodology reviewed offers unique trade-offs between power savings and performance. This section compares these trade-offs, providing a framework for selecting the appropriate approach based on particular application needs.

B. Market Adoption and Challenges

Despite the potential benefits, the acquisition of these technologies faces challenges such as cost, complexity, and requires new design methodologies. This section discusses the current state of market adoption and the barriers that must be overcome.

IX. CONCLUSION

A. Summary of Key Trends

The review highlights the significant strides made in low-power VLSI design, with advanced transistor technologies, power optimization techniques, and energy-efficient architectures leading the way.

B. Impact on the Industry

The ongoing innovations in low-power VLSI are poised to have a impact on the electronics industry, driving the evolution of more energy-efficient devices and systems

C. Future Research Directions

Future research should focus on overcoming the issues associated with emerging technologies and exploring new materials and architectures that could further reduce power consumption.

REFERENCES

[1]. A.P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low-Power CMOS Digital Design", IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473-484, April 1992.

[2]. J. Rabaey and M. Pedram, "Introduction" in Low Power Design Methodologies, New York:Kluwer Academic Publisher, pp. 5-16, 1996.

[3]. A.P. Chandrakasan, R. Mehra, M. Potkonjak, J. Rabaey and R.W. Brodersen, "Optimizing Power Using Transformations", IEEE Trans. On CAD, pp. 13-32, Jan. 1995.

[4]. B. Jeevan;K. Sivani "A new 18nm FinFET-based Programmable Logic Array type Multiplexer for High-speed and Low-Power applications" IEEE 20th India Council International Conference (INDICON) 2023.

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[5]. Jency Rubia J; Ezhil E Nithila; Sherin Shibi C; Babitha Lincy R "Design and Analysis of RNS based Montgomery multiplier using FinFET Technology", IEEE 9th International Conference for Convergence in Technology (I2CT), 2024.
[6]. Mukesh Kumar;Kanika Jindal;Pawan Kumar Shukla "Enhancing Low-Power SRAM Performance with FinFET Integration: A 10T Model Analysis" IEEE International Conference on Communication, Computer Sciences and Engineering (IC3SE), 2024.
[7]. Shuo Zhang;Jun Z. Huang;Hao Xie;Afshan Khaliq;Dawei Wang;Wenchao Chen;Kai Miao;Hongsheng Chen;Wen-Yan Yin,"Design Considerations for Si- and Ge-Stacked Nanosheet pMOSFETs Based on Quantum Transport Simulations" IEEE Transactions on Electron Devices,2020.
[8]. Nilesh Anand Srivastava;Anjali Priya;Ram Awadh Mishra,"Performance evaluation of Hetero-Gate-Dielectric Re-S/D SOI MOSFET for low Power Applications" IEEE International Conference on Electrical, Electronics and Computer Engineering (UPCON),2019.
[9]. V. Ostwal;R. Meshram;B. Rajendran;U. Ganguly,"An ultra-compact and low power neuron based on SOI platform", IEEE International Symposium on VLSI Technology, Systems and Applications,2015.
[10]. Inkwon Hwang;Massoud Pedram, "A Comparative Study of the Effectiveness of CPU Consolidation Versus Dynamic Voltage and Frequency Scaling in a Virtualized Multicore Server " IEEE Transactions on Very Large Scale Integration (VLSI) Systems,2016.
[11]. Dustin Peterson; Oliver Bringmann,"Power-Gating Models for Rapid Design Exploration" 17th IEEE International New Circuits and Systems Conference (NEWCAS), 2019.
[12]. Chamak Ganguly; Mazeda Zafor Meem; S.M Kifayat Kabir; Satyendra N. Biswas, Analysis of a Low-Power Full Adder and Half Adder Using a New Adiabatic Logic, 26th International Conference on Computer and Information Technology (ICCIT), 2023.
[13]. Pramesh Pandey,Noel Daniel Gundi,Prabal Basu,Tahmoures Shabanian,Mitchell Craig Patrick,Koushik Chakraborty andSanghamitra Roy, "Challenges and Opportunities in Near-Threshold DNN Accelerators around Timing Errors", Low Power Electron. Appl. 2020, 10(4), 33; https://doi.org/10.3390/jlpea10040033 - 16 Oct 2020.
[14]. Mehdi Tahoori andMohammad Saber Golanbari," Cross-Layer Reliability, Energy Efficiency, and Performance Optimization of Near-Threshold Data Paths",Low Power Electron. Appl. 2020, 10(4), 42; https://doi.org/10.3390/jlpea10040042 - 3 Dec 2020.
[15]. Sarangam K; B. Chandrababu Naik; B. Naresh Kumar Reddy; Aruru Sai Kumar, Design and Energy Dissipation Analysis of Full-Adder for Low Power Applications Using Reversible Logic Gates, 3rd International Conference on Emerging Frontiers in Electrical and Electronic Technologies (ICEFEET),2023.
[16]. Himanshu;Chaagan Charan," A 16-Byte Asynchronous Gray Code FIFO Memory Using Verilog HDL for Real Time Applications", 2nd International Conference on Device Intelligence, Computing and Communication Technologies (DICCT), 2024.
[17]. Koutaro Inaba;Tomohiro Yoneda;Toshiki Kanamoto;Atsushi Kurokawa;Masashi Imai, Hardware Trojan Insertion and Detection in Asynchronous Circuits,25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2019.
[18]. John Paul Strachan, "Power efficient hardware accelerators for machine learning, combinatorial optimization, and pattern matching applications", International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2020.
[19]. Seungmin Woo;Hyunsoo Lee;Yunjeong Shin;MinSeok Han;Yunjeong Go;Jongbeom Kim;Hyundong Lee;Hyunwoo Kim;Taigon Song,"Reinforcement Learning-Based Optimization of Back-Side Power Delivery Networks in VLSI Design for IR -Drop Reduction" , Design, Automation & Test in Europe Conference & Exhibition (DATE),2024.
[20]. Pei-Yu Lee;Tung-Chieh Chen, "AI-Driven Innovations in IC Designs: From Planning to Implementation", International VLSI Symposium on Technology, Systems and Applications (VLSI TSA), 2024.
[21]. Dawei Li;Seda Ogrenci-Memik;Lawrence Henschen,"On-chip integration of thermoelectric energy harvesting in 3D ICs" IEEE International Symposium on Circuits and Systems (ISCAS), 2015.

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[22]. Pankaj Pathak;Ajay Kumar;Dhiman Mallick," Light-Induced Static and Dynamic Magnetization Modulation in Magnetoelectric Heterostructure for Beyond- MOS Devices",8th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 2024.
[23]. An Chen," Low-power beyond-CMOS devices",12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2014.
[24]. Aishwarya Vaishnavi Gajendrula;Nikhil Deep Gupta," Optoelectronic heterostructure transistor based on perovskite-silicon for neuromorphic computing " IEEE 19th India Council International Conference (INDICON), 2022.