IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.53
Volume 4, Issue 2, August 2024

Implementation of 4-bit Universal Shift Register using Reversible Logic

Yathin[1], Shashank Pai[2], Nishma P Karkera[3], Sudheesha[4], Deepthi Shetty[5]
UG Students, Department of Electronics and Communication Engineering[1- 4]
Senior Assistant Professor, Department of Electronics and Communication Engineering[5]
,Mangalore Institute of Technology & Engineering, Mangalore, India

Abstract*: The field of digital logic design is increasingly exploring reversible logic due to its potential in minimizing power dissipation, an essential criterion in low-power applications. This paper presents the design and implementation of a 4-bit universal shift register (USR) using reversible logic gates. The design leverages Fredkin gates, multiplexer (MUX), and D flip-flops to achieve functionality with minimal power consumption. Simulation results demonstrate the efficiency and effectiveness of the proposed design. Reversible logic is essential to low-power digital design and quantum computing because it makes it possible to reconstruct input signals from output signals, which reduces heat generation and information loss. The suggested shift register can be used for hold, parallel load, and left and right shift operations. To implement the functions of the shift register, we used a variety of reversible gates, including the Toffoli and Fredkin gates. When the architecture is contrasted with traditional non-reversible shift registers, it shows notable gains in reduced gate count and power efficiency*

Keywords: Reversible logic, Fredkin gate, universal shift register, multiplexer, D flip-flop, low power design

I. INTRODUCTION

The design and optimization of digital circuits have become a crucial focus in computer engineering, driven by the growing demand for low-power and high- performance computing devices. One approach to addressing this challenge is the use of reversible logic, which has the potential to reduce power consumption and improve the efficiency of digital systems. Reversible logic has gained significant attention due to its theoretical promise of zero power dissipation, which contrasts with traditional irreversible logic circuits where energy is lost in the form of heat. The primary objective of this research is to implement a 4-bit universal shift register using reversible logic gates, focusing on Fredkin gates for constructing key components like multiplexers and D flip-flops.Traditional digital circuits are based on irreversible logic, where bits of information are lost, leading to energy dissipation as heat. In contrast, reversible logic ensures that no information is lost, thereby theoretically achieving zero power dissipation. This property makes reversible logic highly suitable for low-power applications, including quantum computing, low-power VLSI design, and nanotechnology.Universal Shift Registers are versatile components in digital systems capable of performing shift-left, shift-right, parallel load, and hold operations.

II. LITERATURE REVIEW

Anamika et al.; [1]: The paper presents transistor-level implementations of state-of-the-art reversible gates and designs Boolean logic circuits using the SCL180nm library. It introduces a D flip flop and a 4x1 MUX with energy efficiencies of 14% and 94%, respectively, compared to conventional designs. These circuits achieve both area and power efficiency due to the unique input output mapping of reversible logic gates. The limitations include potential challenges in scaling complexity and the need for further real-world validation and exploration of performance trade offs.

Kalavakolanu et al.; [2]: The design and implementation of sequential and combinational circuits using reversible logic gates, developed with Xilinx ISE. The study compares parameters such as delay, power supply, and temperature between reversible and conventional circuits. The findings demonstrate that reversible circuits exhibit reduced heat dissipation due to the absence of internal signal switching. The limitations include the complexity of designing reversible logic circuits and potential challenges in integrating them into existing systems. The study primarily focuses on theoretical and simulated results, necessitating further real-world validation and exploration of scalability and performance trade-offs.

Kumar et al.; [3]: The design and implementation of VLSI circuits using reversible logic gates such as Fredkin, Peres, Feynman, and Toffoli gates. It highlights the advantages of reversible logic, including zero heat dissipation, reduced energy dispersion, and increased speed, making it This paper discusses the design and implementation of VLSI circuit using reversible logic gates such as Fredkin, Peres, Feynman, and Toffoli gates. It highlights the advantages of reversible logic, including zero heat dissipation, reduced energy dispersion, and increased speed, making it suitable for nanotechnology and low-energy CMOS designs. The limitations include the increased hardware complexity and the need for further validation and optimization for practical applications. The study primarily focuses on theoretical benefits without extensive real-world testing.

Chowdhury Kolayet al.; [4]: The paper introduces the SS reversible logic gate, detailing its input output table and the implementation of half adder-subtractor and full adder- subtractor circuits. The study emphasizes the gate's potential for ultra-low power consumption, benefiting technologies like CMOS, bioinformatics, and cryptography. The limitations include the need for extensive validation against existing reversible gates, potential integration challenges in complex systems, and the lack of real-world application testing to confirm theoretical benefits.

Rajput et al.; [5]: The advantages of reversible logic in quantum computing, focusing on reducing power consumption and heat dissipation while increasing speed. It describes various reversible logic gates, including Toffoli, Fredkin, and Feynman gates, and provides a comparative analysis between classical and quantum logic gates across different parameters. The limitations include the need for further real-world validation, potential integration challenges with existing technologies, and the complexity of designing and implementing reversible logic circuits.

Byeon et al.; [6]: The paper "Empowering energy with a cutting-edge reversible logic framework for Universal Shift Registers," presents a novel reversible logic framework aimed at enhancing the energy efficiency of Universal Shift Registers (USRs). The study details the design and optimization process, demonstrating significant reductions in power dissipation and heat generation. This work highlights the importance of reversible logic in developing energy-efficient computing solutions for applications such as digital signal processing and communication system.

Sushma S et al.; [7]: The paper "QCA based Universal Shift Register using 2 to 1 mux and D flip flop," explore the design of a Universal Shift Register (USR) using Quantum- dot Cellular Automata (QCA) technology. The proposed design employs a 2-to-1 multiplexer and D flip-flop, emphasizing QCA's advantages in terms of reduced area and power consumption. The study showcases QCA's potential for developing highly compact and energy-efficient digital circuits, which are crucial for future nano-electronics applications.

Chakraborty et al.; [8]: The paper "Design and implementation of high-speed low power multipliers using reversible logic," investigates the use of reversible logic gates to design and implement high speed, low-power multipliers. The study provides a detailed analysis of various reversible logic designs and their impact on the performance of multipliers, showing significant improvements in speed and power consumption. This research highlights reversible logic as a promising approach for creating efficient arithmetic units in modern computing systems.

M. Maity, H et al.; [9]: The paper "Design of quantum cost efficient 4-bit reversible Universal Shift Register," present the design and implementation of a 4-bit Universal Shift Register using reversible logic. The study focuses on minimizing the quantum cost, which is a key metric in reversible computing. By optimizing the design, the authors demonstrate significant improvements in efficiency compared to traditional approaches. The research highlights the potential of reversible logic in creating energy-efficient and high-performance digital circuits

Soeken, M et al.;[10]: The paper "Fredkin-enabled transformation-based reversible logic synthesis," introduce a synthesis method for reversible logic circuits utilizing Fredkin gates. The study focuses on a transformation-based approach that leverages the Fredkin gate to enhance the synthesis process. The authors demonstrate how this method can improve the efficiency of reversible logic designs, offering potential advantages in terms of reduced gate count and improved performance for applications in reversible and quantum computing.

IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.53
Volume 4, Issue 2, August 2024

III. IMPLEMENTATION OF REVERSIBLE LOGIC GATES

Fredkin gate, a crucial component in the design, is discussed in detail. The Fredkin gate can act as a universal gate, allowing the construction of multiplexers and D flip- flops used in the USR.

A. Description of the Fredkin Gate:

The Fredkin gate is a 3x3 reversible gate with the following mapping: (A, B, C) → (A, A'B + AC, A'B + AC'). This functionality allows it to act as a controlled swap gate, where the first input A controls whether the second and third inputs B and C are swapped or passed through unchanged.

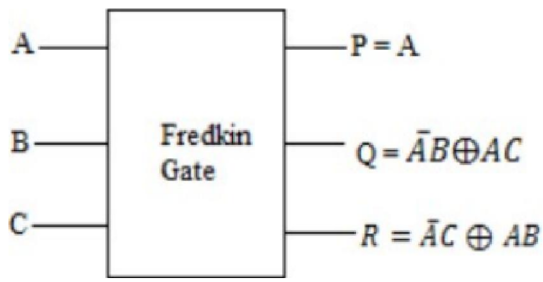

Fig. 1. Fredkin Gate

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

TABLE 1: Truth Table

B. Implementation of Fredkin Gate in Designing Multiplexers and D Flip-Flops

The Fredkin gate's ability to perform controlled swaps makes it ideal for implementing multiplexers. By configuring the inputs appropriately, a Fredkin gate can select between two data inputs based on a control signal. Similarly, D flip-flops can be constructed using a combination of Fredkin gates to ensure data is correctly latched based on the clock signal.

C. Advantages of Using Fredkin Gates in Reversible Logic Circuits:

Fredkin gates provide a balanced trade-off between gate count and functionality, making them suitable for complex logic circuits. Their conservative nature ensures no information loss, aligning with the principles of reversible computation.

IV. PROPOSED REVERSIBLE CIRCUIT DESIGN

A 4-bit USR can perform left shift, right shift, parallel load, and hold operations. The design involves four stages, each consisting of a multiplexer and a D flip-flop, with control signals dictating the operation mode.

A. Design of the Reversible Multiplexer Using Fredkin Gates

The multiplexer, constructed using Fredkin gates, selects between inputs based on control signals. Each Fredkin gate can implement a 2-to-1 multiplexer by configuring its inputs and control signals appropriately.

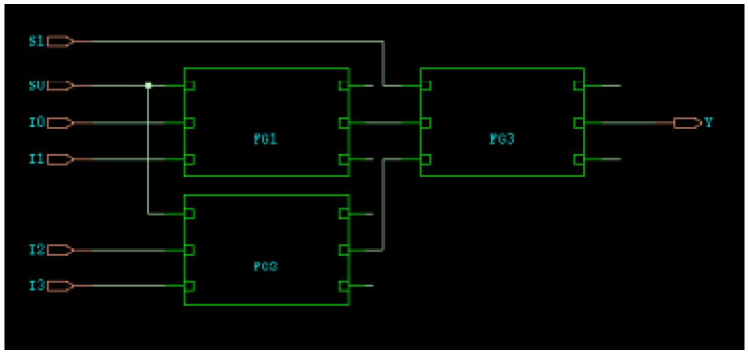

Fig. 2. Mux using Fredkin Gate

B. Design of the Reversible D Flip-Flop Using Fredkin Gates:

The D flip-flop design leverages Fredkin gates to latch the input data based on the clock signal. The reversible nature of the Fredkin gate ensures that the flip-flop operates with minimal power dissipation.

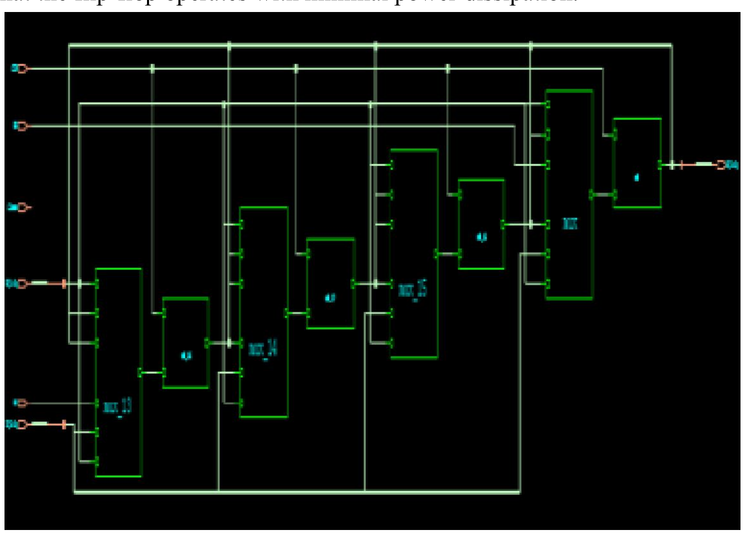

Fig. 3. D flip flop using Fredkin Gate

C. Integration of Components into the USR:

The USR integrates the multiplexers and D flip-flops in a sequential manner, controlled by mode selection inputs to perform various operations. The data path is designed to allow seamless shifting and loading of data.

IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.53
Volume 4, Issue 2, August 2024

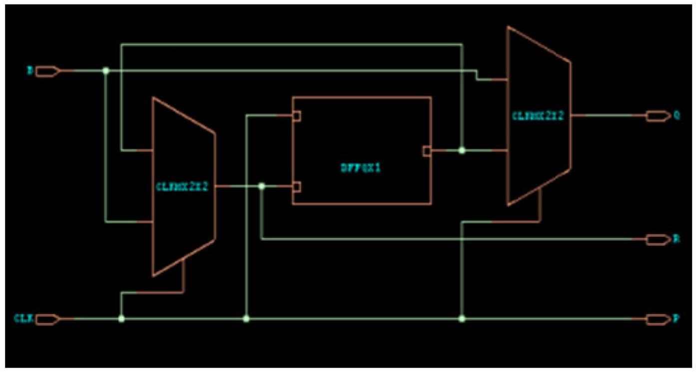

Fig. 4. Reversible Universal Shift Register

V. RESULTS AND DISCUSSION

The proposed reversible 4-bit universal shift register (USR) was successfully designed and simulated, yielding promising results in terms of power efficiency and functionality. The gate-level simulation confirmed that the USR performed all intended operations shift left, shift right, parallel load, and hold correctly and efficiently. The gate report indicated a balanced gate count, showcasing the efficiency of the Fredkin gate in constructing the necessary multiplexers and D flip-flops

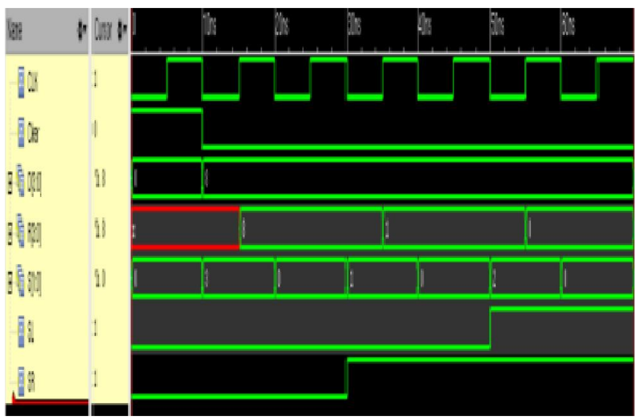

Fig. 5. Output of Reversible USR

Furthermore, the cell report highlighted the optimized use of logic cells, demonstrating that the reversible logic approach did not excessively inflate the circuit's complexity compared to traditional designs. The switching power analysis revealed a significant reduction in power dissipation, affirming the theoretical advantages of reversible logic. The measured switching power was notably lower than that of conventional irreversible USRs, validating the effectiveness of the Fredkin gate in minimizing energy loss

TABLE 2: Comparison Table

Report	Existing Model	Proposed Model
Cell Area	157.435	148.52
Gate	22	16
Switching Power	88.2	78.1

These positive results underscore the potential of reversible logic in developing low-power digital circuits. The 4-bit USR's efficient performance and reduced power consumption make it a viable candidate for applications requiring energy-efficient data processing and storage. Overall, the findings reinforce the feasibility of using reversible logic for complex digital designs, paving the way for further advancements in low-power computing technologies.

VI. CONCLUSION

In this research paper, we presented the design and implementation of a 4-bit universal shift register (USR) using reversible logic gates, specifically focusing on the Fredkin gate. The study aimed to explore the potential of reversible logic in reducing power dissipation, a critical factor in low-power digital circuit design. Our proposed design successfully integrated reversible multiplexers and D flip-flops to form a fully functional 4-bit USR capable of performing shift left, shift right, parallel load, and hold operations. The simulation results validated the correct operation of the USR, confirming the effectiveness of the Fredkin gate in constructing these key components. The analysis of the gate report, cell report, and switching power demonstrated that the reversible USR not only achieved the desired functionality but also exhibited significant power savings compared to conventional irreversible designs. The reduced power dissipation aligns with the theoretical benefits of reversible logic, making it a promising approach for energy-efficient digital systems. The findings of this research highlight the viability of reversible logic in practical applications, paving the way for further exploration and development in this field. Future work can extend this approach to more complex digital systems, potentially incorporating other reversible gates and optimizing the design for higher performance and lower power consumption. In conclusion, the successful implementation of the 4-bit USR using reversible logic marks a significant step towards the realization of low power digital circuits, offering a promising solution for future advancements in low-power and energy-efficient computing technologies.

VII. FUTURE SCOPE

Reversible logic is used to create a 4-bit universal shift register, which has great potential for future developments in a number of important fields. Reversible logic circuits are perfect for quantum applications, but as quantum computing advances, their intrinsic capacity to lower error rates and information loss will make them even more crucial. Furthermore, the demand for power-efficient technologies is being driven by the focus on energy-efficient computing, and reversible logic circuits provide a workable way to construct ultra-low-power processors and memory devices. The concepts and methods exhibited in this 4-bit shift register can be extended to more intricate systems, such digital signal processors, control units, arithmetic and logic units, and so on. This makes it easier to create integrated circuits that are more effective. The integration of reversible logic with emerging technologies like superconducting electronics, spintronics, and nanotechnology could lead to innovative hybrid systems that leverage the strengths of each technology. Furthermore, this research can serve as an educational tool, providing a foundation for teaching concepts related to low-power design, quantum computing, and digital circuit design. Finally, the commercial and industrial sectors stand to benefit from reversible logic based designs, particularly in areas where energy efficiency and heat management are paramount, such as consumer electronics, automotive systems, telecommunications, and data centers.

VIII. ACKNOWLEDGMENT

The authors would like to express their sincere gratitude to MITE, particularly the Department of Electronics and Communication Engineering (ECE), for providing the necessary resources and support to conduct this research. Special thanks are extended to our guide, Mrs. Deepthi Shetty, Senior Assistant Professor, for her invaluable guidance, insightful feedback, and continuous encouragement throughout the course of this project. We also wish to acknowledge project coordinators, for their assistance and coordination in facilitating this research. Lastly, we are grateful to our peers and colleagues for their constructive discussions and support.

REFERENCES

[1]. Anamika and Bhardwaj, R. (2018) 'Reversible logic gates and its performances', 2018 2nd International Conference on Inventive Systems and Control (ICISC)

IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.53
Volume 4, Issue 2, August 2024

[2]. Kalavakolanu, S.R. (2018) 'Implementation of reversible logic at Gate Level', 2018 2nd International Conference on Inventive Systems and Control (ICISC)

[3]. Kumar, U., Sahu, L. and Sharma, U. (2016) 'Performance evaluation of Reversible Logic Gates', 2016

[4]. International Conference on ICT in Business Industry & Government (ICTBIG)

[5]. Chowdhury Kolay, S., Chattopadhyay, S. and Bandyopadhyay, M. (2020) 'Design and development of SS Reversible Logic Gate and its application as Adder & Subtractor', 2020 International Conference on Inventive Computation Technologies (ICICT)

[6]. Rajput, A.K., Chouhan, S. and Pattanaik, M. (2019) 'Low power boolean logic circuits using reversible logic gates', 2019 International Conference on Advances in Computing, Communication and Control(ICAC3)

[7]. Byeon, H. (2023) 'Empowering energy with a cutting-edge reversible logic framework for Universal Shift Registers', Results in Control and Optimization, 13,

[8]. Sushma, S. et al. (2021) 'QCA based Universal Shift Register using 2 to 1 mux and D flip-flop', 2021 International Conference on Advances in Computing, Communication, and Control (ICAC3)

[9]. Chakraborty, K. (2016) 'Design and implementation of high-speed low power multipliers using reversible logic', International journal of Emerging Trends in Science and Technology

[10]. Maity, H. et al. (2017) 'Design of quantum cost efficient 4-bit reversible Universal Shift Register', 2017 Devices doi:10.1109/devic.2017.8073903. for Integrated Circuit (DevIC).

[11]. Soeken, M. and Chattopadhyay, A. (2015) 'Fredkin enabled transformation-based reversible logic synthesis', 2015 IEEE International Symposium on Multiple-Valued Logic.