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Optimized Hybrid Flip-Flop with Conditional Boosting for Near-Threshold Voltage Applications

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Abstract: *In addition to space and speed, the issue of power consumption is considered to be one of the challenges of modern VLSI design. The flip-flop forms part of digital systems. Four different flip-flop topologies in sub-threshold operation will be compared and contrasted, namely IP-DCO, MHLFF, CPSFF, and CPFF. Such topologies include conditional and pulse-triggered. Recently, it has become possible to apply applications with very low power consumption thanks to sub threshold technology. The advantage of this technology is that it makes the flip-flops consume less power. A subthreshold circuit consumes less power as compared to strong inversion circuit when the frequency is of the same frequency. Tanner uses the 18nm technology in cmos, design. The flip-flops are also tested at a power supply voltage of 1 V at various angles and the properties of the flip-flops such as average power, product of power delay, and power delay are measured.*

Keywords: Low-power, digital, design, efficiency, flip-flop, CMOS, energy-delay product, PVT variations

I. INTRODUCTION

The clock frequency and timing standards have to be increased and strained so as to satisfy the requirement that electronic systems run at a high pace [1]. These systems have been consuming high power in order to satisfy the timing requirements needed, by means of high-speed circuits. The use of mobile electronic devices in the contemporary life has also enhanced the demand of energy- efficient computation [2, 3]. It might be necessary to compromise on speed performance, but low power design techniques including voltage scaling to cut switching power and conditional operation to eliminate unnecessary power can be applied to overcome energy constraints [4, 5]. In high-performance mobile applications, it is a normal behavior to trade-off certain power to achieve a faster processing time. Flip-flops and latches control state transitions and synchronised data flow in synchronised digital integrated systems. The timing-critical signal paths include flip-flops which usually dictate the maximum operating frequencies, and thus the high-speed design of flip-flops is essential [8]. Low-power flip-flop design has become increasingly significant over the last few years since it has been seen that a given processor can use millions of flip-flops [9], and their total power usage can be reduced to 20-40 percent of overall power [9], [10], [11]. Therefore, one of the most important issues in the design of mobile electronic systems with high speeds is how to reduce power consumption and delay in the use of flip-flops and latches, which is not easily done at the same time. It can be used in synchronous digital integrated circuits to offer moderate power and data-to-output (DQ) delay of the transmission- gate flip-flop (TGFF) through the master-slave topology [12] (FIGURE 1). The other benefit that can be realized through the reliability of TGFF to work at near-threshold voltage (NTV) is power savings through voltage scaling. Pulse-based techniques in TGFF can minimize the DQ latency since processing of the input data and their capture in the master and the slave stages are separated, respectively [13], [14], [15]. An example of such implementation is the transmission-gate pulsed latch (TGPL) [13], which is a combination of a pulse generator and a single latching step. Lowering of the DQ latency is brought about by removing the master stage in TGFF as well as transferring the input data straight to the output at the end of the tiny

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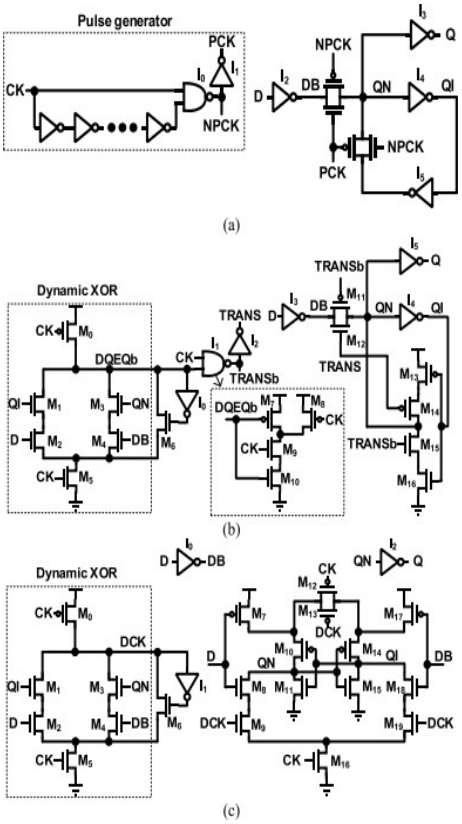
pulse caused by the clock edge. Despite the rapid operation, TGPL can consume a significant amount of power due to the circuit overhead to produce the short pulse. Moreover, the uncertainty of pulse width as an effect of process variables may cause undesirable operation, especially in the NTV zone. Though the new circuit methods had been used to assist pulse generation in certain applications, the continued use of internally delayed local clocks in pulsed operations continues to lead to increased overall power consumption than in TGFF [14], [15]. Another way of making timing components faster is through the use of the sense-amplifier- based flip-flop (SAFF) technique [17]. The flip-flop may be used in the first stage to produce high-speed operation by use of a symmetric latch and a differential precharged circuit respectively, providing fast sampling and input data capture at the triggering clock edge. A change in the architecture of the latching stage can further enhance the power and speed, yet could also introduce some unwanted signal fighting that reduces latency and power consumption [18]. Further, these flip-flops are susceptible to the growing variability in the NTV region because they operate with a weak shorting to ensure that they operate in a static. Although the problem can be eliminated through surveillance of the arrival of precharged nodes, enormous power and latency overheads exist. The presented work presents conditional bridging flip-flops (CBFFs) which can be implemented on the basis of sensing amplifiers and can possibly enhance the speed and reduce the power consumption. The shorting device issue mentioned above is also eradicated with the proposed conditional bridging method, which does not come with any overheads of power or speed. A single-ended version (CBFF-S) of the flip-flop is proposed to reduce power consumption whereas a differential version (CBFF-D) is proposed to reduce latency.

Besides being fast, low power and contention free, the CBFFs can also be reliable in the NTV zone.

II. EXISTING METHOD

A. Sense-Amplifier-Based Flip-Flop



Conditional Bridging

Fig:1. A) TGPL [13], (B) STPL [14], and (C) DCPL [15] Are Pulsed Latch-Based Ffs.

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An alternative approach that is proposed to resolve the issues with the reducing device (M4) in the traditional SAFFs is a conditional bridging approach that is more power-efficient. Driven by the thought that the shorting device is only to be activated when D is no longer the same once it has been gathered by Q, the aim is to remove any redundant transition in any way relevant. In other cases, it is wiser to deactivate the equipment to avoid the disadvantages of having an ineffective device, and also to avoid unnecessary release of internal node (X or Y) on the other branch. Figure depicts the conditional bridging circuit in the SA stage with the shorting circuit driven by the output of the circuit (CBG). The proposed conditional bridge network measures the values of D, DB, SB and RB to activate M4 when CK=1 only when D varies and is not equal to Q. The pre-charge of SB and RB when CK is low, so that, in activating M13, M17, and perhaps one of M12 and M16 at the same time, maintenance of CBG low is not dependent on the value of D. SB or RB discharge at the ascending side of the clock depending on the value of D. Under the assumption that SB is discharged, it is possible to maintain CBG low at D=RB=1 at M16 -M17. When D drops low, CBG shoots high through M14 and M15 and this allows activation of M4 to provide a DC path to the ground and ensure the provision of the statical functionality.

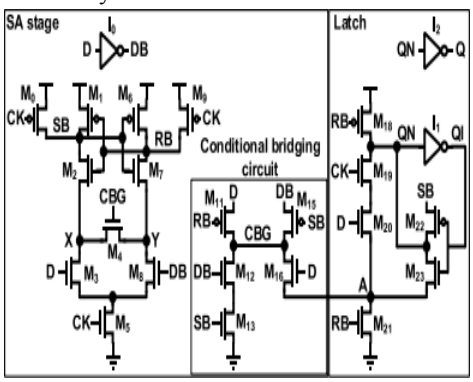

Fig:2. A Flip-Flop That Just Has One Side Open Is Another Option.

Structure And Operation

Two versions of the conditional-bridging flip-flop (CBFF) are proposed, both applying the conditional bridging mechanism, which has already been mentioned. The single-ended version (CBFF-S) consists of a sensing amplifier stage (M0-M9 and I0), aconditional bridging circuit (M11-M16) and a single-ended latch stage (M18- M23, I1, and I2) as depicted in Figure 5. The conditional bridging circuit is modified to bring down the total number of transistors in the flip-flop. To be more precise, D drives sources in M11 and the sources in DB, but the sources in M15 are driven through DB. Figure 5 shows the combination of M21 and M17 that were manipulated by RB in Figure 4. The irregularity- and contention-free single- ended latch, driven by the SA stage with no inversion (as shown on the right-hand side of Fig.), enables the latching stage to be designed in terms of the power consumption and number of device count. M18 activates the pull-up of QN only after the rising clock edge, as opposed to M19-M21 which only activates the pull-down of QN. The driving of M20 by D is done to eliminate the QN glitches due to the high value (precharged) of RB at the start of the high frequency of the clock. To bring down QN non- contentionally, SB is used to drive the source of M22. The source of M23 is also connected to node A in such a way that pulling up QN does not create a conflict. The absence of a pulsed operation is what makes the latching stage of the CBFF-S in Fig. different compared to the conventional pulsed latches [13], [14], [15].

CBFF-S should be used when it is important to you that it is reliably functioning, has low latency, and low power consumption. A possible method of preventing unwanted CBG transitions is to regulate the point at which the shorting device (M4) is used by the conditional bridging logic. The conditional bridging circuit will consume the least amount of power at low switching activity as it will switch when D changes when D is grabbed by Q when CK=1. Circuit enables miniaturisation through lowering the power and avoiding shorting. CBFF-S only releases the opposing precharge node (X or Y) when D changes, since under low input switching activity seldom does D change. They are regularly charged

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and discharged on a clock cycle by regular SAFFs as aforementioned. Any timing critical impulse (such as SB and RB) might potentially be drawn out sooner by the smallest possible shorting device since the smaller parasitic capacitance of that shorting device. This can be achieved by disabling the shorting device so that the input can be sampled faster by removing the interference between SB-RB signals. RB avoids signal inversion and contention by direct control of the latching process, therefore, reducing clock-to-output (CQ) time. By minimizing congestion in the SA stage, pulling down precharged nodes at low supply voltages is made reliable. CBFF-S latching stage contention-free & conditional-bridging SA stage makes sure that input data is safely collected as the system runs safely in the extremely turbulent NTV zone. The following table is the proposed differential suggested flip-flop commonly referred to as CBFF-D it is possible to refer to figure 13 which displays some two transistors namely M13 and M30 that can be used in the conditional bridging circuit without the third transistor being added due to the symmetric differential structure. On post-latching addition of a few transistors and removal of the output inverter (I2 in Fig.), we can instruct SB and RB to push difference outputs Q, QB. Arrangement CK-powered M24 in parallel with pull-up keepers transistors M22 and M25 accelerates the pull-down of these transistors since they will not strain to pull-down. A design similar to the single-ended type (M22 driven by SB in Fig) can also work well with normal supply voltages, but the addition of a delayed transistor (M24) is required because of reliability issues pointed out by Monte-Carlo simulation in the worst corners. CBFF-D is the same in terms of operation speed and power consumption as its single-ended counterpart. In spite of the slightly greater total power consumption due to the larger load capacitance of CK used to drive the differential latch, CBFF-D also reduces power consumption significantly in low-activity switching situations with its conditional bridging operation. CBFF-D can be faster than CBFF-S because the outputs of the SA the stage in the process of driving Q and QB different latches.

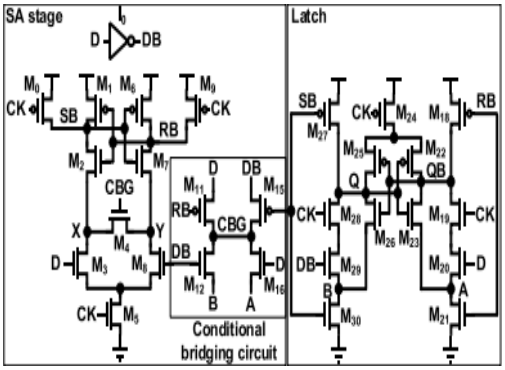

Fig:3. The Suggested Flip-Flop In Its Differential Form.

III. PROPOSED FLIP FLOP DESIGNS

A. CONDITIONAL BOOSTING AMPLIFIER

A conditional boosting flip-flop applies conditional boosting in order to enhance its performance in input data collection. It is some sort of flip-flop circuit. The logic state of each of the input and output signals defines the boosting operations that this flip-flop performs. To maximise its operation under varying conditions of input data, the conditional boosting flip-flop combines output-dependent presetting ideas and intake-dependent boosting concepts. Such a method reduces the power consumption under normal operation, but enables faster collection of data when required.

Outputs Q and QB to Capacitor terminals N and NB define preset voltages which are output-dependent, as seen in Figure 4(a). This indicates that when Q is low and QB is high, N will be left-hand and NB will be high as illustrated in the left-hand figure in Figure 4(a). Conversely, N will be high and NB will be low where Q is low and QB is high (also identified diagram in Fig. 4(a)). In Figure 4(b) a nMOS transistor is used to tie the noninverting input (D) to NB and to input-dependent boosting and another nMOS transistor to input-dependent boosting is used to tie the inverting input (DB) to N. Capacitor presetting could happen as observed on the left side of Figure 4(a) in case low data are stored in the flip-flop. In this case, with a large input in the left hand side of Figure 4(b) above, NB pulls to ground and therefore N is propelled to -VDD through capacitive coupling. Conversely, a low input, which is indicated by the bottom left

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schematic of Figure 4(b)), would usually connect N to ground. But since to the setting of the node the node would be in VSS, practically no change of voltages would be developed at NB, so it would not be boosted. In the other scenario, as depicted in the right hand diagram of Figure 4(a) capacitor presetting is possible when high data is stored in the flip-flop, then a low input causes N to be drawn to the ground that drives NB to be drawn towards -VDD by capacitive coupling as shown in the bottom right-hand circuit of Figure 4(b).

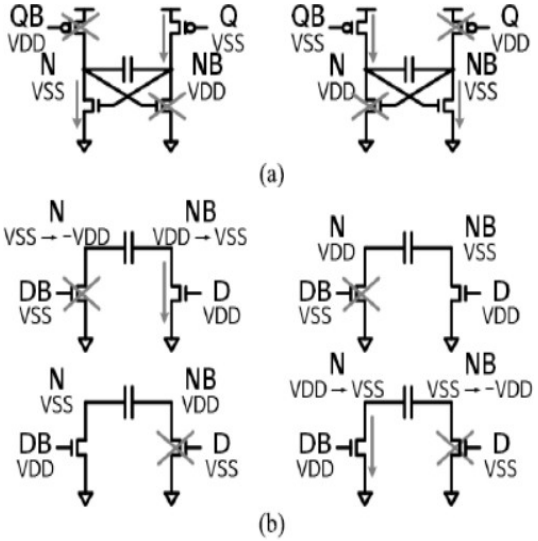

Fig 4: Block Schematics For (A) Data-Dependent Presetting Of Outputs And (B) Data-Dependent Boosting Of Inputs.

	input (D)	output (Q)	boosting node (N)	boosting node (NB)
output-dependent presetting	-	VSS	VSS	VDD
		VDD	VDD	VSS
input-dependent boosting	D=VDD	VSS	VSS → -VDD	VDD → VSS
		VDD	VSS	VDD
	D=VSS	VSS	VDD	VSS
		VDD	VDD → VSS	VSS → -VDD

Fig 5: Findings For Various Q And QB Out Puts

The system consists of an explicit short pulse generator, a symmetric latch and a conditional-boosting differential stage. Figure 6(a) illustrates the conditional-boosting stage of differential. In the case of output-dependent presetting, we shall have MP5, MP6, MP7, and MN8 and MN9. In the case of input dependent boosting we apply MN5, MN6 and MN7 together with the boosting capacitor CBOOT. Figure 6(b) illustrates the symmetric latch that comprises of MP813 as well as MN1015. Figure 6(c) illustrates a special explicit pulse generator that produces a short pulsed signal PS that is applied to the gate of a selected set of transistors within the differential stage. The proposed pulse generator differs with the conventional pulse generators as it lacks a pMOS keeper. This results in both the reduction of the processing time and the power consumed since signal fighting is removed during the pull-down of PSB. When MN1 is introduced together with MP1, it takes the role of the keeper in that it assists in returning PSB to low rather fast and maintaining its logic value at high. In the ascending phase of CLK, MN1, MP1, and I1 discharge PSB rapidly making PS high. Once I 2 and I 3 are passed, PSB is charged by MP 2, leading PS back to low and a short positive pulse at PS whose width depends on the latency of I 2 and I 3. Although, MP2 is not performing any action at the low direction of CLK, MP1 is maintaining PSB high. We have analyzed that, using the same pulse widths and slew rates, lower power of up to 9% can be obtained.

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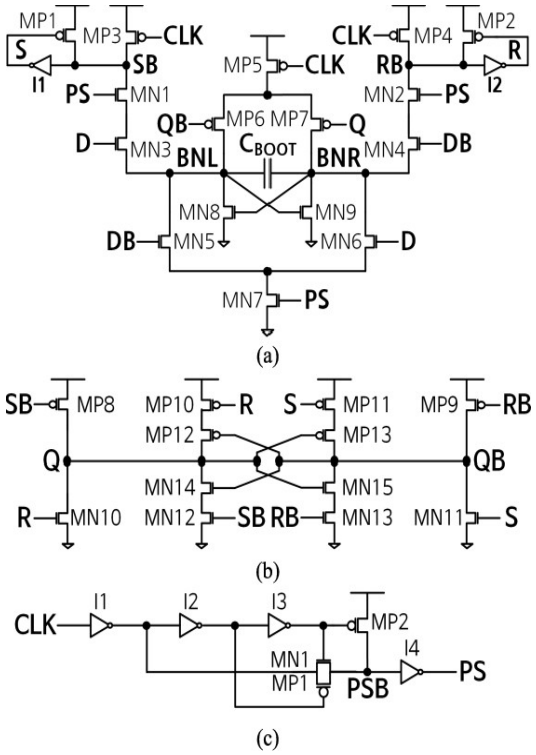

Fig:6. Presented As A Possibilities CBFF. (A) The Threshold For Conditional-Boosting Differentials. (B) Latch Is Symmetrical. (C) A Generator Of Explicit Short Pulses.

Other power consumption problems as well as delay which depends on parasitic capacitances can be avoided by eliminating them. The figure shows the difference in the delay time of flip-flops. According to the graph, it is clear that MHLFF has lower latency as compared to other flip- flops. Figure shows the average electric consumption of a flip-flop. CPSFF has the lowest average power usage whereas MHLFF has the highest. Compares the power delay product. The variation in the average power of the various types of flip-flops. CPSFF is of lesser value compared to other flip flops. Of these four flip-flops, CPSFF is the most effective.

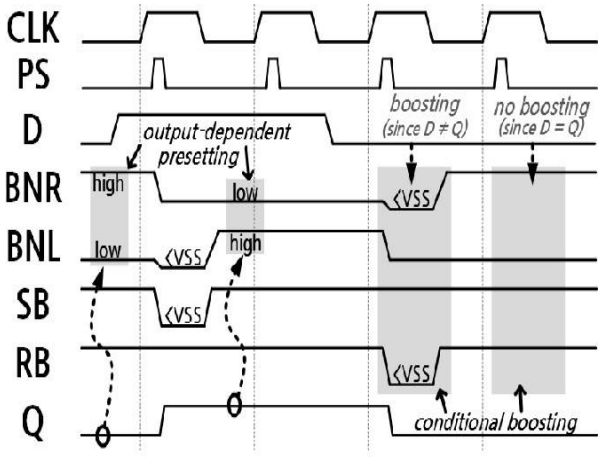

Fig: 7. The Suggested Flip-Flop's Timing Diagram.

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IV. RESULTS

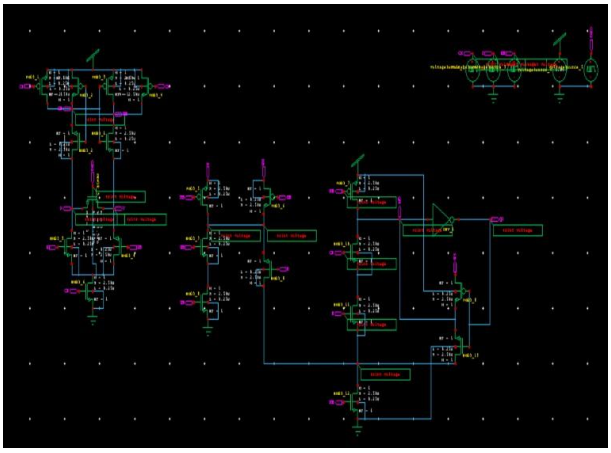

Fig:8. Existing schematic Single-ended version flip-flop

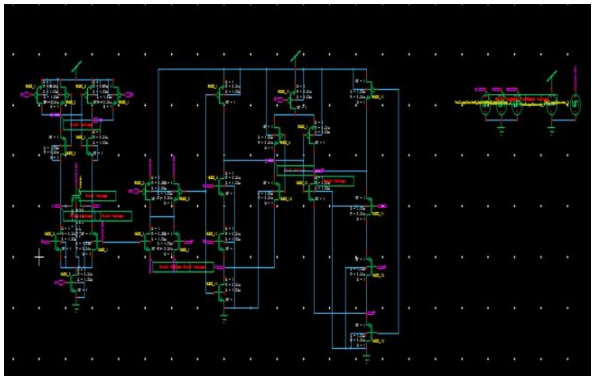

Fig:9. Existing Schematic Differential Version Flip-Flop.

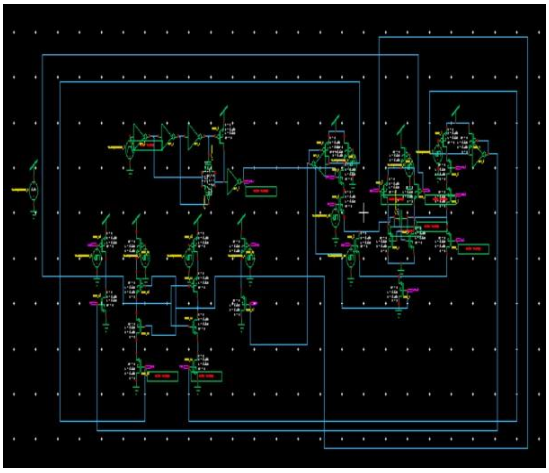

Fig:10. Schematic of Proposed conditional Boosting Flipflop.

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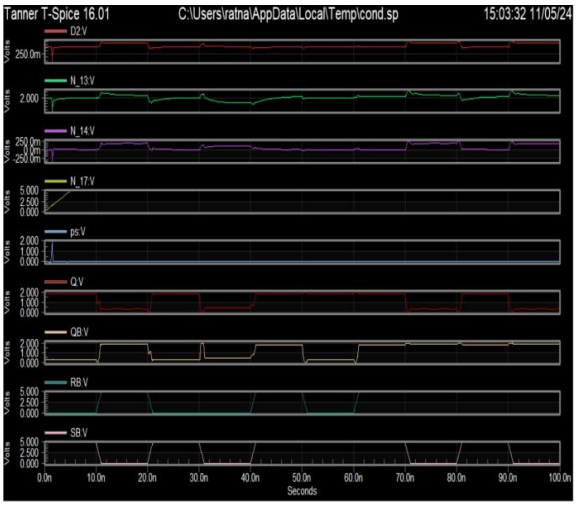

Fig 11: Amplified Output Waveform.

The system's power usage trends were inconsistent, averaging 8.1984W. Power consumption ranged from 0.00000W at the lowest to 1.7371W at the maximum throughout this period. The system stabilized at a reported setup time of 0.03 seconds, which is quite similar to the DC operating point. Further research revealed that a transient phase lasting 0.39 seconds signified the system's settling into a steady state.

Performance Comparison:

Parameters	Existing method	Proposed method
Min Input Power	4.736 W	0.0000 W
Max Input power	7.6304 W	1.7371 W
Avg Input power	6.2587 W	8.1984 W
Delay	0.95 sec	0.82 sec

V. CONCLUSION

The work proposes reliable, high performance and low power flip-flops that are founded on sense amplifiers. The shorting device is activated adaptively through the proposed conditional bridging to guarantee that there are no redundant transitions leading to the correct operation of the shorting component. Consequently, the parasitic capacitance of the effective capacitance of the signal pathways that are timing-sensitive can be minimized by minimizing the size of the shorting device. The benefit of driving the locking step directly without glitches and conflict is that it saves power and delay significantly. The single ended version of the proposed flip-flop uses a redesigned latching stage to optimise space and power consumption. It is also presented in the form of the differential version that involves a differential latching step; this is to maximise the performance and enable the differential operation. The suggested flip-flops are also in a position to operate under the NTV area, in addition to being capable of operating with improved power and latency performance. A performance study by using an 18nm CMOS technology of the proposed flip-flops showed promising results and the suggested flip- flops could be applicable in low power, high speed digital work. A suggestion has been made to an innovative constrained bandgap filter (CBFF) with aggressive voltage scaling to the region near a threshold voltage with minimal performance degradation. Using a boost body driven scheme, a pulse trigger FF design is provided in this project which is suitable in the case of low power usage. A concept of a multibit flip-flop with a conditional boosting flip-flop is introduced at last, and the power area and latency could be effectively improved.

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