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Specific Investigations Concerning the Improveable Multiplier Architecture of High-Speed and Area-Efficient Adders

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Abstract: *Over the past few decades, the growth of portable devices such as laptops, mobile phone and personal digital assistant has resulted in increasing demand for complex functionality with effective computation. The present day technology is known for digital systems with very high computing capabilities. The demand for high speed, low power integrated circuits for portable devices has become crucial. The never ending growing complexities of integrated circuit for future devices pose a challenging task for integrated circuit designer. Cost effective integrated circuits requires the design meeting out the challenging task to optimize power, area with high performance. Hence this research focuses on the optimization of area, power and speed of Arithmetic circuits, Very Large Scale Integrated circuits (VLSI) are widely used in Arithmetic circuits, Digital Signal Processing (DSP), Image and Video Processing applications*

Keywords: integrated circuits

I. INTRODUCTION

A Binary Common Sub expression Elimination (BCSE) algorithm is utilized in the constant multiplier architecture with effective adders to ensure reduction in power utilized and enhancing the area delay product. The multiplier is the major block in any application like image, advanced Digital signal processing and multi standard wireless communication and so on. The low power utilization, has led to its use in various applications. In the past decades, the constant multiplier architecture had a number of adders and shifters, and so the framework required high power and furthermore the deferral was presented. The multiplier was designed to diminish the number of adders and shifters so the 2 bit and 3 bit BCSE algorithm is used in constant multiplier architecture. The constant multiplier architecture utilizes the Ripple Carry Adder (RCA) and Carry Select Adder (CSA), so the adder steps and the equipment cost is expanded. To keep up a separation from these issues, the 2 bit and 3 bit BCSE algorithm utilizes an efficient adder like RCA with NAND logic and modified CSA This modified BCSE algorithm based constant multiplier decreases the power utilization and enhanced the area delay product proficiently.

II. LITERATURE REVIEW

Adders are the fundamental units commonly used for arithmetic operation in any digital computer. They serve as the basic building block for all arithmetic operations. Implementation of any arithmetic operation involves a binary adder structure which becomes a very critical hardware unit. Since 1950's many binary adders have been proposed for increase in speed, reduce the area and power consumption.

Margala (2008) has designed a low voltage full adder cell for an efficient arithmetic circuit. The sum and carry generated by the full adder cell was designed to meet out low power consumption and to reduce the critical path delay. The full adder cell uses only multiplexer unit to produce the sum and carry output. The designed structure is compared with the conventional half adder based full adder cell.

Chiraz Khedhiri et al. (2012) have proposed a 16 transistor one bit ALU (Arithmetic Logic Unit) that performs eight different two control signals. The output of the logic functions is design logic unit cell which outputs their

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complemented logic function perations with d with a single ns. Hence this technique requires fewer transistors compared to the conventional CMOS logic design.

Panda et al. (2018) have presented a detailed analysis of full adder cells with different transistor level and compared their performance in terms of PDP.

Chang et al. (2005) have designed a 26 transistor modified low power XOR-XNOR logic cells. The disadvantage full adder with e of using this logic is that it causes a huge delay due to logic transition which, however can be reduced through an increase in additional transistor in the full adder cell.But this adder has the disadvantage in terms of area overhead consumption.

Adarsh Kumar Agrawal et al. (2009) have propose the full adder based on static C OS inverter using the mixed gate diffusion input technique. Improvement in the performance over the conventional full adderchain has been done through the GDI full adder chain follow d by inverters.The full adder is optimized in terms of propagation delay, static and dynamic power dissipation by changing the full adders between the inverters. The design steps were carried out by .18µm CMOS technology for the evaluation of the delay and power consumption.

Morgenshtein et al. (2000) have proposed a Shan adder for overcoming the problem of area overhead. It uses on based GDI smaller area as it uses the MUX based design without the requirement of any pre computing circuit for the design of the adder. Hence the optimized adder has been designed using MUX based circuit to reduce the area and power consumption

III. PROPOSED TECHNIQUE

This section, depicts the use of BCSE algorithm in a constant multiplier architecture with modified adder for a reduction in power utilized and for enhanced the area delay product and power delay product is discussed. The adders in this approach are decided by the number of input bits n for a n bit BCSE algorithm. The adder required for the generation of the partial product is 2 n-1 -1 which is obtained from total of 2n – (n+1) common sub expression. The critical path for the adder steps can be obtained by non zero element present in the coefficient. To illustrate these algorithm a 16 bit input (Y) and a 16 bit coefficient (K) are considered. The least favourable conditions occurs for the coefficient of all non zero value 16'HFFFF. The coefficient K value ranges from 0 to 1. Shift and add based multiplication operate between input (Y) with the nonzero coefficient 16'HFFFF values can be written as

$$Y*K = Y/2 + Y/2^2 + Y/2^3 + Y/2^4 + Y/2^5 + Y/2^6 + Y/2^7 + Y/2^8$$
$$Y/2^9 + Y/2^{10} + Y/2^{11} + Y/2^{12} + Y/2^{13} + Y/2^{14} + Y/2^{15} + Y/2^{16} \quad (1)$$

The equation (1) can be reduced by choosing the length of BCSE algorithm.

2 Bit BCSE Algorithm

The partialproduct generation unit is also called ashift and addunit. Input Y is considered to be a 16 bit binary data. In the partial product unit, BCS technique is focused for the elimination of redundant Computationof coefficients. Forexample 2 bit binary representationcan form fourdifferent combinations as follows

00 = which is treated as 0

$$01 = Y/2 \quad (2)$$
$$10 = Y \quad (3)$$
$$11 = Y + Y/2 - X \quad (4)$$

The equation (4) requires one adder and one right shifter. Substituting equations (4) in (1).

$$Y*K = X/2 + X/2^3 + X/2^2 + X/2^1 + X/2^9 + X/2^{11} + X/2^{13} + X/2^{15} \quad (5)$$

For the above equation the hardware can be realized by using seven adders and eight partial product generators to produce a constant multiplication output.

3-Bit BCSE Algorithm

Consider a 3 bit BCSA it requires three adders of 16 bit to generate the partial products. The input Y is grouped as 3 bit patterns, if Y contains

000 = which is treated as 0

010=Y/2 (6)

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001=Y/4 (7)
011=Y/2+Y/4 (8)
100=Y (9)
101=Y+Y/4(10)
110= Y+Y/2 (11)
111= Y+Y/2 +Y/4 (12)

Equations (8), (10), (11) require one adder each and equation (12) requires 2 adders hencefor a total of 5 adders are required in the conventional method. Identical patterns are eliminated using CSE algorithm.Equation (8) can be modified as

011=2(Y+Y/2)=2 (110)=2C (13)

C is Y+Y/2

111=Y+2C (14)

101 be A= Y+Y/4

Equations (10), (13) and (14) show the requirement of number of adder requires for generation of the partial product will be 3 in case of 3 bit BCS.

Ripple Carry Adder (RCA)

The ripple carry adder is a logic circuit designed using the group of full adders. The RCA adder likewise is used for adding the N-bit numbers. In the proposed method, for the addition of the partial product term, the proposed 2-bit BCSE constant multiplier uses the buffer based full adder. The buffer based full adder helps in reduction of delay and a power delay product of the constant multiplier.

The proposed buffer based full adder shown in Figure 1, incorporates an incrementer unit with two data selector units and XOR gates. The two data sources input B and C applied to the XOR gate. In the XOR gate operation the high or low value of two information sources B and C lead to the implication of B = 1 and C = 1 or B = 0 and C = 0, and the output will be Low. This output drives the adder to skip the incrementer unit and the entire output will be the estimation of A input for sum and the carry output is the estimation of B input. On the off chance that if any one of the input information is low, that implies B=0 and C=1 or B =1 and C = 0 the output of the XOR will be 1. This output of XOR makes buffer to get engage and the information will be allowed to increment which produce the sum and carry output.

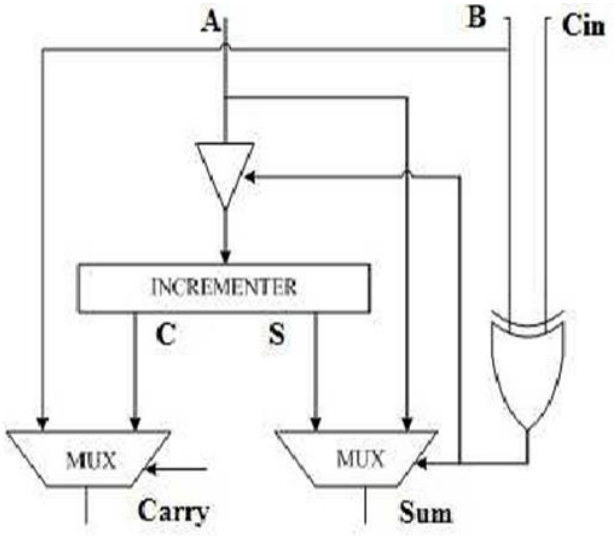

Figure 1 Schematic of Proposed buffer based full adder

The select line for the multiplexer is the output of XOR operation. The delay of the circuit is reduced once the XOR gate, select line for the buffer is enabled. When the enable and select line is 0 value of A is directed to output only the part of the logic utilized leading to the occurrence of a delay in reduction. Thus the buffer based full adder is utilized for diminishing the delay and the Power Delay Product.

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NAND Logic Based Ripple Carry Adder Structure

The buffer based full adder structure is implemented using only NAND gates. The AND, OR and NOT gates in the design are replaced by the NAND gates. AND, OR, NOT gate requires 2, 3, 1 NAND gates respectively. The worst case delay can be calculated by counting the number of NAND gates in the critical path. The area utilization can be calculated using the number of NAND gates used in the full adder cells. The structure shown in Figure 2 is implemented by using only NAND logic. While converting from the logic level to the NAND level implementation redundant NOT structures are eliminated. Thus the structure becomes efficient in the case of delay and power delay product.

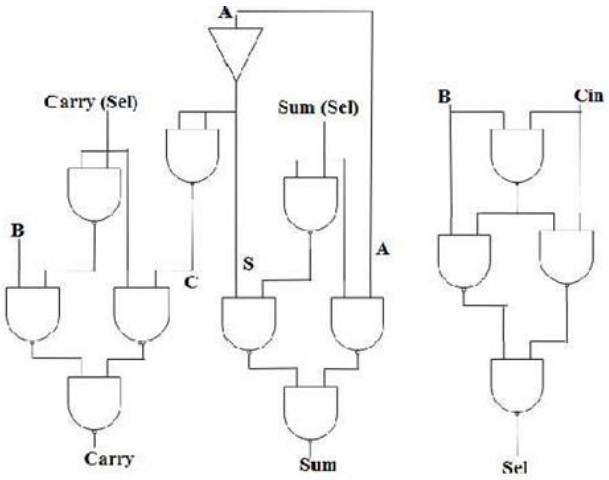

Figure 2 Schematic of Proposed buffer based NAND full adder

Carry Select Adder (CSA)

The carry select adder consists of a block of ripple carry adders and the multiplexers. Therefore carry select adder requires a high hardware space compared to the other adder structures as shown in the Figure 3.7. The main advantage of the CSA is that the addition operation is carried out simultaneously as the assumption of the carry input as zero for one set of ripple carry adder and carry input as one for another set of ripple carry adder.

The input carry is assumed to be the select line for all the multiplexers. The CSA architecture has a fast operation as it assumes the condition for Carry in (Cin) as 1 and 0 (predefined) that compute the sum output faster. This architecture utilizes hardware space. both the two RCA sections, so it requires the high. The constant multiplier utilizes the modified CSA for the expansion operation for overcoming the problem.

Proposed Carry Select Adder

The modified CSA obtained helps reduction in space requirement leading to delay. The proposed CSA uses half adder, multiplexer (MUX) and the NOT gates. To start with two inputs A (0) and B (0) are applied to the half adder (HA). The generated carry from the half adder is fed as input carry to the full adder and select line for the multiplexer. The output of each full adder is fed to the incremental unit. incremental unit is fed as input to the 2 to 1 multiplexer. The output of In the output segment, the two outputs are obtained from the half adder, one is the S(0) and another one is the carry output (Cout). At the same time, the full adder additionally created the two outputs, in that place one NOT gate is associated with the full adder output. These two outputs (i.e., NOT gate and full adder) are passed on to the multiplexer. In the modified CSA, the lower part of the adder structure is replaced by the incremental unit and multiplexer. Because of this reason, little delay overhead occurs in modified carry select adder architecture but the there is reduction in the area.

IV. RESULTS AND DISCUSSION

The proposed 2-bit and 3-bit BCSE based constant multiplier produces better and effective delay reduction using the buffer based full adder structure and a reduction in area outcome is achieved by using Proposed CSA architecture. The CSA in the current strategy comprise two adder areas, enabling expansion of the adder steps because of this reason, the

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space utilization and power utilization is high in the constant multiplier. The proposed 2 bit and 3 bit BCSE based constant multiplier incorporates the proposed CSA structure. For keeping away from intricacy the entire partial product unit in the multiplier architecture utilizes the buffer based full adder and adders used in each steps of multiplier use buffer based RCA structure. The 2 bit and 3 bit constant multiplier using RCA produces better results in terms of delay and power delay product.

Table 1 Comparisons of 2 Bit BCSE Constant Multiplier Area, Power, Delay and PDP using RCA

S. No.	Methods	2-bit BCSE constant multiplier			
		Area μm^2	Power µw	Delay µsec	PDP µw- µsec
1	RCA Amelifard *et al.* (2005)	4964	297.11	15.25	4530.92
2	RCA Dayananda Rajkumar *etal.*(2016)	4876	293.32	15.19	4455.53
3	Proposed RCA with buffer	6126	312.06	14.12	4406.28
4	RCAN AND Mano(2017)	4983	304.20	14.92	4538.66
5	Proposed RCA NAND with buffer	6448	316.04	13.75	4345.55

Table 1, shows the contrast between area, power, delay and PDP of 2 bit BCSE based constant multiplier technique based adder structure. In the proposed RCA technique, the availability of buffer in architecture, causes an increased power utilization by 4.79 % when contrasted with RCA based technique. Similarly, in the proposed NAND based RCA, there is an increase in 3.74 % of power when compared with the existing NAND based RCA. This is due to the elimination of redundant NOT gates in the adder structure. The proposed buffer based RCA technique causes delay improvement by 7.4 % compared to the existing RCA. The buffer based NAND RCA technique has 8.2 % improvement over NAND based RCA strategy as shown in the Figure 3

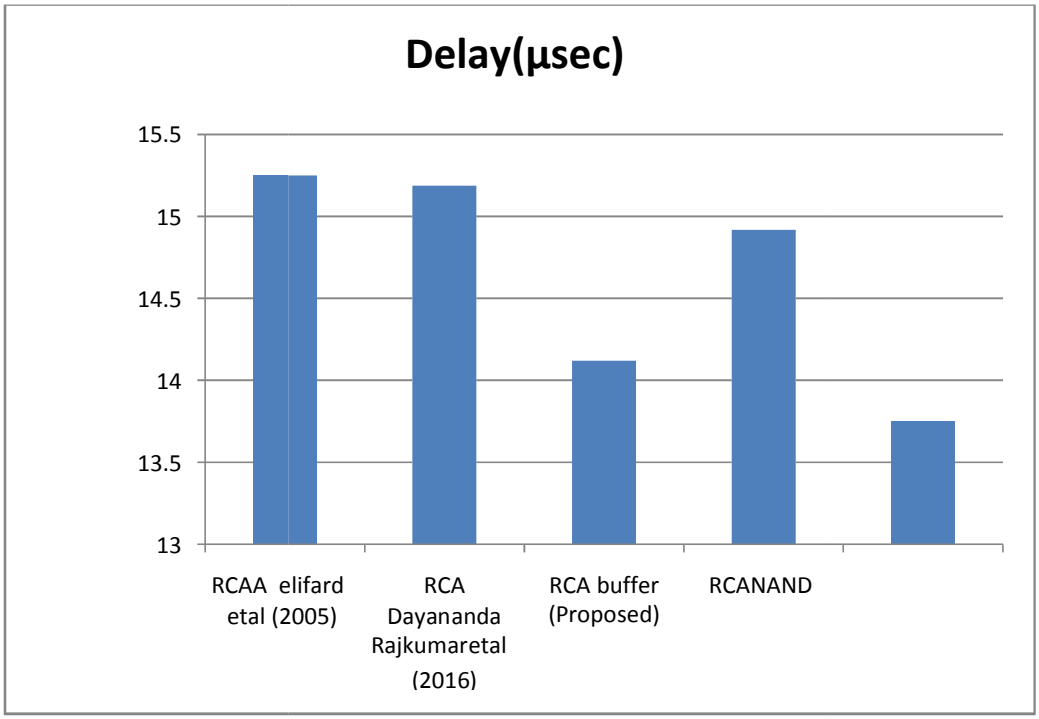

Figure 3 Delay Graph for 2 bit BCSE Constant Multiplier using Existing and Proposed RCA Adders

Table 2 Comparison of 3 bit BCSE Constant Multiplier Area, Power, Delay and PDP using RCA

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S. No	Methods	3 bit BCSE constant multiplier			
		Areaμm^2	Powerμw	Delay μsec	PDP μw- μsec
1	RCA Amelifard *et al.* (2005)	69528	2732.19	18.5	50545
2	RCA Dayananda Rajkumar *et al.* (2016)	69437	2730.32	18.4	50237
3	Proposed RCA withbuffer	72426	2931.31	17.1	50229
4	RCA NAND Mano(2017)	65780	2864.16	18.1	51841
5	Proposed RCA NANDwith buffer	68678	2964.78	17.4	51587

Figure 4 shows the improvement in Power Delay Product (PDP) over the existing and proposed adders used in the 2 bit BCSE ConstantMultiplier architecture. It shows a 2.7 % improvement in existing RCA based constant multiplier over the buffer based RCA constant multiplier. Similarly a 4.2 % improvement is seen in PDP in the buffer based NAND RCA 2 bit BCSE constant multiplier architecture over NAND based RCA.

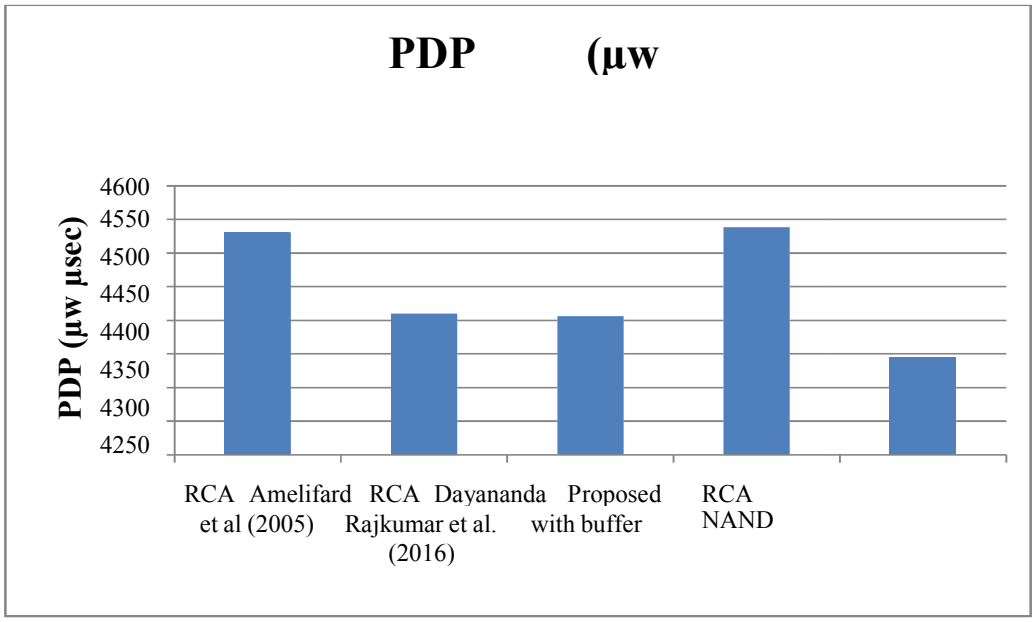

Figure 4. PDP Graph for 2 bit BCSE Constant Multiplier using Existing and Proposed RCA Adders

Table 2, shows the results of Area, Power, Delay and PDP 3 bit Constant Multiplier for the existing method and the proposed method adders. Here, the existing RCA method is compared with the buffer based RCA while the existing RCA NAND methods are compared with the RCA NAND with buffer method. The proposed buffer RCA method shows a decrease in delay over 7.5 % in the existing RCA method. The NAND based techniques demonstrate 3.8 % decrease in delay as shown in Figure 5.

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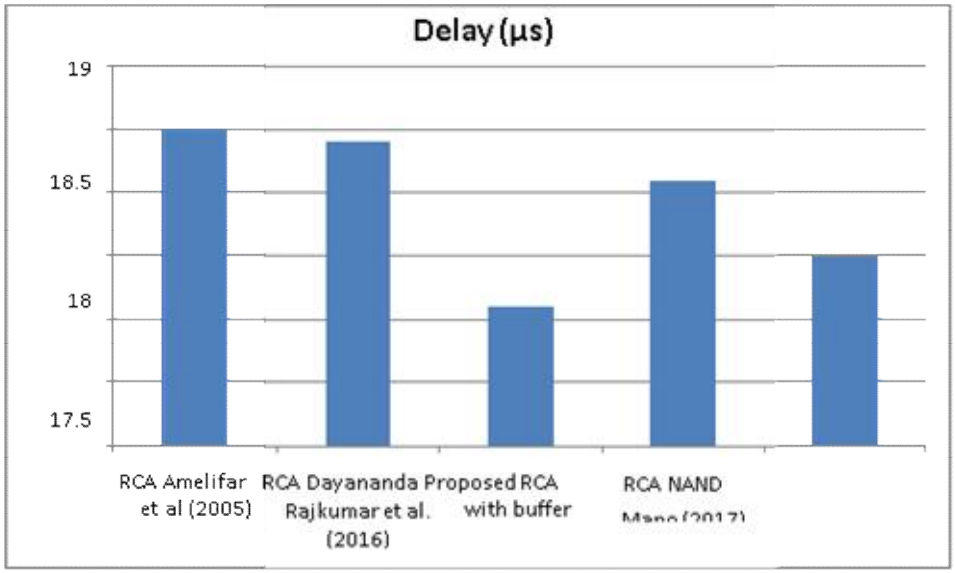

Figure 5.Delay Graph for 3 Bit BCSE Constant Multiplier using Existing and Proposed RCA adders

Similarly the PDP for the 3 bit constant multiplier is contrasted for different adder structures where the value of PDP shows the improvement over the existing methodologies as shown in the Figure 6. The proposed buffer RCA shows a 0.6 % improvement in PDP over the existing RCA based 3 bit Constant Multiplier architecture. Similarly NAND based RCA makes a 0.4 % improvement in PDP over the buffer based NAND structure.

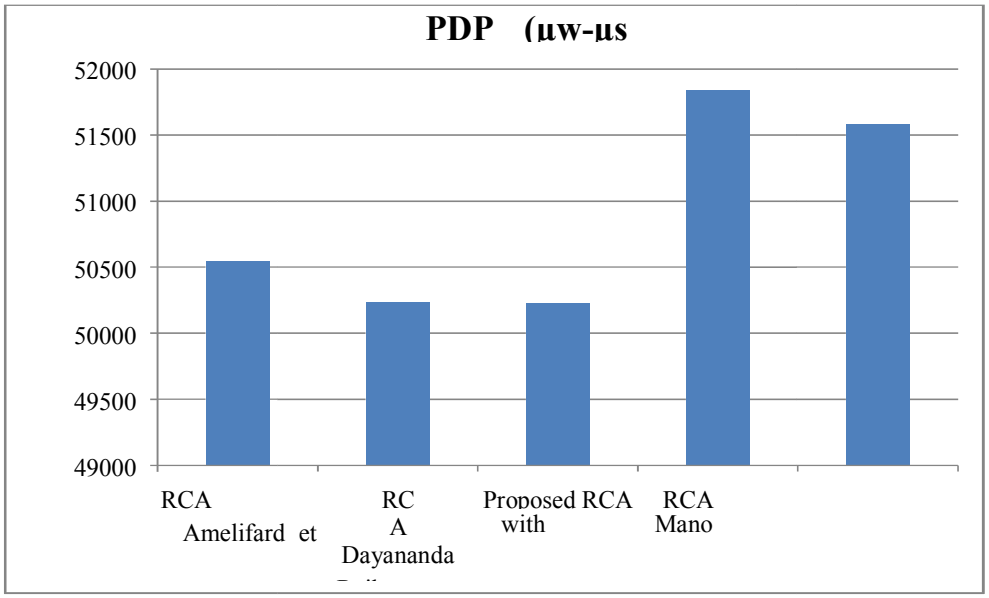

Figure 6. PDP Graph for 3 Bit BCSE Constant Multiplier using Existing and Proposed RCA adders

V. CONCLUSION & FUTURE WORK

Simulations were done using Cadence EDA tool with 180 nm technology. The constant multiplier architecture utilizes the 2 bit and 3 bit BCSE algorithm which decrease the number of adders and shifters. The multiplier architecture utilizes the RCA, NAND RCA and CSA, leading to the expansion of the adder steps and the equipment cost. The 2 bit and 3 bit BCSE algorithm utilizes productive adders such as RCA with buffer, RCA with NAND proposed. For keeping up a separation from this issue the BCSE algorithm helps reduction in the area utilization and enhanced the delay. The 2

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bit BCSE constant multiplier based on CSA adder has 0.8 to 1.2 % reduction in area and also 0.2 to 0.8 % reductions in ADP over the existing architecture. Similarly for 3 bit BCSE constant multiplier has 12 to 15 % reduction in area and 8 to 12 % reduction in the ADP over the existing architecture. Thus use of the modified CSA based 2 bit and 3 bit BCSE constant multiplier helps reduction in the area and improvement of the ADP. There is a reduction in delay and Power Delay Product in the 2 bit and 3 bit BCSE based constant multiplier architecture based on RCA and NAND based RCA structure. The proposed buffer based and NAND based 2 bit BCSE method shows a 7.4 to 8.4 % improvement over delay and a 2.7 to 7.5 % improvement in PDP compared to the existing RCA and RCA NAND constant multiplier. In addition for 3 bit BCSE constant multiplier produce a 3.8 to 7.5 % improvement in delay and a 0.4 to 0.6 % improvement in PDP than existing RCA NAND and RCA constant Multiplier architecture. Thus by using the buffer based RCA and buffer based NAND 2 and 3 bit BCSE constant multiplier has improvement in delay and PDP. Thus high speed and area efficient adders were designed for constant multiplier architecture.

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