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Design and Analysis of CMOS Full Adder

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Abstract: *This paper presents a comparative study of Complementary MOSFET (CMOS) full adder circuits. Our approach is based on hybrid design full adder circuits combined in a single unit. Full adder circuit is an essential component for designing of various digital systems. It is used for different applications such as Digital signal processor, microcontroller, microprocessor and data processing units (DSP). In most of these systems the adder lies in the critical path that determines the overall speed of the system. Full adder is mainly used in VLSI devices like microprocessor for computational purposes. The proposed full adder cell has low power consumption, better area efficiency. Recently, there have been massive research interests in this area due to the growing need for low-power and high-performance computing systems. Our aim is to design and compare the full adder circuit in various technologies and compare their power capacity. By using the hybrid structure of NMOS and PMOS, we have implemented the circuit of full adder.*

Keywords: Technology, CMOS, Full adder, Microwind

I. Introduction

Binary addition is the basic operation found in most arithmetic components and various logic. Full Adder circuit plays an important role in low power applications as well as high power applications. Hence the realization of full adders with low power and high performance is very essential now days. Designing low-power and high speed Very Large-Scale Integration (VLSI) systems has emerged as highly in demand because of the fast-growing technologies in telecommunication and other battery power applications. One of the efficient software Microwind is used for waveform analysis. Since numerous FA (full adder) topologies have been proposed, especially in recent times, it is necessary to evaluate their performance metrics using a common platform to enable VLSI designers to pick the right FA (full adder) topology that best suits their system requirements. With the advent of the transistor and, decades later, the arrival of the IC (Integrated Circuit), power dissipation became a lesser concern. As a result, the magnitude of power per unit area has kept growing and the accompanying problem of heat removal and cooling has kept getting worse, as exemplified by general-purpose microprocessors. In this paper, the design and performance comparison of full-adder cells is implemented based on the multiplexing of the Boolean functions XOR/ XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively.

Microwind is truly integrated EDA (Electronic design automation) software encompassing IC (Integrated Circuit) designs from concept. Microwind integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. It directly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification. We have conducted simulations and results were analysed on 0.12nm, 12nm, 32nm, 45nm, 65nm and 90nm Microwind using EDA (Electronic design automation) tool.

II. Basic Adder

Half Adder is a digital combinational circuit that executes addition of two single bit binary numbers and generates two outputs i.e., a sum bit (Sum) and carry bit (Carry). If A and B are taken as primary input bits, then sum bit (Sum) is obtained by X-ORing of input bits A and B and the carry bit (Carry) is obtained by ANDing of input bits A and B. Half adder is the simplest adder circuit and used in many applications such as to design full adders and calculators, in ALU (Arithmetic Logic Unit) of various processors, to calculate the addresses and many more.

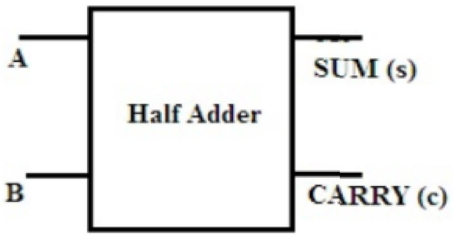

Fig 1. Block Diagram of Half Adder

Input		Output	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 1. Truth Table

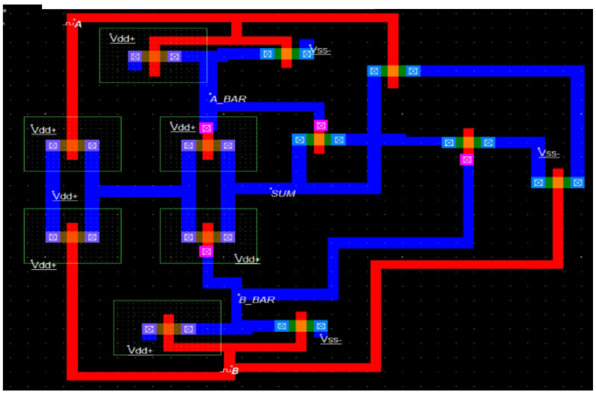

Fig 2. Simulation of Sum

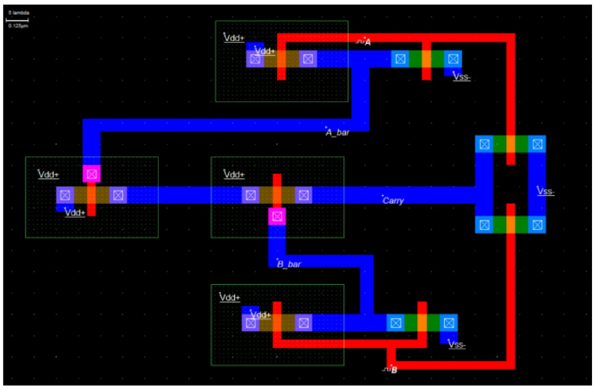

Fig 3. Simulation of Carry

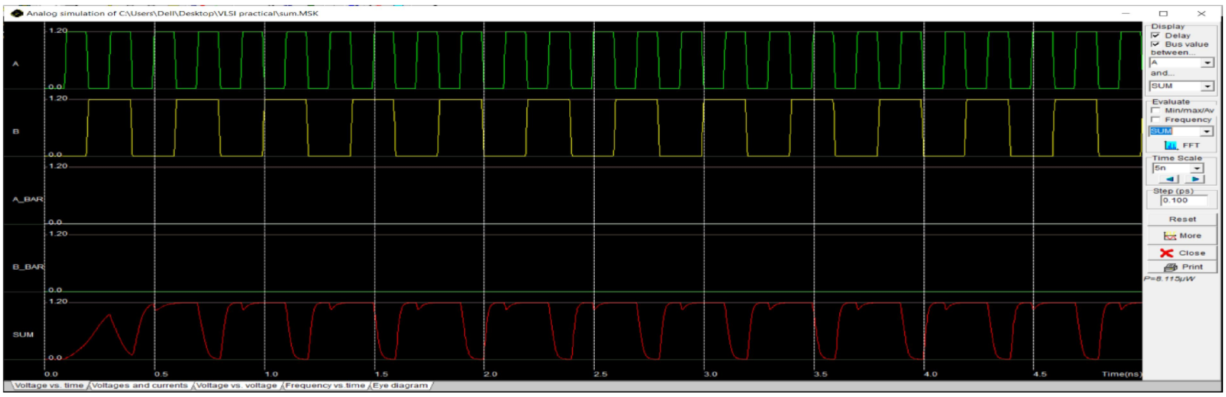

Fig 4. Waveform of Sum

Fig 5. Waveform of Carry

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III. Full Adder

There are standard implementations with various logic styles that have been used in the past to design full-adder cells and these are used for comparison in this paper. Although they all have similar function, the way of producing the intermediate nodes and the outputs, the loads on the inputs and intermediate nodes and the transistor count are varied. The fundamental distinction between the pass-transistor logic design and also the complementary CMOS logic design is the main aspect of the pass logic electronic transistor network which is connected to some input signals rather than the facility lines. The pass-transistor network logic is much more capable to implement the logical functions; by that the outputs are generated by a minimum number of electronic transistors and a lower input load. Once the transistor gates are oversized the inputs can be overloaded and it may create high capacitance values.

3.1 Basics of Full Adder

A basic full adder circuit is used to add three one-bit binary number started from "000" to "111" i.e. A, B and C. It Produce two one-bit output i.e., sum and carry. This logic expression deals with realization of full adder without utilization of XOR gate and reusing the Cout term in the Sum term as a common sub expression.

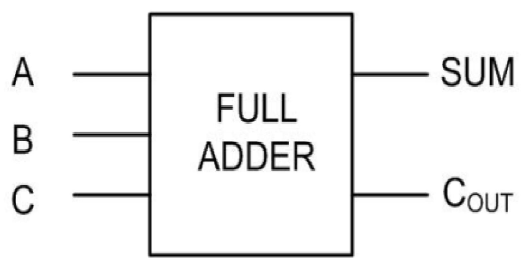

Fig 6. Block Diagram of Full Adder

INPUT			OUTPUT	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2. Truth Table Full Adder

Equations of full adder based on the truth table is get verified by using k-map is as follows:

SUM = $A \oplus (B \oplus C)$

COUT = $AB + BC + AC$ OR

COUT = $C (A \oplus B) + AB$

Some designs of the full adder circuit based on transmission gates are shown in Figure 9. Transmission gate logic circuit is a special kind of pass-transistor logic circuit. The main disadvantage of TGL (transmission gate logic) is that it requires twice the number of transistors than pass-transistor logic or more to implement the same circuit. TG gate full adder cell has 20 transistors. Similarly, transmission function full adder (TFA) cell has 16 transistors. It exhibits better speed and less power dissipation than the conventional CMOS adder due to the small transistor stack height.

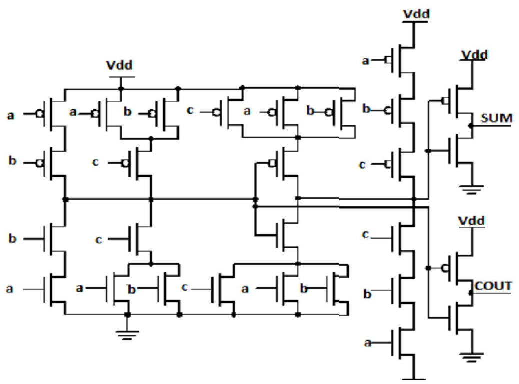

Fig 7. CMOS Full Adder

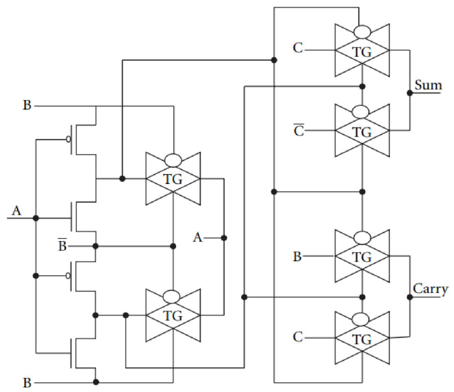

Fig 8. Transmission gate Full Adder

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3.2 Simulation and Result

The simulation results are obtained by verifying the functionality of the full adders in digital schematics and for these full adders the layouts are drawn in micro wind and waveform analysis.

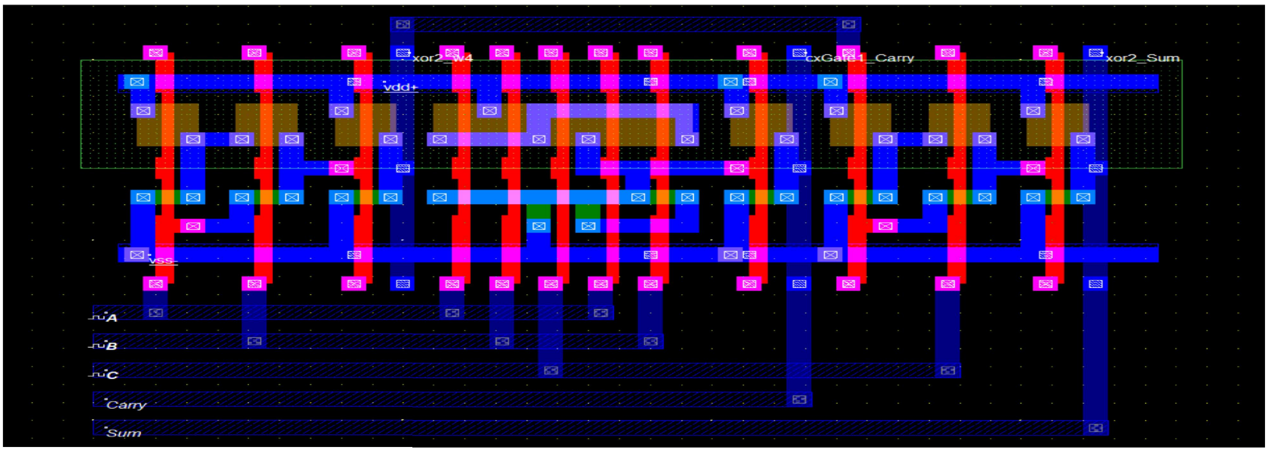

Fig 9. Simulation of full adder

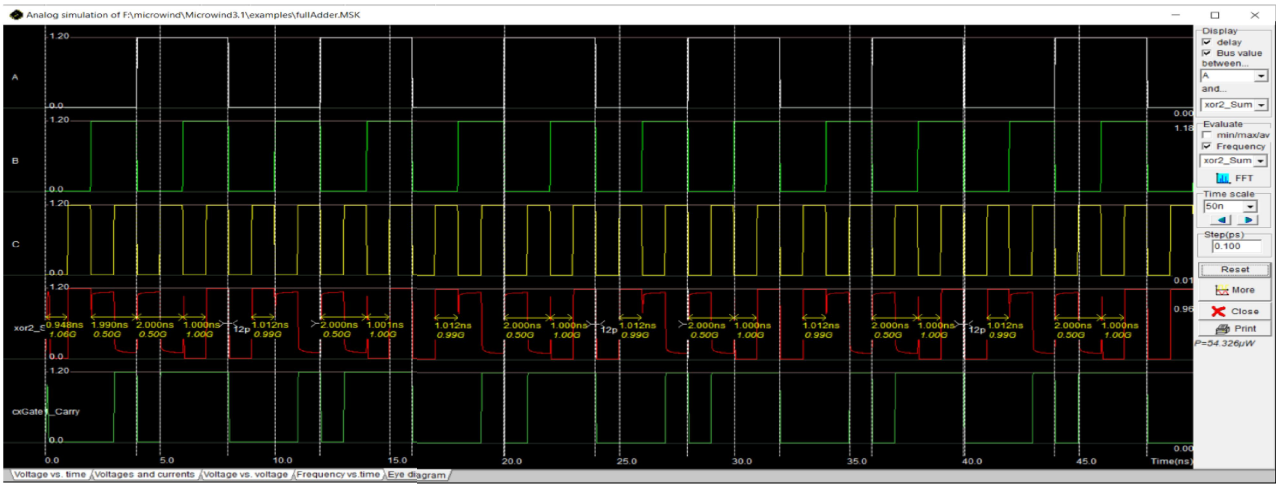

Fig 10. Waveform of full adder

3.3 Comparison of Full Adder in Power

Sr. No.	Technology	Dynamic Power
1	0.12nm	24.802 µW
2	12nm	2.694 mW
3	32nm	0.201 µW
4	45nm	0.211 µW
5	65nm	2.553 µW
6	90nm	47.333 µW

Table 3: Comparison of power using various technologies

IV. Conclusion

The CMOS full adders in different logic styles are designed and simulated. From the simulation results it is observed that the Dynamic power is get varied by using different technologies. Any arithmetic circuit which uses this low power full adder consumes low power. And using these CMOS full adders many arithmetic applications like comparator, ripple carry adder etc.

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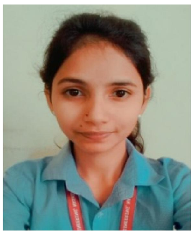
BIOGRAPHY



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