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Design and Implementation of High Speed SRAM Cell

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Abstract: *Static Random Access Memory's main design goals are to have a consuming low power and high speed, as technology is developing at a faster paceand this has given rise to new challenges.The high speed along with stability of SRAM are important issues to improve efficiency and performance of the system. This proposed work presents design and implementation of 1Kb 6T SRAM using CMOS technologies by using EDA tool. In this proposed work, SRAM's cell is operated in 1V voltage. Our proposed high speed SRAM consisting 6T achieved read delay and write delay of 29.4ps & 15ps respectively. And also our designed cell has stability of 70 mV & 195 mV for read SNM and write SNM respectively.*

Keywords: Pre-charge, Row and Column Decoder, Sense Amplifier, Column mux and Write Driver

I. INTRODUCTION

Memory arrays fall into two categories: Random Access Memory(RAM) and Serial Access Memory. Static RAM is classified as volatile memory. The volatility of SRAM gives it an edge over non-volatile DRAM, as it eliminates the need for refreshing and is faster in operation. Because of this, SRAM cells are an essential component of contemporary computer systems and a vital technological advancement for high-speed data processing. Because of its high speed and low power consumption, SRAM is frequently employed as cache memory in microprocessors, personal computers, and workstation routers. Other memory technologies like DRAM offer better cost-effectiveness for larger capacity needs, while SRAM excels in speed-critical applications. SRAM is used as Cache memory which is very fast and used to speed upthe task of processor and memory interface.

II. CONVENTIONAL 6T SRAM CELL

Two CMOS cross-coupled inverters are used in the architecture of the 1-bit 6T SRAM to function as a latch. The data to be preserved is latching onto these two inverters. Latch perform different operations, i.e. Read, Write & Hold. This latch is operated by internal pulse provided to it. Its two access transistors are used to access Bit Line, Bit Line Bar (both BL & BLB function according to WL). The fundamental design of a 6Tcell is seen in Figure 1.

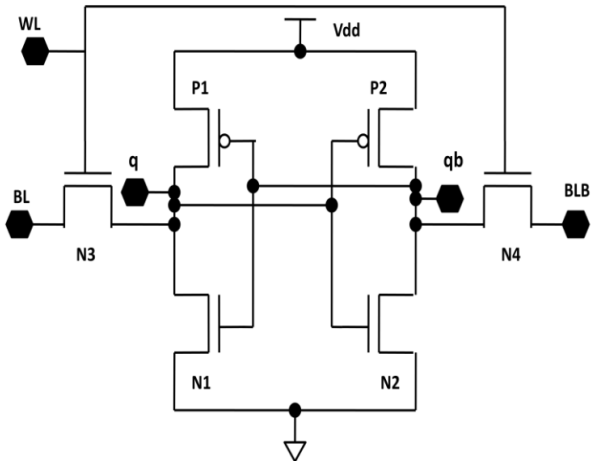

Fig.1: One bit Memory Cell

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III. PROPOSED 6T MEMORY CELL

Two cross-coupled CMOS inverters made up of two pairs of NMOS pull-down transistors (NM3 & NM4) and PMOS pull-up transistors (PM1 & PM2) make up the basic memory cell.Two additional NMOS transistors (NM1 & NM2) serve as access transistors, connecting the inverters to complementary bit lines (BL & BLB)

The SRAM can operate at high speeds by improving a number of features of its architecture and functionality. Such design aspects are as follows:

Low Voltage Operation: The static RAM was designed to run at a lower voltage, which shortens the transistors' on and off times. The Voltage used for operation is 1V.

Proper transistor sizing: Proper selecting of the width-to-length (W/L) ratios of transistors helps to achieve in reducing delay. Since the Length (L) has been fixed according to technology node, the Width (W) of transistor is changed accordingly. For the faster write operation to be possible, PMOS PM1 needs to be weaker than the access transistor NM1. To read data from the cell faster, the driver NM3 needs to be more powerful than the accessing transistor NM1. Use of wider access transistors helps for faster current flow during read/write access.

(W/L)pull-up < (W/L)access << (W/L) pull-down.

The table below shows the proposed 6T SRAM cell's dimensions.

Design of Peripheral Circuits: By designing peripheral circuits such sensing amplifiers, write driver circuits, and pre-charges, read/write performance is greatly increased and cell latency is decreased.

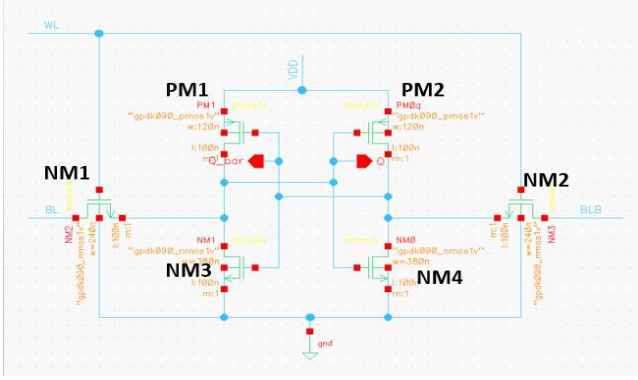

Fig.2 Proposed Cell

Table1:Transistor sizing of our proposed 6 Transistor cell

Description	Transistor	Width
Memory Element of SRAM	PM1	120n
	PM2	120n
	NM3	380n
	NM4	380n
Access Transistor	NM1	240n
	NM2	240n

IV. PRECHARGE CIRCUIT

The pre-charge circuit is one of the crucial components of the SRAM cell that is constantly in use.The bit lines and bit line bar are charged using this circuit to supply voltage VDD/2, and pre-charging must be completed before each write and read operation. Transistors M1 and M0 will pre-charge the bit lines prior to that cell being read, and transistor M2 will equalize them to ensure that every bit line in a pair is at the same potential. As bit lines have high capacitance, precharge circuit needs to provide large current to bit lines to get charged quickly

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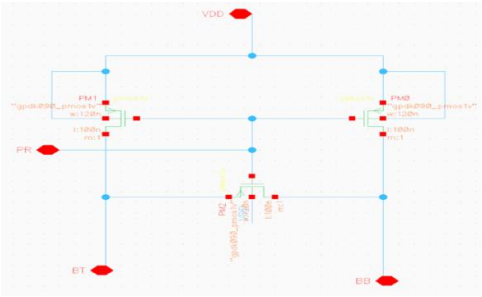

Fig.3: Pre-charge Circuit

V. WRITE-DRIVE CIRCUIT

When the enable signal (WE) is high, the input data (DATA) is written into the bitlines (BL and BLB) using two pass transistors (NM1 and NM2). If DATA is high, BL is pulled high and BLB is pulled low, and vice-versa if DATA is low. This written data is then stored to the corresponding SRAM cell connected to the activated bitlines.

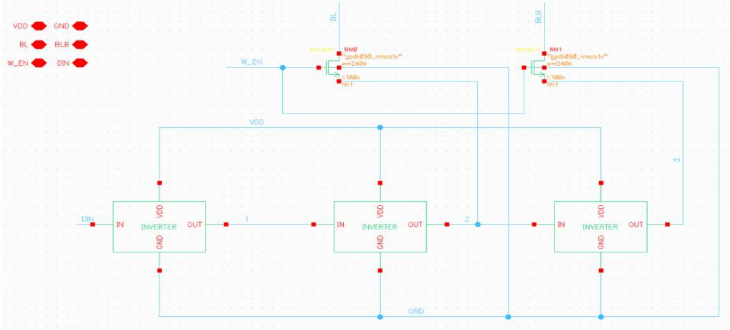

Fig.4: Write-Driver Circuit

VI. DESIGN OF SENSE-AMPLIFIER CIRCUIT

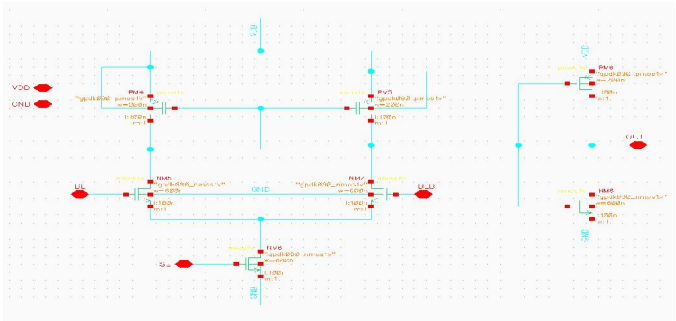

Fig.5: Sense-Amplifier Circuit

Sense-amplifier circuit is used to speed up the read cycle operation in the memories. Sense-amplifier circuitry takes the small signal difference bit line voltage as input and gives full swing single ended output.Access time and power consumption of memory is affected by the sense-amplifier circuitry hence the performance of memory is improved by reducing both sensing delay and power dissipation.

VII. ROW-DECODER, COLUMN-MUX AND COLUMN-DECODER

These three circuits block work together to enable efficient and accurate access of data bit in the SRAM memory array. Without these circuit blocks, it is impossible to address and retrieve specific data elements from the vast array memory.

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- **Addressing:** The Row-Decoder and Column-Decoder ensure that the correct SRAM Cell gets selected for reading or writing.
- **Data Transfer:** The column MUX ensures the data of the selected columns is properly routed to the output, enabling the transfer of multiple bits of data in parallel.

VIII. BLOCK DIAGRAM OF 1KB SRAM CELL

Fig. 6 shows 1-kb SRAM block structure which includes Cell Array, decoder, sense amplifier, write driver, column MUX and pre-charge circuitry as the peripheral circuit to the SRAM cell array.

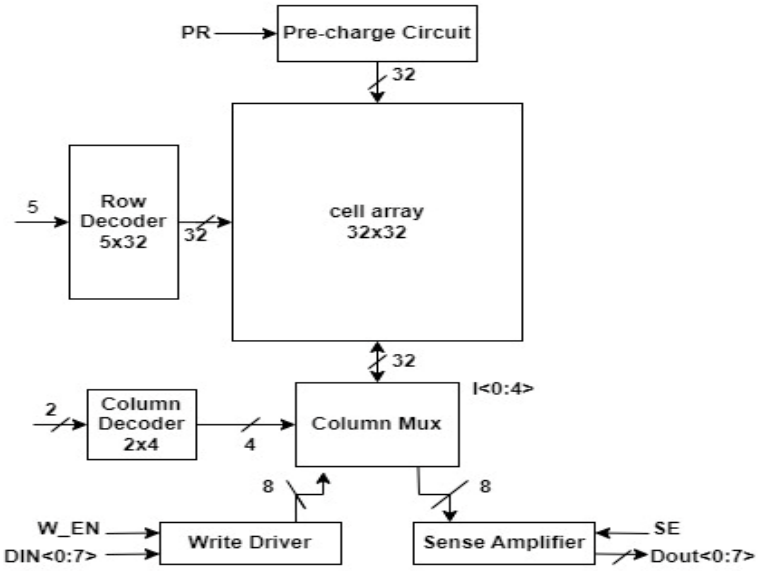

Fig.6: Block Diagram of 1KB SRAM Cell

Core Components:

- **Cell Array (32x32):** The heart of the SRAM Memory, this is a two-dimensional grid where data is stored. Each cell in the array is a tiny sram cell that holds data.
- **Row Decoder (5x32):** This circuit receives a 5-bit row address and activates the corresponding row in the cell array.
- **Column Decoder (2x4):** This circuit receives a 2-bit column address and activates the corresponding columns in the cell array.
- **Column Mux:**The column MUX ensures that the data of the selected columns is properly routed to the output, enabling the transfer of multiple bits of data in parallel.
- **Sense Amplifiers:** These amplifiers detect the tiny charges in the activated cells and convert them into a readable voltage level.
- **Write Driver:** This circuit amplifies the data input and drives it into the activated cells during a write operation.

Pre-charge Circuit: This circuit ensures that the bitlines are pre-charged to VDD/2 before read write operation.

Input/Output Pins:

- **DIN<0:7>:** 8-bit data input lines for writing data into the SRAM.
- **Dout<0:7>:** 8-bit output data lines for reading data bit from the SRAM.
- **W_EN:** Write enable control signal to write driver, for write operation to be performed.

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- **SE:** Sense amplifier circuit enable signal which controls the activation of the sense amplifiers during a read operation.
- **PR:** Pre-charge enable signal which controls the pre-charging of the bitlines.

VIII. SIMULATION RESULTS

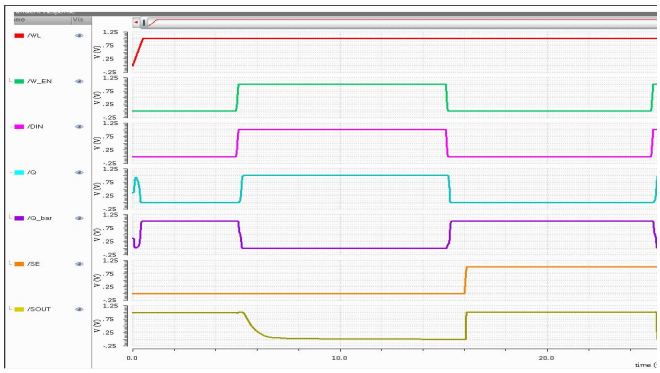

Fig.7: Simulation results of 1bit SRAM memory Cell

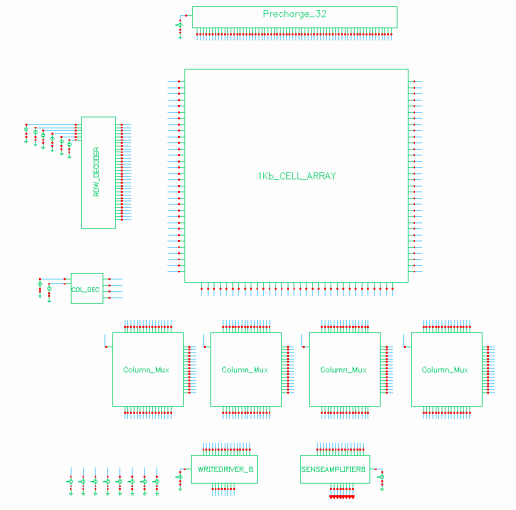

Fig.8: Schematic of 1Kb SRAM memory

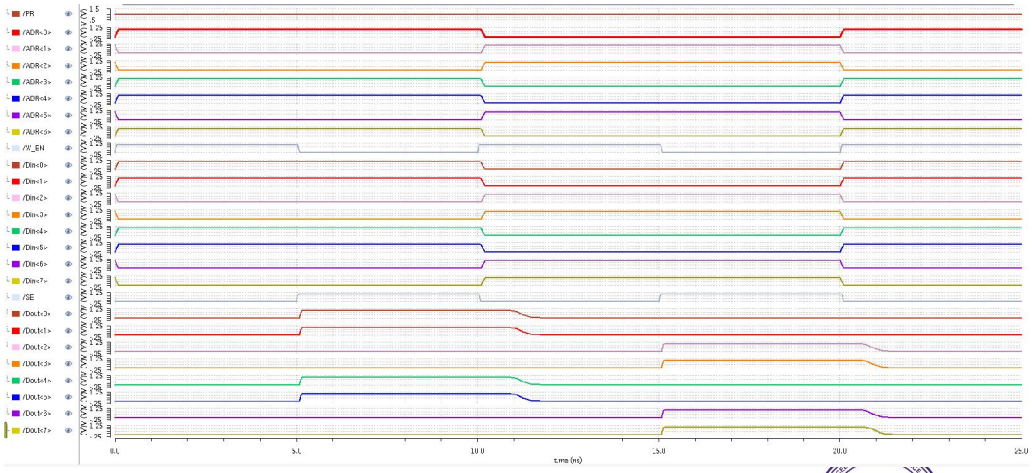

Fig.9: Waveform of 1KB Memory

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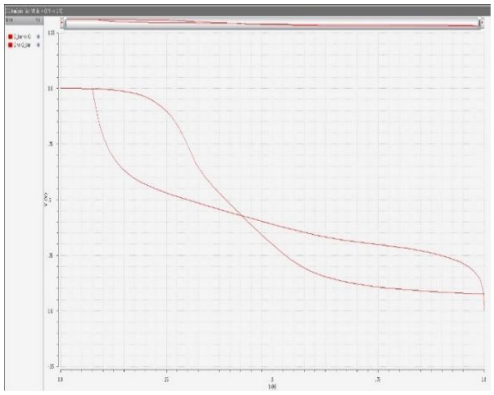

Fig.10: Read SNM curve

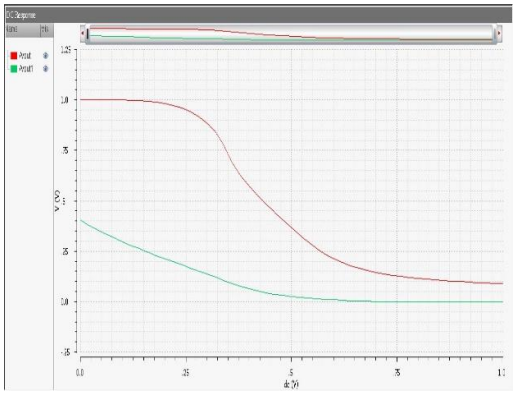

Fig.11: Write SNM curve

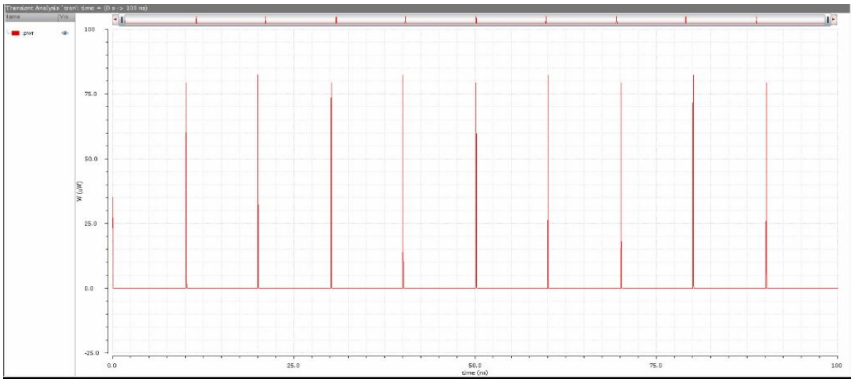

Fig.12: Power-DissipationGraph

Table 2: Results

Parameters	Values Obtained
Read Delay	29.4ps
Write Delay	15ps
Dynamic-Power Dissipation	82.231uW
Static-Power Dissipation	36.617nW
Write SNM	195mV
Read SNM	70mV

IX. CONCLUSION

The performance of a 1Kb Static Random-Access Memory (SRAM) was analyzed using a 1-bit 6T SRAM. Simulations were done with in Virtuoso tool using 90nm CMOS technology. Future work involves manufacturing a 2kb and 1MB chip based upon the 1kb block design. The goal is to maintain an similar operating frequency for the 1MB memory as the 1kb design. High-speed performance and 90nm CMOS technology presented unique challenges, particularly in transistor sizes and interconnect delays. The project also focused on analyzing delays to ensure the memory operates within the required speed.

GitHub Link:

https://github.com/Sandeshg25/Design_and_Implementation_of_High_Speed_1Kb_SRAM_Memory_Array

X. ACKNOWLEDGMENT

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