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FPGA Implementation of DFT Processor using Vedic Multiplier

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Abstract: *Many a times Mathematical computations are easier in frequency domain than time domain. Discrete Fourier transform (DFT) is a tool to convert signals from time domain to frequency domain which is widely used mainly in Digital Signal and ImageProcessing applications. Fast Fourier Transform (FFT) is a method to find DFT in time constraint applications which is affected by number of complex multiplier. In this paper 16-bit DFT using Vedic Multiplier, a high- speed multiplier is proposed with an objective to replace conventional complex multiplier and to decrease computation time. The proposed system is implemented in Virtex-4 FPGA and the results show that FFT using Urdhva Tiryakbhyam algorithm of Vedic multiplier is faster than other methods of DFT*

Keywords: Vedic Multiplier; Discrete FourierTransform; Fast Fourier Transform; Computational time

I. INTRODUCTION

Technology is moving towards optimized systems. Fast, high performance and less power dissipation are key areas of focus for technological advancement. An area of research in Digital Signal Processing, Digital filtering, Spectral Analysis, Digital Image Processing, Speech processing and recognition, Audio Signal Processing, compression of audio and video, Digital communication systems, Radar, Sonar etc., mainly requires Discrete Fourier Transform (DFT) as the main tool. With increasing demand of the DFT algorithm, the need for fast computation with accurate results arises. The basic units of DFT are complex adders, complex multipliers and delay elements. The speed of the algorithm is considerably affected due to number of complex multipliers and designing it constitutes the main challenge while implementing DFT.

Amongst different multipliers available such as Array Multiplier, Baugh Wooly multiplier, Braun and Wallace tree, Vedic multiplier is a high-speed multiplier which is derived from the ancient Indian puranas and scripts. In Vedic Multiplication, real time scenarios are converted to word problems and common man methodologies are applied on. The Vedicmultiplierisa short hand method for multiplying single to multiple digit numbers in a fraction of time. This is achieved by performing parallel multiplication as Vedic multiplier follows pipelined multiplier architecture for high speed. To get the essence of the Vedic multiplier, different forms of DFT is implemented and the computational time is compared with that of conventional multiplier. Also, FFT algorithm is ahead of other forms of DFT, if computational time is considered as a major factor.

The lesser computational time by Vedic Multiplieris because of parallel multiplication process. This advantage can be further enhanced using FPGA (Field Programmable Gate Arrays) over microcontrollers since FPGA has the ability of parallelism within device to maximize the performance [6].

In this paper, the capability of Urdhva Tiryakbhyam (UT) algorithm based FFT is implementedin FPGA and compared with conventional multiplier. Also, DFT with conventional algorithm and Vedic multiplier based FFT is compared and results are presented here.

II. BACKGROUND STUDY

Often it is easier to work on frequency domain signals than time domain signals. Discreate Fourier Transformor DFT is frequency domain representation of the time domain input sequence. The basic element of DFT that influences the computational speed, area and power dissipation is the complex multipliers. Many high-speed multipliers are available.

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An intense research and comparison amongst them have been performed and observed that there is always a trade-off between speed, area and power dissipation. Compared to Booth multiplier and Lion's bit serial multiplier, GF(2^n) gives a better result [1].

FFT is an algorithm that rapidly computes DFT, i.e. signals of a time domain to frequency domain representation by divide and conquer rule, thus reducing complexity. FFT can be computed by decomposing the time domain sequence of size N to even and odd sequence of size N/2. Thus, a larger DFT is divided to smaller sub transforms which can be represented using butterfly units [7].Large body of knowledge texts originating in the ancient Indian subcontinent is called Vedas. Based on it, few techniques have been formulated for mental calculation known as Vedic Mathematics by an Indian Monk Jagadguru Swami Sri Bharati Krsna Tirthaji Maharaja [2]. Multiple ways of Vedic multiplication are possible with sutras - Nikhilam Sutra, Anurupyena Sutra, Urdhva Tiryakbhyam Sutra, Vinnculum Process, Ekayunena Purvena and Antyaordaske'pi, of which only Urdhva Tiryakbhyam is a general technique while others are specific techniques [3], [8]. Multipliers are of two types Serial and parallel multipliers. Serial Multipliers has the advantage of chip size optimization.

Parallel multipliers compromise on hardware size but has the merit of low computation time. Vedic Multiplier based on Urdhva Tiryakbhyam(UT) algorithm is a parallel multiplier, wherein concurrentaddition of all partial products occurs parallel, thus the processing becomes independent of clock frequency. Thus, this clock frequency independence and parallel multiplication enables clock to operate on low frequency which aids in achieving lower power dissipation, lower operating temperature and higher speed and efficient regular structure which makes it easier to make layout. Thus, a Vedic multiplier is ahigh-speed multiplier whose time of computation increases gradually for increased number of bits as compared to conventional multiplier making it time and power efficient. [5]

III. IMPLEMENTATION

DFT Algorithm

The N point DFT is given in equation 1, where n is thelength of the input sequence.

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi kn/N} \quad (1)$$

Four input DFT for values x0_r + j x0_i, x1_r + j x1_i, x2_r + j x2_i, x3_r + j x3_i is implemented, which were obtained from expanding the generalized equation and separating real and imaginary parts as in equation 2, 3,4 and 5.

For k=0,

$$X\_r(0) = x0\_r + x1\_r + x2\_r + x3\_r$$
$$X\_i(0) = x0\_i + x1\_i + x2\_i + x3\_i \quad (2)$$

For k=1,

$$X\_r(1) = x0\_r + (-j)x1\_i - x2\_r + (+j)x3\_i$$
$$X\_i(1) = x0\_i + (-j)x1\_r + x2\_i + (+j)x3\_r \quad (3)$$

For k=2,

$$X\_r(2) = x0\_r - x1\_r + x2\_r - x3\_r$$
$$X\_i(2) = x0\_i - x1\_i + x2\_i - x3\_i \quad (4)$$

For k=3,

$$X\_r(3) = x0\_r + (+j)x1\_i + x2\_r + (-j)x3\_i$$
$$X\_i(3) = x0\_i + (+j)x1\_r + x2\_i + (-j)x3\_r \quad (5)$$

FFT Algorithm

FFT algorithm is implemented using butterfly diagrams.

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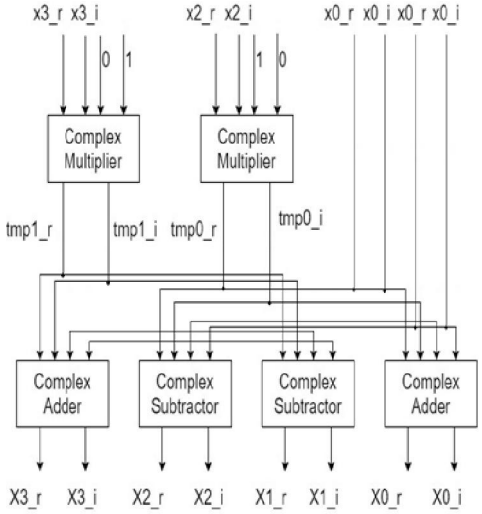

Figure 1. Implementation of Four Point Butterfly Four input FFT for real integer values, x0, x1, x2, x3 is implemented. The sequence is first divided into even (x0, x2) and odd (x1, x3) sequence and Two Point butterfly is calculated and then passed to a Four Point butterfly to complete the FFT process as illustrated in the figure 1.

Vedic Multiplier

Vedic multiplier is a fast and parallel multiplier which follows pipelined architecture. It has been obtained from one of the sixteen sutras of Vedic Mathematics which is Urdhva Tiryakbhyam(UT) algorithm. Urdhva Tiryakbhyam means vertically and crosswise. The algorithm involves vertical and cross lines and each line represent multiplication of corresponding values. The process begins by drawing a vertical line connecting the LSB bits, a0 and b0 of two numbers involved in multiplication, say A(a1a0) and B(b1b0). Then crosslines are drawn to connect a1 and b0, and b1 and a0. The products obtained are added together with previous carry (from a0b0), if any. Lastly, vertical line connects the MSB bits, a1 and b1 and carry from previous stageis added with it to get the final multiplication results. This process of two-bit multiplication has been illustrated using line diagram in Fig.2. It takes lesser computation time to compute for positive and negative values. Immediate products are generated in parallel hence reducing steps for multiplication. Illustration of UT algorithm for four, eight and sixteen bits is shown using line diagram in Fig.3, Fig.4 and Fig.5 respectively. Four-bit numbers a3a2a1a0 and b3b2b1b0 is multiplied and an eight-bit result is obtained. Here we reuse the two-bit multiplier by combining bits. First, LSB bits a1a0 and b1b0 are multiplied. Then cross multiplication of a1a0 and b3b2 and, a3a2 and b1b0 is performed, summed along with previous carry, if any. The carry obtained in this step is added with the multiplication result of a3a2 and b3b2 to obtained the final result. Thus, for an N-bit input, (N/2) bit Vedic Multiplier and UT algorithm is considered and result of 2N bits is obtained.

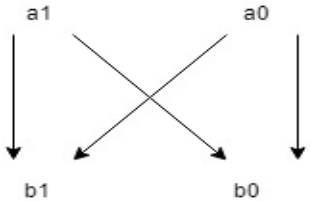

Figure 2. Urdhva Tiryakbhyam (Vertical & Crosswise)for two-bit number

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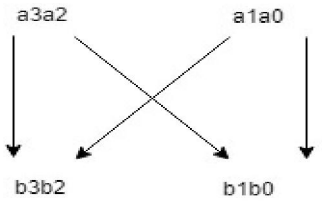

Figure 3. Urdhva Tiryakbhyam (Vertical & Crosswise)for four-bit number

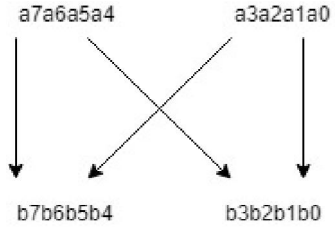

Figure 4. Urdhva Tiryakbhyam (Vertical & Crosswise) for eight-bit number

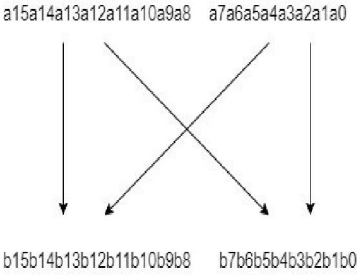

Figure 5. Urdhva Tiryakbhyam (Vertical & Crosswise)for sixteen-bit number

Complex multiplication is then performed based onthese Vedic multipliers as in equation 6.

(6) $(a + ib) * (c + id) = (ac - bd) + i(ad + bc)$

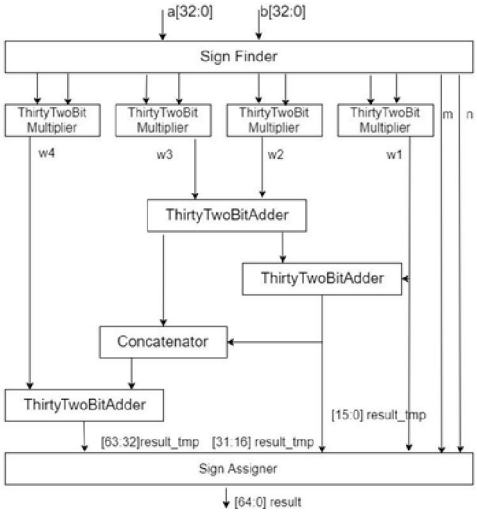

Figure 6. Implementation of Eight-bit Vedic Multiplier

UT algorithm is initially applied for two-bit inputs a1a0 and b1b0.Referring to the Line Diagram, here each stage input is single bit, hence, and gate and half adders are used for implementation, to obtain four-bit output [3:0] result. For four-bit input a3a2a1a0 and b3b2b1b0, each input is split to two bits (a3a2, a1a0, b3b2, b1b0) and pass it to a Two-bit Vedic multiplier and UT algorithm is applied over it, and eight-bit [7:0] result is calculated. Similarly, for eight-bit input a7a6a5a4a3a2a1a0 and b7b6b5b4b3b2b1b0, each input is split to four bits (a7a6a5a4, a3a2a1a0, b7b6b5b4, b3b2b1b0) and employ Four-bit Vedic multiplier and UT algorithm and get [15:0] result as illustrated in Fig.6.

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IV. RESULTS AND DISCUSSION

The proposed four-point DFT architecture using conventional multiplier and Vedic multiplier was modeled using Verilog HDL. The functionality was tested by creating stimulus blocks and observed in Xilinx ISim. The values were verified with MATLAB. Fig.7. presents the simulation results of the proposed design.

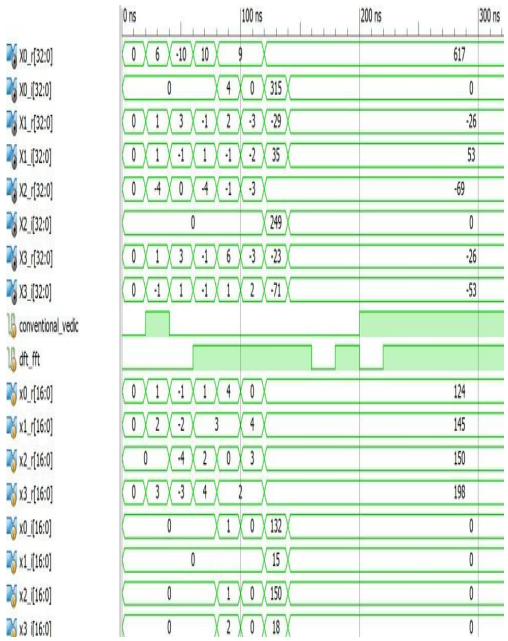

Figure 7. Simulation Result of Implementation of DFTand FFT using Conventional and Vedic Multiplier

The design is tested for three different input sequences of 16-bit values: positive integers, negative integers and complex numbers. The output values are 64 bits wide. In case of complex numbers, real numbers are 64-bits and imaginary numbers are 64-bits wide. The design after logic verification is implemented in Xilinx Virtex4 xc4vsx25 FPGA. The logic synthesis for the design in FPGA is given in Table I.

Table 1. Device Utilization Summary

DFT Processor	4-input LUTs	Slices
With conventional multiplier	176	96
With Vedic Multiplier	239	133
Using FFT	363	182
Using FFT with Vedic multiplier	403	213

The delay summary of the logic synthesis is shown in Table II. The table shows that the total delay including logic delay and the route delay is less for Vedic multiplier implementation. Even though the device utilization seems to be slightly more than conventional multiplier, the delay involved is less for Vedic multipliers.

Table 2. Delay Summary

DFT Processor	Logicdelay (ns)	Routedelay (ns)	Totaldelay (ns)
With conventional multiplier	17.67	4.69	22.36
With Vedic Multiplier	12.75	8.33	21.09
Using FFT	7.93	6.49	14.4
Using FFT with Vedic multiplier	9.45	3.77	13.22

The onboard clock frequency of FPGA is 40MHz and the control parameters are applied through the IO port. Inputs are given through DIP switches and results were verified through display. The sample inputs applied to the DFT processor implemented in FPGA and the corresponding outs are given in Table III.

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Table 3. Sample Input and Corresponding Output

	Input Sequence	Output insigned Decimalform
Positive Integer	[1 2 0 3]	[6 1+j -4 1-j]
Negative Integer	[-1 -2 -4 -3]	[-10 3-j 0 3+j]
Complex numbers	[124+ 132j 145 + 15j 150+150j 198+18j]	[617+315j - 29+35j -69+249j -23-71j]

V. CONCLUSION

In this paper, Vedic multiplier for performing complex multiplication of Discrete Fourier Transform and Fast Fourier Transform is proposed. 16-bit DFT using Vedic Multiplier is implemented and compared with conventional complex multiplier. It is observed that the computation time decreased with Vedic multiplier implementation. The proposed system is implemented in Virtex-4 FPGA and the results show that FFT using Urdhva Tiryakbhyam algorithm of Vedic multiplier is faster than other methods of DFT. Thus, the parallel processing of Vedic multiplier gives advantage of reduced computational time while implementing DFT.

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