IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.301
Volume 3, Issue 2, December 2023

SPI Master Slave Communication

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Abstract: *The serial-peripheral interface (SPI) protocol also called asynchronous serial interface specification is used for communication between single master and single/multiple slaves. With the increase in number of slaves causing high complexity of circuit creates a demand in self-test ability feature for SPI module in order to test for fault free circuits. Built-In-Self-Test (BIST) in the answer for self-test in circuits as well as it helps in reduction of maintenance and testing cost. Design of BIST embedded SPI module with single master and single slave configuration has been introduced in these paper, Here 8-bit is transferred across the module, Where the Circuit under Test (CUT) is being Self-Tested with BIST feature for its correctness. This SPI module is designed using Verilog hardware description language(HDL) using EDA playground platform for application like applications specific integrated circuit (ASIC) or system on chip (SOC). SPI stands for the Serial Peripheral Interface. It is a serial communication protocol that is used to connect low-speed devices. It was developed by Motorola in the mid-1980 for inter-chip communication. It is commonly used for communication with flash memory, sensors, real-time clock (RTC), analog-to-digital converters, and more. It is a full-duplex synchronous serial communication, which means that data can be simultaneously transmitted from both directions. The main advantage of the SPI is to transfer the data without any interruption. Many bits can be sent or received at a time in this protocol. In this protocol, devices are communicated in the master-slave relationship. The master device controls the slave device, and the slave device takes the instruction from the master device. The simplest configuration of the Serial Peripheral Interface (SPI) is a combination of a single slave and a single master. But, one master device can control multiple slave devices..*

Keywords: Serial Peripheral Interface

I. INTRODUCTION

SPI interface followed ban introduction to Analog Devices' SPI enabled switches and mixes, and how they help reduce the number of digital GPIOs in system board design. SPI isa synchronous, full duplex main-sub node-based interface [1]. The data from the main or the sub synchronization on the rising or falling clock edge. Both main and sub node can transmit data at the same time. The SPI interface can be either 3-wire or 4-wire. This article focuses on the popular4-wire SPI interface. Serial peripheral interface (SPI) is one of the most widely used interfaces between microcontroller and peripheral ICs such as sensors, ADCs, DACs, shift registers, SRAM, and others. This article provides a brief description of the SPI interface followed by an introduction to Analog Devices' SPI enabled switches and mixes, and how they help reduce the number of digital GPIOs in system board design. SPI is a synchronous, full duplex mainsub node-based interface. The data from the main or the sub node is synchronized on the rising or falling clock edge. Both main and sub node can transmit data at the same time. The SPI interface can be either 3-wire or 4-wire. This article focuses on the popular 4-wire SPI interface.

In short, in this communication protocol, devices exchange data in master/slave mode. The master device is mainly responsible for the initiation of the data frame. The master device also selects the slave device to which data need to be transferred. Chip select line is usually used to identify or select a particular slave device.Whenever a master device read to transmit data to slave or want to receive data from the slave, the master does so by activating the clock signal. Every master device sends data on the MOSI line and receives data through another line that is MISO.

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II. LITERATURE SURVEY

The literature review of Serial Peripheral Interface (SPI) with Single Master and Single Slave ensures us to implement the design using FPGA as Master and other Peripheral as a Slave. The Low power SPI Protocol can be implemented on FPGA using various EDA tools by which its functional verification can be done through Functional Simulation. The history ofSPI dates back to the early days of microelectronics, primarily in the 1980s when it was introduced by Motorola. Originally designed for communication with in single integrated circuits, SPI has evolved to support communication between various microcontrollers, sensors, displays, memory devices, another peripherals. SPI communication typically involves master device and one or more slave devices connected through four essential lines: Master Out Slave In (MOSI), Master In Slave Out (MISO), Serial Clock (SCK), and Slave Select (SS/CS). Researchers have extensively explored the details of SPI modes (0, 1, 2, and 3), focusing on clock polarity and phase configurations to enable precise data transfer. Efforts have been directed towards enhancing the performance of SPI communication. This includes studies on increasing data rates, minimizing latency, and reducing power consumption. Researchers have explored various clocking schemes and techniques.

III. VERY LARGE SCALE INTEGRATION (VLSI)

The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as small-scale integration (SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like ultra-large-scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread.

In 2008, billion-transistor processors became commercially available. This became more commonplace as semiconductor fabrication advanced from the then-current generation of 65 nm processors. Current designs, unlike the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high-performance logic blocks like the SRAM (static random-access memory) cell, are still designed by hand to ensure the highest efficiency.

IV. EXISTING SYSTEM

The inception of VLSI technology can be traced back to the 1970s when the first microprocessor was introduced. A milestone that showcased the potential of VLSI design and integrating multiple transistors on a single chip. This breakthrough marked the beginning of a new era in microelectronics.single chip can hold an ever-increasing number of transistors thanks to VLSI technology. The creation of transistors with smaller dimensions and better performance characteristics has been made possible by the development of semiconductor materials and manufacturing techniques. These advancements in VLSI design has caused an ongoing rise in integration density, allowing for the creation of extremely sophisticated and complex electronic systems.As the number of transistors integrated on a chip increases, the processing power of electronic systems also improves significantly. With more transistors available, complex computations can be executed at a faster rate, enabling high-performance computing. As a result, disciplines like artificial intelligence and machine learning, data analytics, and scientific simulations have advanced significantly.

V. SOFTWARE USED

Xilinx sells a broad range of FPGAs, complex programmable logic devices (CPLDs), design tools, intellectual property and reference designs.[16] Xilinx customers represent just over half of the entire programmable logic market, at 51%. Altera (now subsidiary of Intel) is Xilinx's strongest competitor with 34% of the market. Other key players in this market are Actel (now subsidiary of Microsemi), and LatticeThe main design toolkit Xilinx provides engineers is

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the Vivado Design Suite, an integrated design environment (IDE) with a system-to-IC level tools built on a shared scalable data model and a common debug environment. Vivado includes electronic system level (ESL) design tools for synthesizing and verifying C-based algorithmic IP; standards based packaging of both algorithmic and RTL IP for reuse; standards based IP stitching and systems integration of all types of system building blocks; and the verification of blocks and systems. A free version WebPACK Edition of Vivado provides designers with a limited version of the design environment.

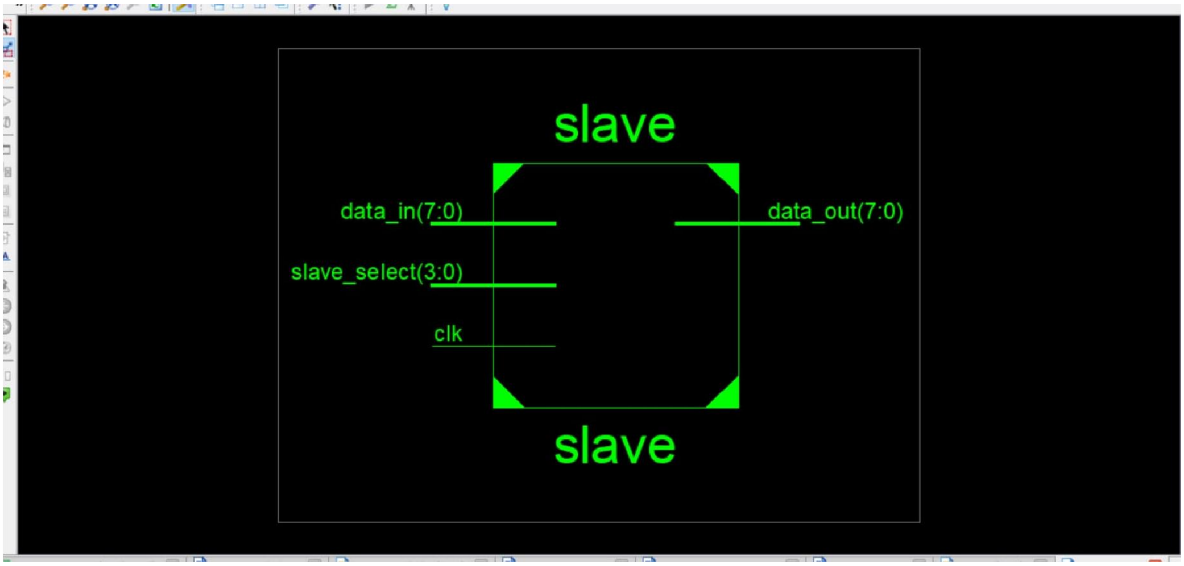
In 2019, Xilinx exceeded $3 billion in annual revenues for the first time, announcing revenues of $3.06 billion, up 24% from the prior fiscal year. Revenues were $828 million for the fourth quarter of the fiscal year 2019, up 4% from the prior quarter and up 30% year over year. Xilinx's Communications sector represented 41% of the revenue; the industrial, aerospace and defense sectors represented 27%; the Data Center and Test, Measurement & Emulation (TME) sectors accounted for 18%; and the automotive, broadcast and consumer markets contributed 14%.

In August 2020, Subaru announced the use of one of Xilinx's chips as processing power for camera images in its driver-assistance system. In September 2020, Xilinx announced its new chipset, the T1 Telco Accelerator card, that can be used for units running on an open RAN 5G network.

On October 27, 2020, AMD reached an agreement to acquire Xilinx in a stock-swap deal, valuing the company at $35 billion. The deal was expected to close by the end of 2021. Their stockholders approved the acquisition on April 7, 2021. The deal was completed on February 14, 2022. Since the acquisition was completed, all Xilinx products are co-branded as AMD Xilinx; started in June 2023, all Xilinx's products are now being consolidated under AMD's branding.In December 2020, Xilinx announced they were acquiring the assets of Falcon Computing Systems to enhance the free and open source Vitis platform, a design software for adaptable processing engines to enable highly optimized domain specific accelerators.

In April 2021, Xilinx announced a collaboration with Mavenir to boost cell phone tower capacity for open 5G networks. That same month, the company unveiled the Kria portfolio, a line of small form factor system-on-modules (SOMs) that come with a pre-built software stack to simplify development. In June, Xilinx announced it was acquiring German software developer Silexica, for an undisclosed amount.

VI. RESULTS



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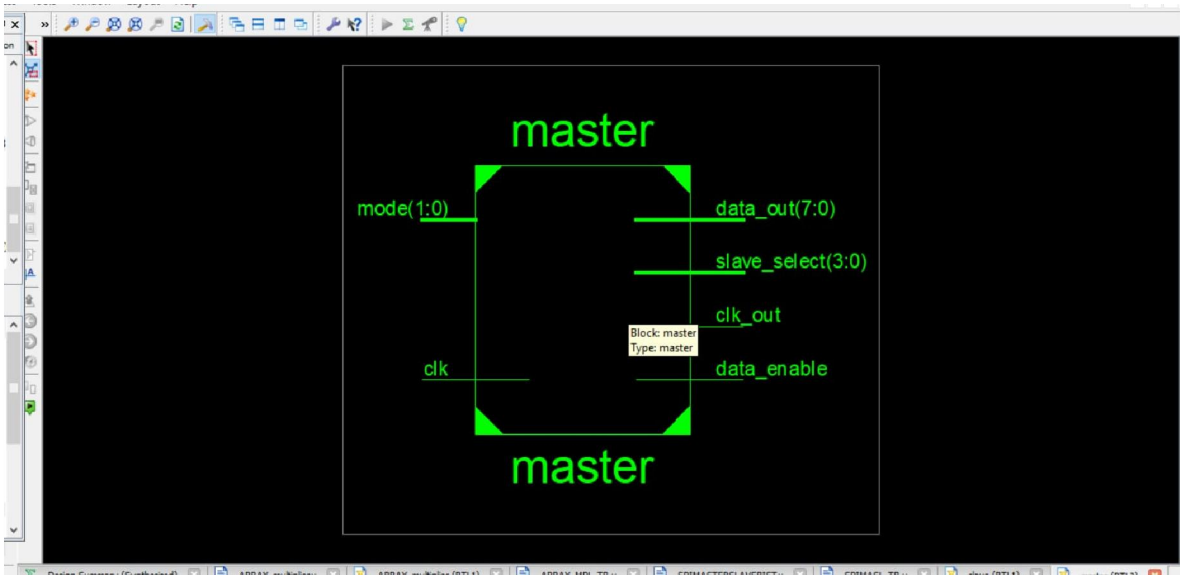

VII. CONCLUSION

SPI master-slave communication continues to be a cornerstone of embedded systems and digital electronics. This literature review has highlight the historical development, architecture, hardware, software, perform conceptualization, error handling, security, applications, comparative studies, and emerging trends in SPI communication. Ongoing research and development will undoubtedly shape its future, ensuring it's continue relevance in the world of digital communication. The classical SPI is locally defined; for instance, for monthly scale or running means, a drought event would begin when the precipitation amount is below its long-term average. However, the proposed method considers the local-time means of the precipitation series by fitting an upper and a lower envelope to precipitation data to obtain the SPI values, thus it explicitly assesses a dry (or wet) spell of weather. When we consider the climatology/meteorological features of precipitation and the physical geographical controls of the climate over Turkey, it is found that the proposed method is more capable of estimating the probability of dry or wet conditions for a station's monthly precipitation totals (or running means) than if the SPI values are obtained using the classical method

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