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Karatsubha Multiplier by using Verilog

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Abstract: *The Karatsuba multiplier is a widely-used algorithm that aims to efficiently multiply large numbers. Traditional multiplication algorithms have a time complexity of O(n^2), where n represents the number of digits in the input numbers. In contrast, the Karatsuba multiplier achieves a faster multiplication process by recursively splitting the numbers into smaller parts and performing intermediate multiplications using only three multiplications instead of four. This Modified architecture saves the 14.9% computation time and it consumes 45.5% less slices than existing Karatsuba multiplier. The proposed architecture has been simulated and synthesized by Xilinx vivado design suite for Spartan & Vertex device family. The new architecture is simple & easy. It emphasizes the significance of the Karatsuba multiplier in improving computational efficiency and highlights its implementation in different domains to accelerate large-scale multiplication tasks. Proposed hardware was implemented on different FPGA devices for various operand sizes, and performance parameters were determined. Comparing to state-of-theart works, the proposed method resulted in a lower combinational delay and area-delay product indicating the efficiency of design. In this we use two 32 bit inputs and produced the 64 bit as the output. In Spartan3E FPGA device family, Modified Karatsuba Algorithm (MKA) is 26.5% faster than Karatsuba Algorithm (KA).It consumes 61.7% less slices than existing KA based Convolution*.

Keywords: Crop recommendation, Humidity, Rainfall, pH, Machine Learning (ML), Random Forest (RF), Decision Tree (DT), Support Vector Machine (SVM), Logistic Regression (LR), and Naïve Bayes (NB),Data collection, Pre-processing, Feature extraction

I. INTRODUCTION

Karatsuba multiplier is the fast multiplication algorithm. It was the first method for computing products with sub-quadratic complexity. It was introduced by Anatolii Alexeevitch Karatsuba, a Russian mathematician, in 1960 and published in 1962. Modern applications in many cases used for VLSI implementations of the arithmetic modules in order to satisfy the high speed requirements. VLSI allows the designers to allocate complex systems consisting of several thousand or even millions transistors on one or very few chips. VLSI modules having Galois field multiplier can be classified into three categories: bit- serial multipliers , bit- parallel multipliers, and hybrid multiplier. Bit parallel architectures tend to be faster and only use combinational logic.

On the other hand, bit serial architectures require less area and uses registers in addition to combinational logic, and the hybrid multipliers, which are partially bit- serial and partially bit-parallel. Hybrid multipliers are faster than bit-serial ones, while their area is smaller than that of bit- parallel. For efficient VLSI implementation suitable hardware architecture is needed. It is obtained by using addition, multiplication, field operations, suitably in the architecture.

II.LITURATURE SURVEY

Tong Zhang and Keshab Parhi Zhang has contributed to machine learning and statistical signal processing, while Parhi is recognized for his work in digital signal processing and VLSI design. Both have made significant advancements, with Zhang focusing on optimization algorithms and Parhi on efficient hardware implementations. Their combined expertise had a substantial impact on advancing technology in these domains.Berlekamp.et.al.

In coding theory, he co-invented the Berlekamp–Massey algorithm, a key method for error correction in data transmission. His work significantly impacted digital communication and storage systems, ensuring reliable transmission of information.co-authoring the influential book "Winning Ways for Your Mathematical Plays." This

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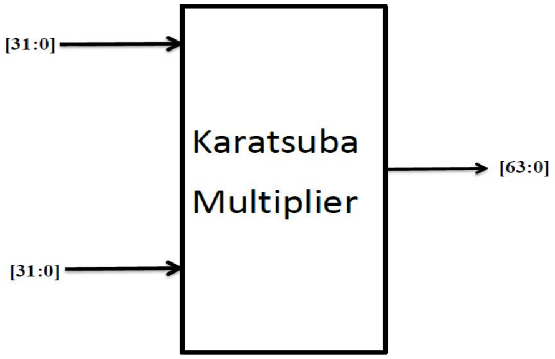
work explored mathematical strategies in various games, providing insights into optimal play.Throughout his career, Berlekamp held influential positions in academia and industry, contributing to the development of information and coding theory. A. Karatsuba and Y. Ofman karatsuba introduced the Karatsuba algorithm, a fast multiplication algorithm, in 1960. Their method significantly improves the efficiency of multiplying large numbers by dividing the problem into three smaller multiplications and a few additions, reducing the overall number of required multiplications. This divide-and-conquer approach enhances the algorithm's performance, particularly for large integers,the product of two numbers in terms of three multiplications instead of the traditional four.

III. VLSI(Very LargeScale Integration)

VLSI, or Very-Large-Scale Integration, refers to the process of integrating or embedding hundreds of thousands (and nowadays billions) of transistors on a single silicon semiconductor microchip. This technology paved the way for the production of advanced CPUs, memory chips, and custom ICs (integrated circuits) that are at the heart of today's electronic devices like computers, smartphones, and other gadgets. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

The VLSI era began in the 1970s and has gone through several phases of scaling down transistor sizes, allowing more and more functionality to be packed into smaller areas. As the size of transistors decreases (measured in nanometers, nm), more transistors can be placed on a chip, leading to more powerful and efficient electronic devices.The design and fabrication of VLSI chips involve several steps, including system design, circuit design, logic design, physical design, and finally manufacturing. The process requires a deep understanding of semiconductor physics, digital electronics, and design software. In essence, VLSI has been pivotal in the technological revolution, enabling the miniaturization and immense processing power of modern electronic devices.

IV. KARATSUBA MULTIPLIER

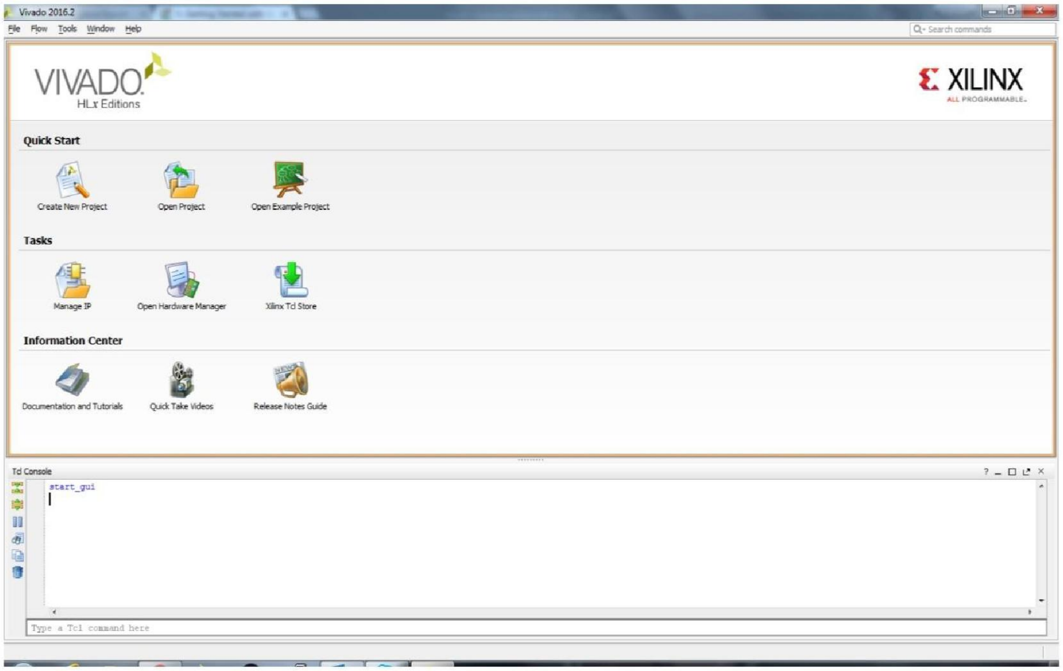


Multiplier takes [31:0] inputs which are multiplied using Karatsuba algorithm. General iterative method and Booths algorithm requires many iterations this increases hardware complexity and propagation delay. The delay of Booths algorithm is in the order of $(\log(n)^2)$. But Karatsuba algorithm follow divide and conquer methodology. Example : consider two 2 bit operands (a1,a0),(b1,b0) multiplication. By naïve approach we solve accordingly. a1 a0 * b1 b0 = (a1 a0)b0 + (a1 a0 0)b1. This require 4 time units but through Karatsuba algorithm we solve as $(a1b1)2^2 + (a1b0 + a0b1)2 + a0b0$

The Karatsuba algorithm is a fast multiplication algorithm. It was discovered by Anatoly Karatsuba in 1960 and published in 1962. It reduces the multiplication of two n-digit numbers to at most {n^{log _{2}3}approx n^{1.58}} single-digit multiplications in general . It is therefore asymptotically faster than the traditional algorithm, which requires n^{2} single-digit products.

V. SOFTWARE USED

Vivado is a software suite developed by Xilinx for designing and implementing digital systems on field-programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs). It provides a comprehensive environment for hardware development, encompassing synthesis, implementation, and debugging stages in the FPGA design process.



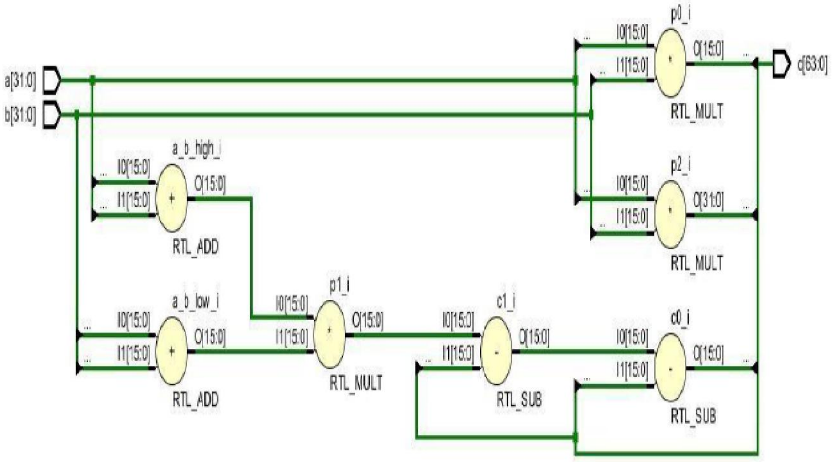
```
start_gui
```

One key feature of Vivado is its high-level synthesis (HLS) capability, enabling designers to describe functionality in C, C++, or SystemC, which is then automatically converted into hardware description language (HDL) code. This accelerates the design process and facilitates algorithmic-level optimizations. Vivado supports a wide range of Xilinx FPGAs and includes advanced tools for system integration, IP (Intellectual Property) integration, and real-time debugging. The software also offers features like partial reconfiguration, allowing users to dynamically modify specific regions of an FPGA while the rest of the system remains operational.

Its intuitive graphical user interface (GUI) simplifies the design flow, making it accessible to both novices and experienced FPGA developers. With ongoing updates and enhancements, Vivado continues to be a leading tool in the field of FPGA development, empowering engineers to create efficient and high-performance digital systems

VI. RESULT

RTL SCHEMATIC



RTL Schematic Diagram

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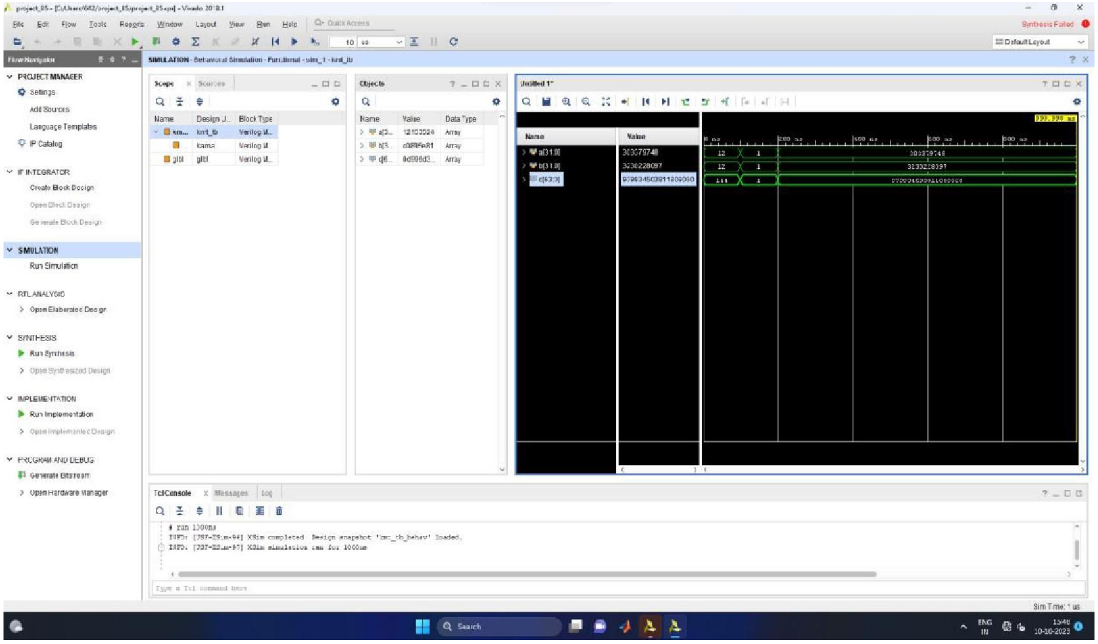
SIMULATION RESULT:



```
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'krst_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

VII. CONCLUSION

The Karatsuba algorithm is a fast multiplication technique that divides numbers into smaller parts, recursively multiplies those parts, and combines the results to achieve multiplication. Its conclusion is that it can significantly reduce the number of arithmetic operations required for large number multiplication, making it more efficient than traditional methods like long multiplication, especially for very large numbers. However, the algorithm does have a certain threshold beyond which traditional methods become more efficient due to the overhead of recursive calls and addition operations. Overall, the Karatsuba multiplier has greatly contributed to the field of multiplication algorithms by offering a more efficient alternative to traditional methods, making calculations involving large numbers more manageable and time-effective.

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