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Design of Smart Traffic Signal using Verilog

Shaheen[1], A. Supriya[2], B. Keerthana[3], B. Srivani[4], Ch. Ajay[5]
Assistant Professor, Dept. of Electronics & Communication Engineering[1]
UG Students, Dept. of Electronics & Communication Engineering[2,3,4,5]
Christu Jyothi Institute of Technology & Science, Jangaon, Telangana, India

Abstract: *Traffic light control can be designed as synchronous sequential machine with finite number of states. Explicit finite state model is used to design the necessary coding for control system using Verilog HDL. The machine is modeled with only six states necessary delay is provided and for that particular delay the necessary traffic lights are set ON and OFF. For illustration just only two roads Chosen and control algorithm controls the traffic lights of that roads proposes a flexible framework which provides a particular delaying particular using click divider, also discusses the issues of modeling the state machine in a synthes is friendly manner.*

The proposed system aims to optimize traffic flow and reduce congestion by dynamically adjusting signal timings based on real-time traffic data. The design includes modules for vehicle detection, data processing, and signal control. By utilizing Verilog's capabilities, the system achieves efficient and accurate signal management, enhancing over all traffic management and contributing to safer and more stream lined urban mobility..

Keywords: Verilog HDL

I. INTRODUCTION

A smart traffic signal implemented in Verilog represents an advanced approach to traffic management, leveraging digital design principles to optimize signal timings and enhance overall traffic flow. In this innovative design, the Verilog hardware description language is employed to create a responsive and adaptive traffic signal controller capable of dynamically adjusting its behavior based on real-time conditions.

At the core of this Verilog implementation is a state machine that governs the transition between different signal states, such as red, yellow, and green. The state transitions are orchestrated by a clock signal, ensuring synchronization and precision in signal changes. Additionally, a reset input is incorporated to handle initialization and system reset scenarios.

To introduce adaptability, the smart traffic signal incorporates a traffic sensor input. This sensor serves as a key component enabling the system to react to the actual traffic conditions on the road. When the sensor detects congestion or increased traffic, it triggers a state transition in the Verilog state machine, dynamically shortening the signal timings to alleviate congestion and enhance traffic flow.

The Verilog code includes parameters defining default and shortened waiting times for each signal state. These parameters allow for easy adjustment to meet specific traffic management requirements. By employing a parameterized approach, the Verilog implementation remains flexible and adaptable to varying scenarios and urban planning needs.

This smart traffic signal design showcases the power of digital logic in creating intelligent, responsive infrastructure. Beyond the traditional fixed-timing traffic signals, this Verilog implementation contributes to more efficient and adaptive traffic control systems, ultimately contributing to reduced congestion, improved safety, and enhanced overall urban mobility. As technology continues to evolve, Verilog-based designs offer a pathway to smarter and more responsive urban infrastructure, aligning with the broader goals of smart cities and intelligent transportation systems.

II. LITERATURE REVIEW

The design of smart traffic signals using Verilog has gained attention in the literature as researchers and engineers explore innovative solutions to enhance urban traffic management. Existing literature reveals a focus on adapting traditional traffic signal control methods using Verilog to create intelligent, adaptive systems.

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Intelligent Transportation Systems (ITS) applications for traffic signals – including communications systems, adaptive control systems, traffic responsive, real- time data collection and analysis, and maintenance management systems – enable signal control systems to operate with greater efficiency. Sharing traffic signal and operations data with other systems will improve overall transportation system performance in freeway management, incident and special event management, and maintenance/failure response times. Some examples of the benefits of using ITS applications for traffic signal control include: Updated traffic signal control equipment used in conjunction with signal timing optimization can reduce congestion.

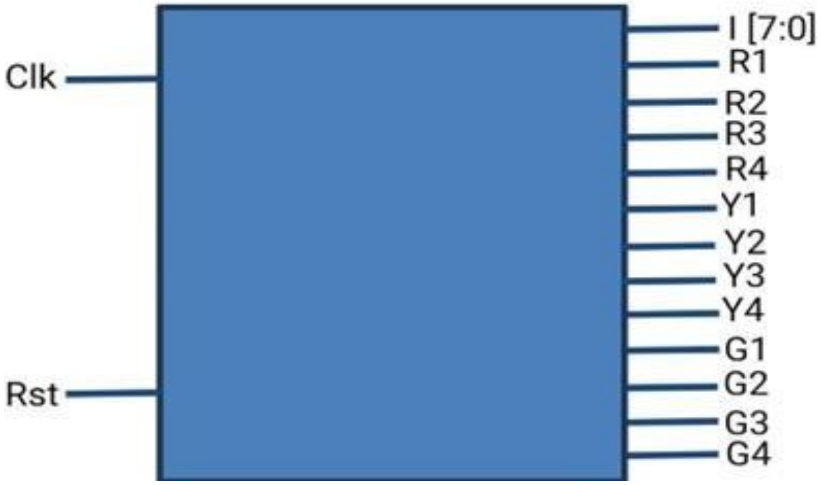
III. VLSI (VERY LARGE SCALE INTEGRATION)

Very Large Scale Integration (VLSI) is a pivotal field in electronic engineering that involves the design and fabrication of integrated circuits (ICs) with an exceptionally high number of transistors on a single chip. As of 2002, VLSI technology had evolved to pack millions, and even billions, of transistors into a single chip, enabling the creation of complex and powerful electronic systems.

The advancements in VLSI have been instrumental in the miniaturization of electronic devices, leading to increased computational power, energy efficiency, and functionality. The year 2002 witnessed the ongoing trend of Moore's Law, predicting a doubling of transistor density approximately every two years, continuing to drive innovation and performance improvements in VLSI.VLSI applications span a wide range, from microprocessors and memory chips to application-specific integrated circuits (ASICs) tailored for specific functions. The collaborative efforts of researchers, engineers, and semiconductor manufacturers contributed to the development of cutting-edge VLSI technology, shaping the landscape of modern electronics.

In the year 2002 marked a significant phase in VLSI, with a relentless pursuit of increased transistor density and miniaturization, driving advancements that profoundly impacted the capabilities of electronic systems and devices.

IV. BLOCK DIAGRAM OF SMART TRAFFIC CONTROL



Traffic lights are integral part of modern life. Their proper operation can spell the difference between smooth flowing traffic and four-lane gridlock. Proper operation entails precise timing, cycling through the states correctly, and responding to outside inputs. The traffic light controller is designed to meet a complex specification. That specification documents the requirements that a successful traffic light controller must meet. It consists of an operation specification that describes the different functions the controller must perform, a user interface description specifying what kind of interface the system must present to users, and a detailed protocol for running the traffic lights. Each of these requirements sets imposed new constraints on the design and introduced new problems to solve. The controller to be designed controls the traffic lights of a busy highway (HWY) intersecting a side road (SRD) that has relatively lighter traffic load. Figure 1.1 shows location of the traffic lights. Sensors at the intersection detect the presence of cars on highway and side road.

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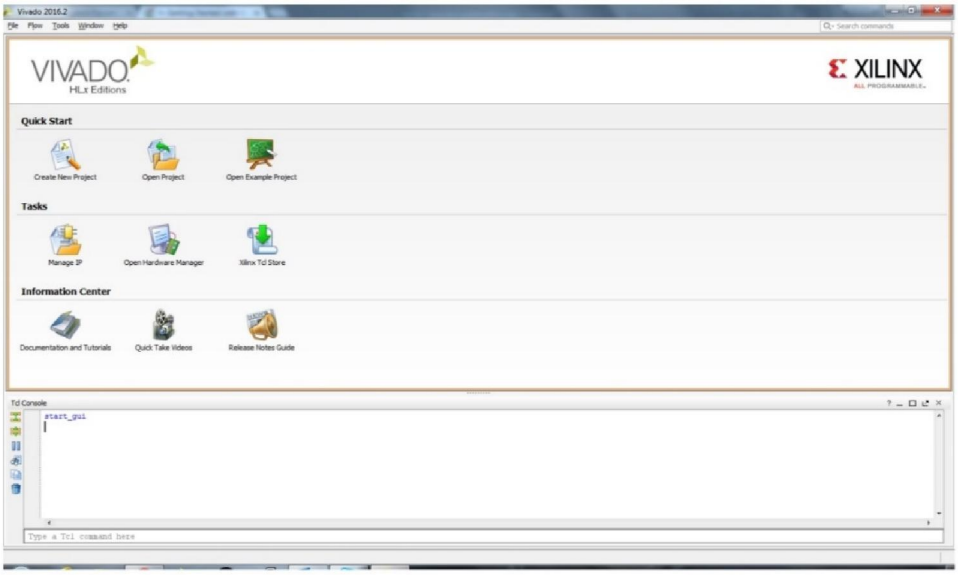
V. SOFTWARE USED

Vivado is a software suite developed by Xilinx for designing and implementing digital systems on field-programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs). It provides a comprehensive environment for hardware development, encompassing synthesis, implementation, and debugging stages in the FPGA design process.

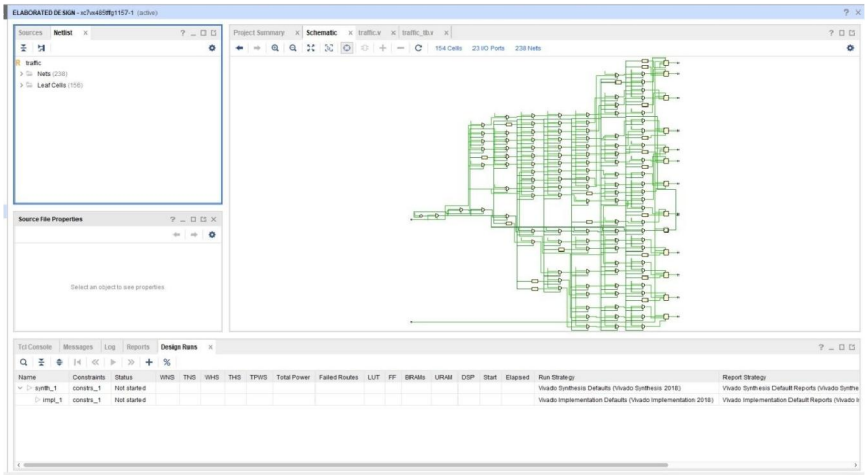


One key feature of Vivado is its high-level synthesis (HLS) capability, enabling designers to describe functionality in C, C++, or SystemC, which is then automatically converted into hardware description language (HDL) code. This accelerates the design process and facilitates algorithmic-level optimizations. Vivado supports a wide range of Xilinx FPGAs and includes advanced tools for system integration, IP (Intellectual Property) integration, and real-time debugging. The software also offers features like partial reconfiguration, allowing users to dynamically modify specific regions of an FPGA while the rest of the system remains operational.

Its intuitive graphical user interface (GUI) simplifies the design flow, making it accessible to both novices and experienced FPGA developers. With ongoing updates and enhancements, Vivado continues to be a leading tool in the field of FPGA development, empowering engineers to create efficient and high-performance digital systems.

V. RESULTS

RTL SCHEMATIC



RTL Schematic Diagram

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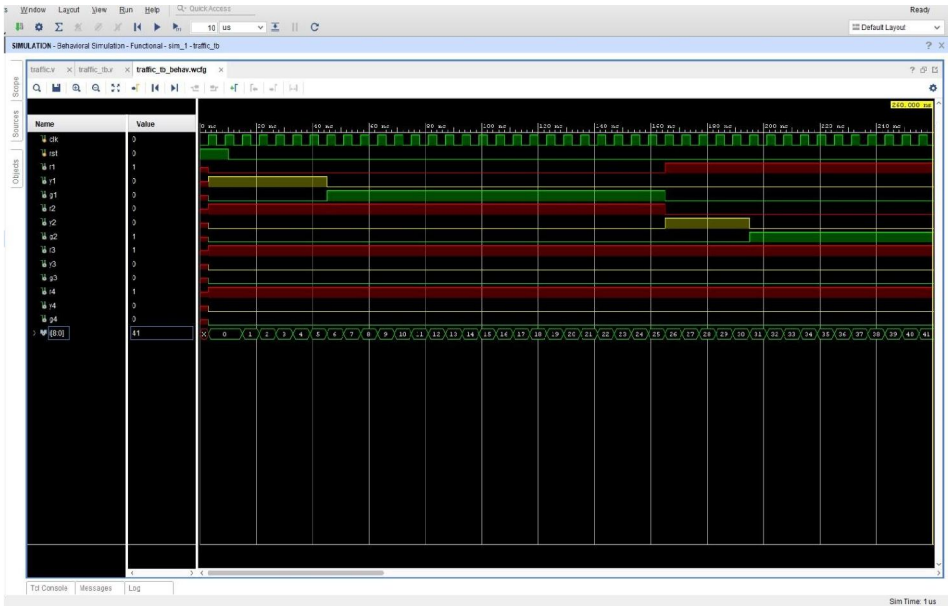
SIMULATION RESULTS:



VI. CONCLUSION

An FPGA design of TLC with six traffic lights has been simulated using Quartus II, implemented and tested using ALTERA FLEX10K chip. One of the advantage of this design over the existing method is the waiting time of driver during off-peak hour has been reduced, means that the normal design cycle (using fixed-time technique) has been reduced notably, thus ameliorate reliability and flexibility of the TLC.

An FPGA design of a 24-hour traffic light controller system of a twelve roads structure with six traffic lights has been simulated, implemented and tested. The system has been designed using VHDL, and implemented on hardware using XILINX Spartan 3E and Virtex 5xc5vlx110t FPGA kit. The functionality of this design can be easily enhanced.

Some of these functions are to control more than 6 traffic lights. Also, to allow the user to assign the time for each traffic light (i.e., minimum time to be Green), adding more sensors on each road to count the number of cars in each road and check for the longer queue to increase the timer for that road. Here we have manually entered the signals for the NS car and EW car since the sensor interfacing is not done at yet manually entered the signals for the Ns car and EW cars in the sensor interfacing is not done yet which remains as future scope as well as the camera interfacing which will detect if any car breaks the traffic rule serve as a security purpose and emergency services.

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