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Subway Automatic Ticket Booking System using Verilog

Y Sreeja[1], A Nikhitha[2], M Sruthi[3], P Kamalakar[4], D Bhargav[5]
Assistant Professor, Dept. of Electronics & Communication Engineering[1]
UG Students, Dept. of Electronics & Communication Engineering[2,3,4,5]
Christu Jyothi Institute of Technology & Science, Jangaon, Telangana, India

Abstract: *Using Verilog HDL language to research a subway automatic ticket booking system. The design of this subway ticketing system takes convenience, quickness and simplicity as the core, and takes saving time for passengers. It completes the main process of buying subway tickets for passengers. Firstly, this project studies the development of subway ticketing system at home and abroad, and then studies the basic components of subway ticketing system. The paper also simulates the ticket selection module, change processing module and display interface module on Xilinx Vivado. In the Verilog design, finite state machines (FSMs) are employed to model the various states of the ticket booking process. These FSMs ensure smooth transitions between states, enabling the system to handle scenarios such as ticket availability checks, payment processing, and generating tickets. Additionally, the communication interface is responsible for securely transmitting booking information to the subway network, ensuring seamless integration with the overall subway infrastructure.*

Keywords: Verilog HDL

I. INTRODUCTION

The subway automatic ticket booking system using Xilinx Vivado is a cutting-edge solutionthat aims to streamline the ticketing process for subway systems. By leveraging the power of XilinxVivado, this system provides an efficient and reliable way for commuters to purchase tickets seamlessly. Through its hardware implementation, it offers fast processing, secure transactions, andreal-time updates, enhancing the overall subway experience for passengers. In this system, Xilinx Vivado plays a crucial role in ensuring the smooth operation of the ticket booking process,showcasing the integration of advanced technology to revolutionize urban transportation.

The hardware-based system can collect and analyze passenger data, offering insights into travel patterns, peak hours, and popular routes, which can aid in optimizing subway operations. Xilinx Vivado offers high-performance hardware acceleration, enabling quick and efficient processing of ticket transactions, leading to reduced waiting times for commuters. In the Verilog design, finite state machines (FSMs) are employed to model the various states of the ticket bookingprocess. These FSMs ensure smooth transitions between states, enabling the system to handle scenarios such as ticket availability checks, payment processing, and generating tickets. Additionally, the communication interface is responsible for securely transmitting booking information to the subway network, ensuring seamless integration with the overall subway infrastructure. The implementation also incorporates security measures to safeguard sensitive user data and payment information. Encryption techniques are employed to protect data during transmission and storage, while authentication mechanisms prevent unauthorized access to the ticketing system. By adopting these security measures, the Verilog-based subway ticket booking system prioritizes user privacy and data integrity

Technologies used:

In this project, we are designing an Intelligent Transport System (ITS) application for Subway Automatic Ticket Booking System using Verilog by using Field Programmable Gate Array(FPGA). FPGA have been used for a wide range of applications. After the introduction of the FPGA, the field of programmable logic has expanded exponentially. Due to its ease of designand maintenance, implementation of custom-made chips has shifted. The integration of FPGA andall

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thesmall devices will be integrated by using Very Large-Scale Integration (VLSI). The code is writtenin Verilog HDL design pattern and synthesis is done in XILINX of version 14.5. Thus,the major technologies used in this project are:

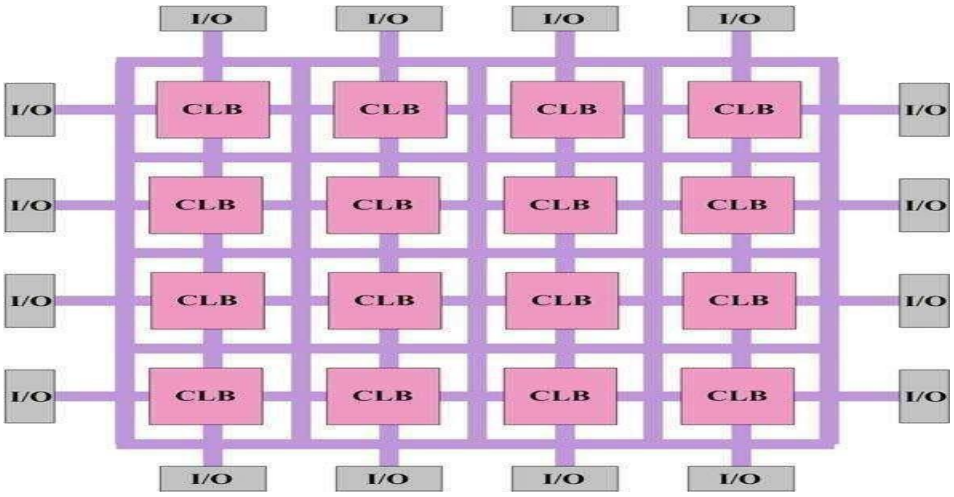
- FPGA
- VLSI
- Verilog HDL
- XILINX 14.5 version

FPGA

Field Programmable Gate Arrays (FPGAs) were first introduced almost two and a half decades ago. Since then, they have seen a rapid growth and have become a popular implementation media for digital circuits. The advancement in process technology has greatly enhanced the logic capacity of FPGAs and has in turn made them a viable implementation alternative for larger and complex designs. Further, programmable nature of their logic and routing resources has a dramatic effect on the quality of final device's area, speed, and power consumption.

This chapter covers different aspects related to FPGAs. First of all, an overview of the basic FPGA architecture is presented. An FPGA comprises of an array of programmable logic blocks that are connected to each other through programmable interconnect network. Programmability in FPGAs is achieved through an underlying programming technology. This chapter first briefly discusses different programming technologies. Details of basic FPGA logic blocks and different routing architectures are then described.[2]

The programmable logic and routing interconnect of FPGAs makes them flexible and general purpose but at the same time it makes them larger, slower and more power consuming than standard cell ASICs. However, the advancement in process technology has enabled and necessitated a number of developments in the basic FPGA architecture. These developments are aimed at further improvement in the overall efficiency of FPGAs so that the gap between FPGAs and ASICs might be reduced. These developments and some future trends are presented in the lastsection of this chapter.[2]



Overview of FPGA architecture

VLSI

Very-Large-Scale Integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s whencomplex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips haveincreased in complexity into the hundreds of millions of transistors.[3]

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VLSI stands for "Very Large-Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas.[3]

- Simply we say Integrated circuit is many transistors on one chip.
- Design/manufacturing of extremely small, complex circuitry using modified semiconductormaterial.
- Most electronic logic devices.

II. VLSI DESIGN FLOW

Design is the most significant human endeavor: It is the channel through which creativity is realized. Design determines our every activity as well as the results of those activities; thus, it includes planning, problem solving, and producing. Typically, the term “design” is applied to the planning and production of artifacts such as jewelry, houses, cars, and cities. Design is also found in problem-solving tasks such as mathematical proofs and games. Finally, design is found in pure planning activities such as making a law or throwing a party.

A semiconductor process technology is a method by which working circuits can be manufactured from designed specifications. There are many such technologies, each of which creates a differentenvironment or style of design.

VERILOG HDL

A typical Hardware Description Language (HDL) supports a mixed-leveldescription in which gate and netlist constructs are used with functional descriptions. This mixed-level capabilityenables you to describe system architectures at a high level of abstraction, then incrementally refinea design’s detailed gate-level implementation.[4]

XLINUX

Steps To Open Vivado Software: -

1. Launching Vivado

Open the start menu on the desktop shortcut created during the installation process

2. The Start Page

This is the screen that displays after Vivado starts up. The buttons are described below using theimageas guide.

3. Creating a New Project

4. The Project Manager

5. Creating a Verilog Source File

6. Creating a Verilog Test bench

III. THE FINITE STATE MACHINE

The FSM-Finite State Machine is the heart of traffic light controller. It responds to the input signals processed by the input handling module and provides the output and control signals neededto make the system function. This design uses a standard two process finite state machine where oneprocess is used to change states on every clock cycle while the other process is used to combinatorically calculate what the next state should be based on the current inputs and the current state.

The FSM has four main groups of states corresponding to the four modes in which the traffic lightcontroller can operate. The read function causes the controller to enter the memory read state. Oncein that state, the system remains there until reset, using whatever value is on the timing parameter selection switches for the RAM address. The memory read state also ensures that writeenable for theRAM is disabled since the system is only trying to read previously stored values in RAM.

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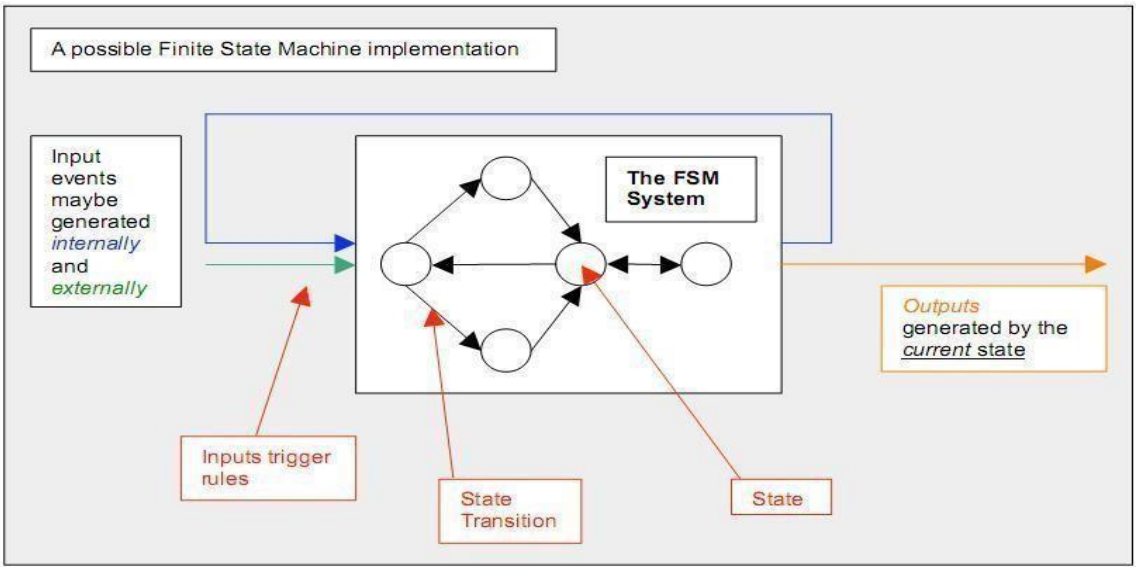
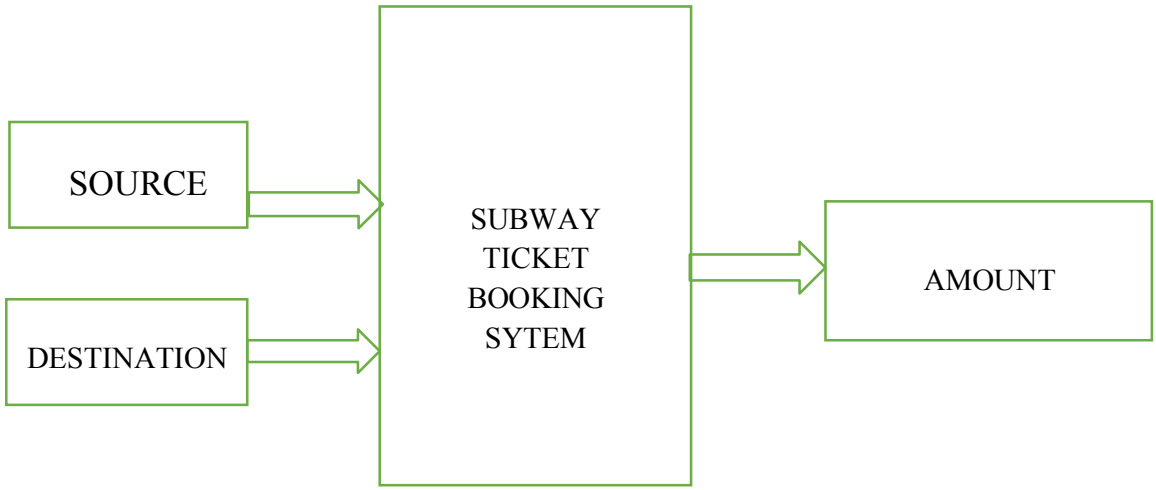


Finite State Machine

The second major state group corresponds to the memory write function. In this mode, theFSM transitions to the memory write state and then returns to the start state. One crucial feature of this design is that the system is only in the memory write state for one cycle; thus, the RAM write enable is never high for more than a single clock cycle.

Block diagram of Automatic Ticket booking System



Block Diagram

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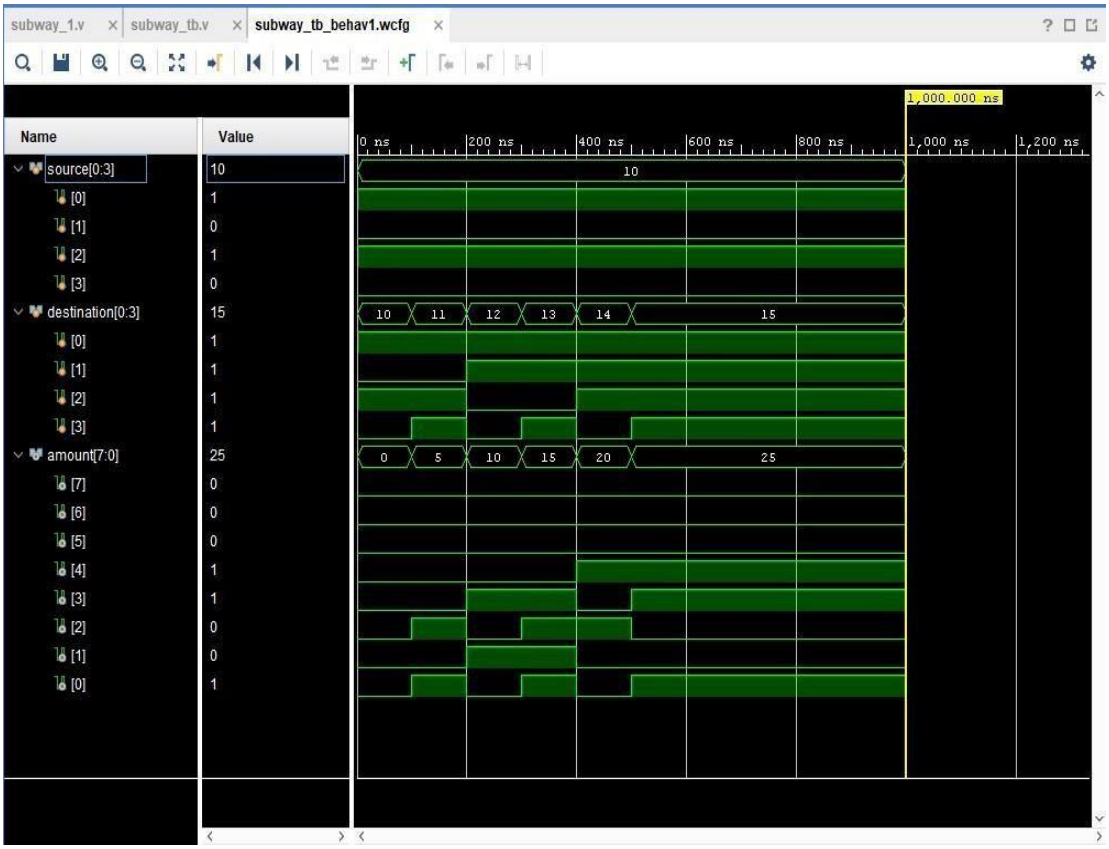
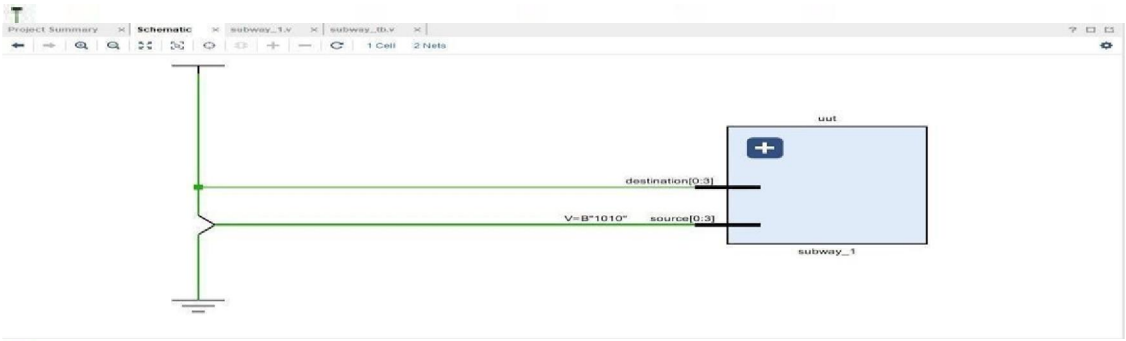
IV. RESULT AND DISCUSSION



A Subway Automatic Ticket Booking System implemented using Verilog is like a smart machine that helps people buy tickets for subway rides. Verilog is a special computer language used to program electronic devices.
In this system, when a passenger wants to purchase a subwayticket, they interact withthe machine by pressing buttons or touching a screen. The Verilog algorithm inside the machine processes their choices and calculates the fare. This process is quick and efficient, making it easy for people to get their subway tickets without the need for human intervention. It's like a digital ticket vending machine that simplifies the ticket-buying process for subway passengers.

RTL Schematic diagram



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V. CONCLUSION

The development of a Subway Automatic Ticket Booking System using Verilog has provento be a promising venture. Verilog, a hardware description language, has enabled the creation ofa robust and efficient system for handling ticket transactions in subway networks. This project offersa reliable and automated solution for commuters, streamlining the ticketing process and reducing human error. By implementing Verilog, we have successfully designed a system that can accurately process ticket requests, calculate fares, and issue tickets in real-time. Overall, this technology not only enhances the user experience but also sets the stage for future advancements in subway ticketing systems, making public transportation more convenient and efficient

- The subway automatic ticket booking system using Verilog provides a convenient and efficient solution for passengers.
- Verilog-based design ensures accurate ticket booking.
- The system can be further enhanced and customized to meet the evolving needs of subway transportation.

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