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BIST (Built-In Self Test) Memory by Using VERILOG

B. Hanumanthu[1], N. Sathvika[2], A. Manikanta[3], A. Praveen[4], Ch. Abhiram[5]
Assistant Professor, Department of Electronics & Communication Engineering[1]
UG Student, Department of Electronics & Communication Engineering[2,3,4,5]
Christu Jyothi Institute of Technology & Science, Jangaon, Telangana, India

Abstract: *Built-In Self-Test (BIST) is a technique that allows a set up to check itself for any error on its own. BIST is a screening mechanism that places the testing functions physically with the circuit applications where system reliability is predominant, and "failure is not an option." The decision to execute a critical mission must be made only if the complete system is running without any error. BIST structures generate pseudo random combinations and output results for an exclusive circuit under test are compared. BIST can be implemented on entire designs, design blocks or structures within design blocks. Memory is a complex architecture (fabrication wise) and used in a large number of applications. BIST is basically used to help in the testing of memory with the help of a few extra pins. In fact, while testing a memory using BIST, applying a simple clock signal along with a few pins helps test the entire memory IC. The proposed BIST enabled RAM is designed using Verilog*

Keywords: Built-In Self Test

I. INTRODUCTION

The introduction to Built-In Self Test (BIST) for memory using Verilog sets the stage for understanding the critical role of self-test capabilities in enhancing the reliability and efficiency of memory testing within digital systems. This dynamic field of research addresses challenges in ensuring the integrity of memory subsystems, crucial components of electronic devices.Memory testing is a pivotal aspect of system verification, ensuring that memories operate flawlessly under diverse conditions. BIST emerges as a compelling solution, integrating testing mechanisms within the memory itself. This approach, facilitated by hardware description language such as Verilog, aims to automate and streamline the testing process, reducing the reliance on external testing equipment and minimizing test time. Academic contributions to this field are highlighted, with IEEE journals and conferences like the Design Automation Conference (DAC) and Design, Automation and Test in Europe (DATE) serving as key platforms for knowledge dissemination.

II. LITERATURE SURVEY

A literature survey on Built-In Self Test (BIST) for memory using Verilog reveals a diverse landscape of research efforts aimed at improving the reliability and efficiency of memory testing. Scholars have explored various aspects, ranging from test pattern generation to fault simulation and optimization of Verilog-based BIST methodologies.Test pattern generation stands out as a crucial element in memory testing. Researchers have proposed automated techniques within the Verilog framework to generate comprehensive test patterns. These patterns aim to thoroughly exercise memory cells and associated circuitry, ensuring effective identification of a wide array of faults. The focus is on creating patterns that stress the system under diverse conditions, enhancing the robustness of the testing process.

Fault simulation in Verilog is another key area of investigation. Studies delve into the accuracy and efficiency of Verilog-based fault simulation models in predicting the behavior of faulty memory circuits. Researchers simulate various fault types, such as stuck-at faults, bridging faults, and resistive faults, to assess the capability of these models in pinpointing potential issues within the memory.The impact of Verilog-based BIST on memory testing efficiency is a recurring theme in the literature. Researchers examine how the integration of BIST techniques influences test time, resource utilization, and overall testing cost. Optimizations in Verilog code are proposed to streamline the BIST process, ensuring a balance between comprehensive memory testing and efficient resource usage.

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The academic community has actively contributed to this field, with IEEE journals serving as a prominent platform for disseminating research findings. Conferences such as the Design Automation Conference (DAC) and Design, Automation and Test in Europe (DATE) have facilitated knowledge exchange among researchers, fostering collaborative efforts to advance Verilog-based BIST methodologies.

III. VLSI (Very Large Scale Integration)

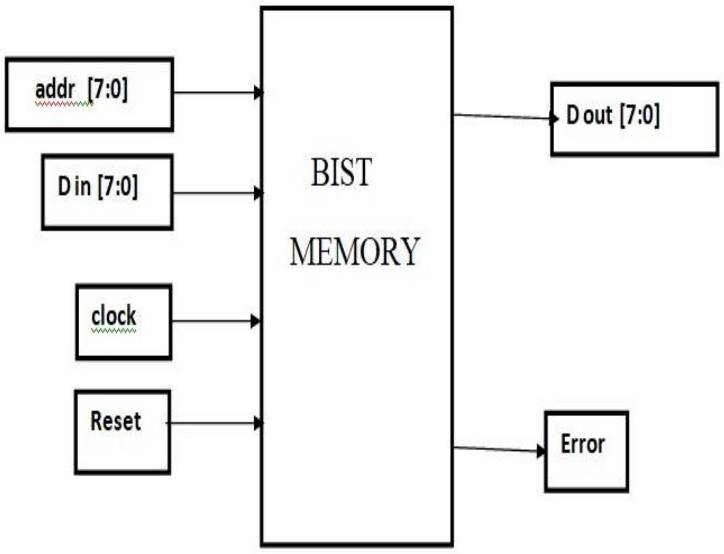
Very Large Scale Integration (VLSI) is a pivotal field in electronic engineering that involves the design and fabrication of integrated circuits (ICs) with an exceptionally high number of transistors on a single chip. As of 2002, VLSI technology had evolved to pack millions, and even billions, of transistors into a single chip, enabling the creation of complex and powerful electronic systems.

The advancements in VLSI have been instrumental in the miniaturization of electronic devices, leading to increased computational power, energy efficiency, and functionality. The year 2002 witnessed the ongoing trend of Moore's Law, predicting a doubling of transistor density approximately every two years, continuing to drive innovation and performance improvements in VLSI.VLSI applications span a wide range, from microprocessors and memory chips to application-specific integrated circuits (ASICs) tailored for specific functions. The collaborative efforts of researchers, engineers, and semiconductor manufacturers contributed to the development of cutting-edge VLSI technology, shaping the landscape of modern electronics.

In the year 2002 marked a significant phase in VLSI, with a relentless pursuit of increased transistor density and miniaturization, driving advancements that profoundly impacted the capabilities of electronic systems and devices.

IV. BIST (Built-In Self Test) MEMORY

Built-in Self Test (BIST) is a crucial technique in VLSI (Very Large Scale Integration) design for ensuring the reliability and functionality of integrated circuits. It involves embedding self-testing capabilities within the chip, allowing it to diagnose and report faults without external test equipment. In VLSI, BIST employs dedicated circuitry that performs comprehensive tests on different components of the chip, such as logic gates and memory cells. This self-contained testing mechanism reduces the need for external testing, minimizing production costs and enhancing overall system efficiency. BIST operates during the startup phase or intermittently during normal operation, running diagnostic tests to identify faults like stuck-at faults or bridging faults.



This self-testing approach is particularly valuable in applications where continuous uptime is critical, such as in aerospace, medical devices, or automotive systems. By integrating BIST into VLSI designs, engineers can enhance the reliability and longevity of electronic systems, contributing to the overall robustness of modern semiconductor devices.

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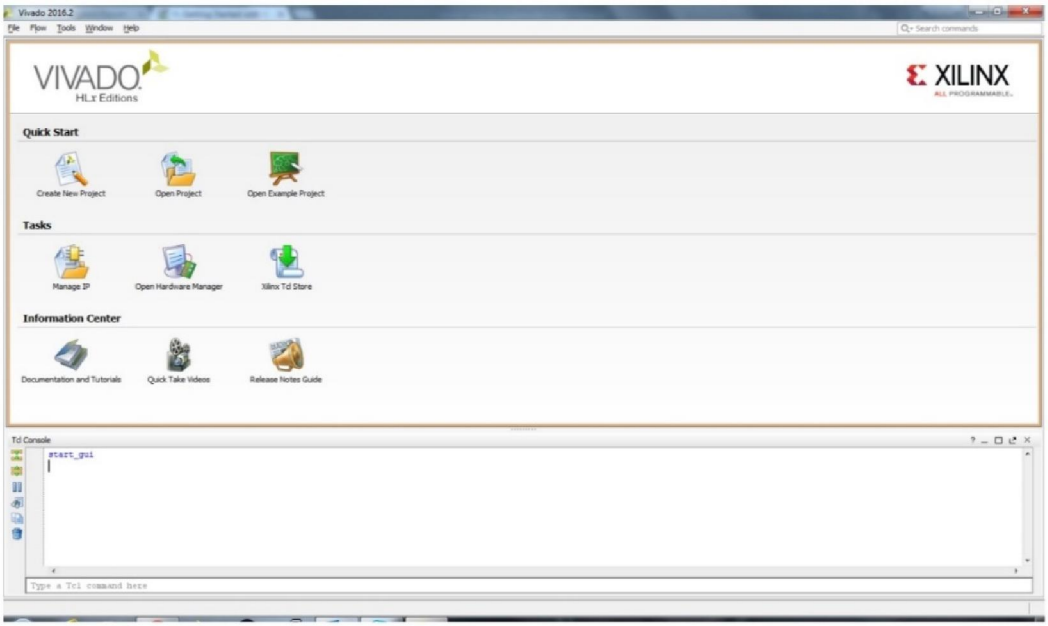
V. SOFTWARE USED

Vivado is a software suite developed by Xilinx for designing and implementing digital systems on field-programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs). It provides a comprehensive environment for hardware development, encompassing synthesis, implementation, and debugging stages in the FPGA design process.

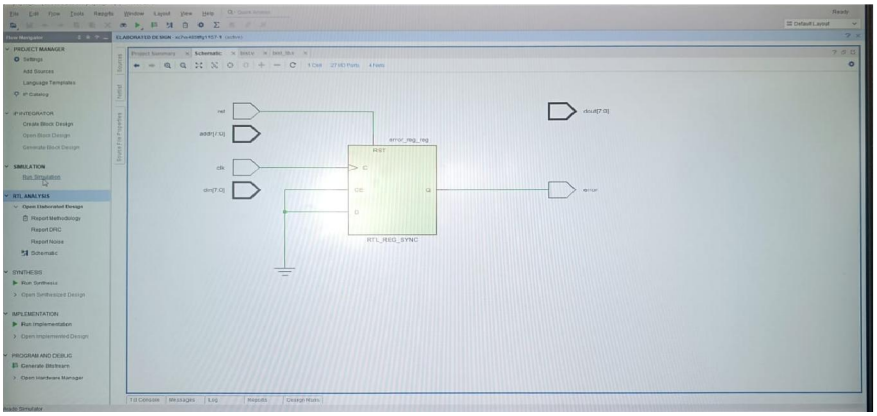
One key feature of Vivado is its high-level synthesis (HLS) capability, enabling designers to describe functionality in C, C++, or SystemC, which is then automatically converted into hardware description language (HDL) code. This accelerates the design process and facilitates algorithmic-level optimizations. Vivado supports a wide range of Xilinx FPGAs and includes advanced tools for system integration, IP (Intellectual Property) integration, and real-time debugging. The software also offers features like partial reconfiguration, allowing users to dynamically modify specific regions of an FPGA



Its intuitive graphical user interface (GUI) simplifies the design flow, making it accessible to both novices and experienced FPGA developers. With ongoing updates and enhancements, Vivado continues to be a leading tool in the field of FPGA development, empowering engineers to create efficient and high-performance digital systems.

VI. RESULTS

RTL SCHEMATIC



RTL Schematic Diagram

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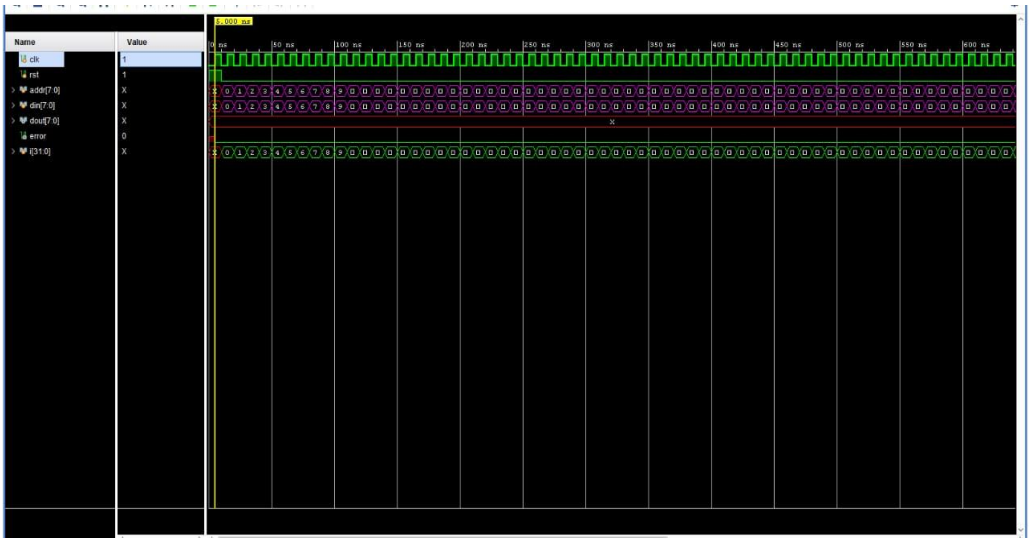
SIMULATION RESULTS:



VII.CONCLUSION

In conclusion, implementing Built-In Self Test (BIST) for memory using Verilog provides a powerful solution for ensuring the reliability and functionality of memory components within digital systems. Verilog, a hardware description language, facilitates the design and integration of BIST mechanisms seamlessly into the memory architecture.BIST for memory allows for self-testing without the need for external test equipment, reducing dependency on external testing resources. This results in more efficient and cost-effective testing processes during both manufacturing and in-field operation. Verilog's ability to describe complex hardware behavior enables the creation of robust and efficient BIST controllers that can perform thorough tests on memory arrays.

Moreover, Verilog-based BIST implementations enhance the fault coverage by detecting and diagnosing various faults within the memory, including stuck-at faults, transition faults, and coupling faults. This ensures a higher level of reliability in the overall system. The modularity and scalability of Verilog contribute to the adaptability of BIST techniques to different memory configurations and sizes.

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