IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.301
Volume 3, Issue 12, May 2023

# Design A Simulation An Asymmetrical 11-level Inverter for Photovoltaic Applications

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**Abstract:** *Multilevel converters are becoming more popular as a way to get around the power rating restrictions in traditional power conversion techniques as a result of rising needs for power conversion technology. Although the focus of this work is on a novel asymmetrical construction of an 11-level inverter, a few comparisons with the traditional topological structure will be made. Limitations in the topologies of conventional types frequently relate to their complexity and volume. Further discussion will focus on how the 11-level inverter's asymmetrical topology deals with these constraints, gets around them, and reduces harmonic distortions for grid-tied PV systems. MATLAB software is used to design and simulate the suggested build. A THD value is produced through real-time simulation analysis of the proposed design.*

**Keywords:** 11-level Inverter, Photovoltaic Application, Electric Current, Power Electronics Circuits

## I. INTRODUCTION

Modern application conversion systems are built around power electronics. The growing need to increase efficiency and usage flexibility creates technical hurdles with regard to the topologies and control methods that are employed. The power ratings and handling restrictions of multilevel inverters could be bypassed by sharing through ratings in the switches' component parts. These converter trends are primarily used with industrial equipment and renewable technologies. Since the PV cells' output is DC, the MPPT maximises the DC power output. For use as a source in domestic and commercial appliances, DC electricity is transformed into AC. The power ratings of the components that make up conventional inverter architectures are limiting.

In order to share and distribute power through the components, multilevel conversion techniques are used. The flying capacitor topology and the diode-clamp design are the two topologies that are most well-known. However, when levels rise, so do the volume, price, and switch count. Asymmetrical designs typically achieve this goal, and with higher levels, harmonic distortions, whose nominal percentages are controlled by IEEE standards in output power, are lessened. The main goal of this is to design a multilevel inverter that can operate as a seven level inverter and naturally splits the power conversion into a higher voltage lower frequency inverter and a lower voltage higher frequency inverter by cascading two three-phase three-level inverters using the load connection and only one dc voltage source.

This study suggests a novel, asymmetrical 11-level inverter architecture that is simulated with PSIM by PowerSimTech in order to address the traditional constraints of inverters. The suggested inverter circuit architecture and switching operations will be explored in more detail in Section II.The proposed 11-level inverter design would be able to overcome traditional topology issues by utilising a smaller number of switches to achieve a high number of n-levels, and the paper will also discuss how this design could be helpful for future research in higher n-level applications to further reduce harmonic values.

## II. INVERTER DESIGN AND OPERATION

### Circuit Design Configuration

Figure. 1 depicts the 11-Level Inverter's design. A(S1-S4) and B(S5-S8), the inverter's two primary stages, each play a distinct part in the suggested inverter operating principle. Stage B(S5-S8) is used to switch the polarity of the inverter's Stage A(S1-S4) DC output, producing an n-level AC output for grid-tied PV systems. Stage A(S1-S4) is used to configure and create the number of n levels (11-level in the proposed design) in the asymmetric inverter. Stage A (S1-

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S4) is directly connected to the DC power source in this proposed 11-level inverter design. The DC source configuration is split into 3 isolated DC sources, each of which has a nominal value of configured E, 2E, and 2E, meaning that the constructor determines the definition value in DC voltage of E while the switches are series type, power ratings are still taken into consideration

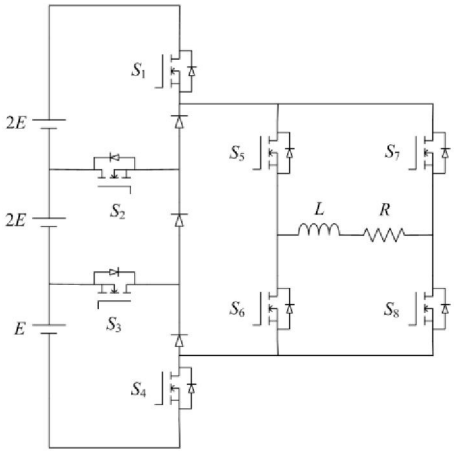


**Figure 1. Circuit Design**

**Switching Operation Modes**

Switch configurations can be operated in one of 11 different modes, numbered 0 through 10. The operation for mode 0 is accomplished when all of the switches in Stage A (S1-S4) are conditioned OFF ("0"), and Stage B (S5-S8) is divided into two primary conditions. The first condition is accomplished when the switches paired S5, S8, and S6, S7 are conditioned ON ("1"), and the switches S6, S7 are conditioned OFF ("0"). Switches S6, S7 must be logically conditioned to be ON "1" and switches S5, S8 must be logically conditioned to be OFF "0" in order for mode 0 to exist. In this procedure, the pairing switches are set to freewheel.

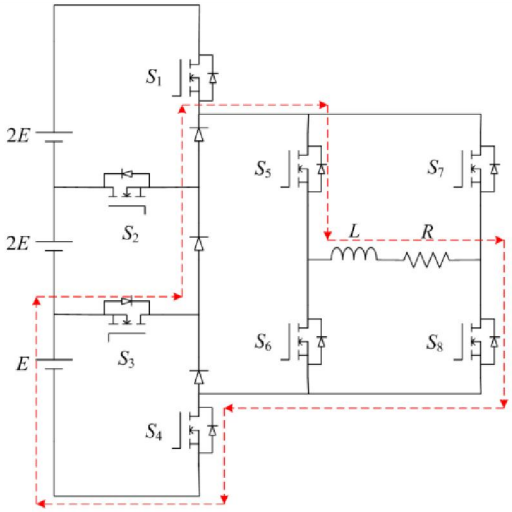


**Figure 2. Operation Mode**

Switches S3, S4 in Stage A (S1-S4) and S5, S8 in Stage B (S5-S8) must be closed in order for mode 1 to operate. Switches S3, S4 in Stage A (S1-S4) and S5, S8 in Stage B (S5-S8) are conditionally "1" or closed, causing Vin to equal E. As a result, the outcome of this operation is evaluated as Vo = E before to the inductive filter.

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**SPWM Gate Switching and Combinational Logic Circuit**

The absolute value of $\frac{1}{2}\lambda$ compared with 5 tiers of triangle waves A, B, C, D, and E with various DC offsetswith a carrier frequency of 10 kHz (Described in Section III.) is used to produce the pulse-width modulation switching in stage A(S1-S4) gates. Table I. outlines the entire switch setup to attain the target level

**TABLE I:** SPWM GATE SWITCHING

| Stage A | | | | Stage B | | | | Vo |
|---|---|---|---|---|---|---|---|---|
| S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 5E |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 4E |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 3E |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 2E |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | E |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | -E |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | -2E |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | -3E |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | -4E |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | -5E |

The output voltage of the inverter circuit will provide the same voltage as the input voltage (before going through the inductive filter), as indicated in Table I. The desired gate switching is achieved by configuring a combinational logic circuit.

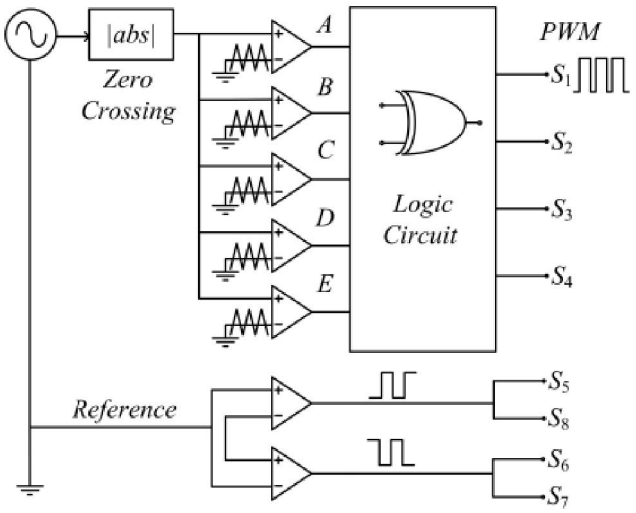


**Figure 3. Switching Configuration and Control Circuit**

The suggested inverter's entire control circuit is shown in Figure 3. The logic circuit layout uses XOR logic gates to provide the desired truth table for the 11-level inverter, as shown by the Boolean equation. The input of the logic circuit is created by comparing the half-positive cycle of a reference sine wave and a triangular carrier waveform, resulting in sinusoidal pulse width modulation (discussed more in Section III).

## III. SIMULATION AND HARMONIC ANALYS

PowerSimTech uses the PSIM software to simulate the design and analysis of the suggested asymmetrical 11-level inverter in real time. Fig. 8 shows the sinusoidal pulse width modulation (SPWM) produced by the comparison of the reference and carrier waves. Combinational logic circuits will be used to further analyse and decode the output SPWM.

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We'll go into more detail about the harmonic distortions in the output waveform of the suggested asymmetrical 11-level inverter architecture. Table II lists the simulation parameters for the suggested inverter circuit.

**TABLE II:** SIMULATION PARAMETER

| Device | Units |
|---|---|
| DC input E | 1V |
| DC input 2E | 2V |
| Inductive Filter | 2mH |
| Load Resistor | 12Ω |
| Reference AC Peak Amplitude | 10V |
| Reference AC Frequency | 50Hz |
| Carrier Triangular Vpp | 2V |
| Carrier Triangular Frequency | 9kHz |
| Carrier Duty Cycle | 0.5 |
| DC Offset Carrier A | 0V |
| DC Offset Carrier B | 2V |
| DC Offset Carrier C | 4V |
| DC Offset Carrier D | 6V |
| DC Offset Carrier E | 8V |
| Print Time | 0.02s |

The sine wave reference is compared to five triangular carriers with various DC offset values (described in Table III) in order to achieve sinusoidal pulse width modulation (SPWM). The offsets value and Vpp are configured to adjust the reference sine waveform half positive cycle with the frequency of each carrier being 10 kHz. The sinusoidal pulse width modulation result for carrier waveforms A, B, C, D, and E.

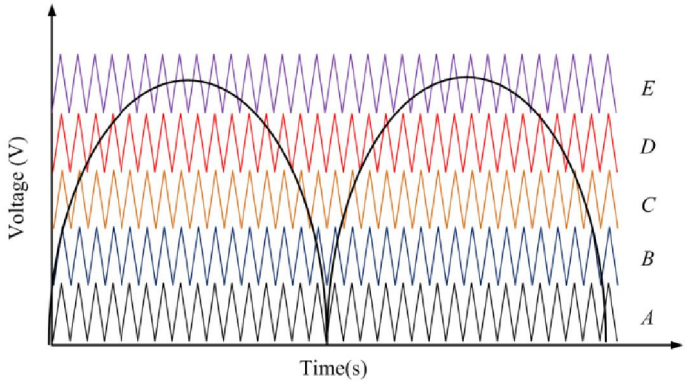


**Figure 9. Triangular Wave 10kHz Comparison with Absolute Value of 1 2 λ Sine Wave 50Hz (Triangular Wave Frequency are not up to Scale)**

## V: MATLAB SIMULATION & RESULTS

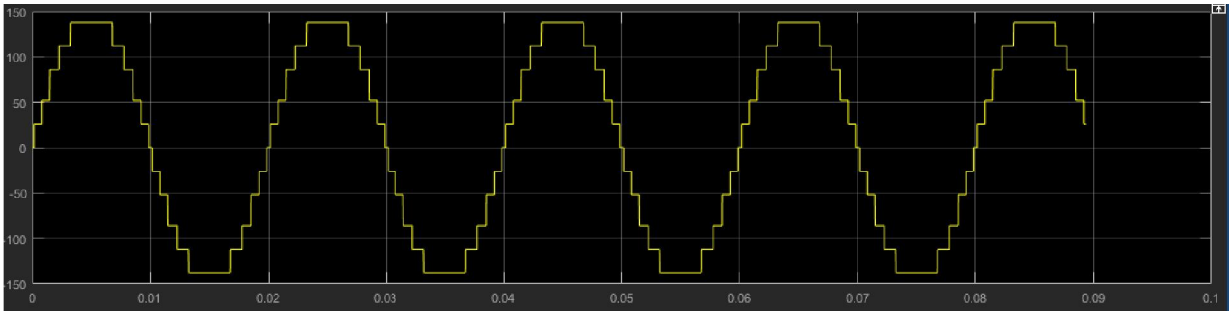


**Figure 10. Scope 1 of 11 Level Inverter**

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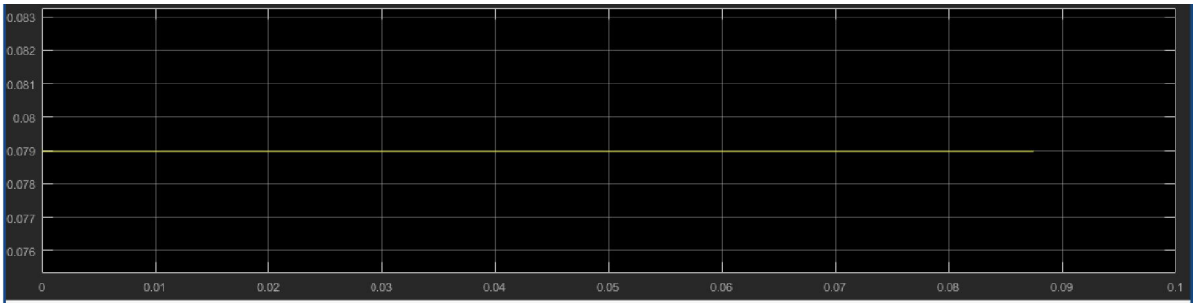


**Figure 11. Current Supply**

**Figure. 10** illustrates how the fundamental half-wave SPWM is used to create an 11-level input SPWM for switches at Stage A (S1-S4), which is then decoded using combinational logic circuits to produce the output stated in the switching configuration and control circuit.

## VI: CONCLUSION

The major topic of this paper is the asymmetrical 11-level inverter design that has been suggested. Compared to the restrictions of typical multilayer inverter topologies (such as flying capacitor and diode clamp), which deal with inverter size and switch count The 11-level asymmetrical inverter employs fewer gate switches to support more n-levels. The grid-tied utility-scale PV system applications are the main emphasis of the proposed design. Adjustments for the proposed design's suitability for its intended use, the number of component switches employed, and the design's adaptability to the output levels generated are all given careful consideration.For PV installations, the planned inverter architecture is altered. A specific DC power generator with values that are maxed out by the maximum power point tracker will be produced by photovoltaic cells, producing 97. Later, the inverter would be powered by a DC input to produce a multilayer AC output.

The THD value for this design, as mentioned in Section III, is 1.19%, which is within the acceptable range of IEEE standards for harmonic voltage limits for power producers (public utilities or co-generators) at 2.3 - 69 kV, 2.5% for 69 - 138 kV, and 1.5% for 138 kV

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## BIOGRAPHY

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