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VLSI Design of Approximate Baugh-Wooley Multiplier for Image Edge Computing

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Abstract: *A sort of digital circuit used to multiply two binary values is called a Baugh-Wooley multiplier. It is renowned for being more effective than other kinds of multipliers in terms of speed and gate count. You would normally start by creating a simple version of the circuit utilizing logic gates like AND gates, XOR gates, and half adders to simulate the Baugh-Wooley multiplier. The design would then be optimized utilizing methods like parallel processing, pipelining, and optimization algorithms to lower the overall gate count and boost the functionality of the circuit. Because of this, estimating a Baugh-Wooley multiplier would require a thorough knowledge of these elements as well as the specifications of the application. Verilog HDL is used to implement this design, and Modelsim 6.4 c is used to simulate it. The synthesis process tool from Xilinx measures performance.*

Keywords: Approximate computing, Edge detection, multiplying circuits

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