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Implementation of Low Power VLSI Design for Various Applications

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Abstract: *In the electronics industry of today, low power has become a major issue. For the design of VLSI chips, power dissipation has taken on equal importance to performance and area. Due to increasing complexity with smaller technology, minimising power consumption and overall power management on chip are the main difficulties below 100nm. Due to the requirement to lower package costs and increase battery life, power optimisation is crucial for many systems. In low power VLSI designs, leakage current also has a significant impact on power management. An growing portion of integrated circuits' overall power dissipation is being accounted for by leakage current. This essay discusses numerous power management approaches, methodologies, and tactics for low power circuits and systems. Also mentioned are potential obstacles to designing low-power, high-performance circuits.*

Keywords: VLSI, Low Power, CMOS, CAD and PSO

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