IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 2, Issue 2, July 2022
Impact Factor: 6.252

Optimized DMA Controller for Soc Interconnections using AMBA

Naval Kishor Sharma[1] and Ritu Juneja[2]
Research Scholar, Department of Electronics & Communication Engineering[1]
Assistant Professor, Department of Electronics & Communication Engineering[2]
School of Engineering & Technology, Bahadurgarh, Haryana, India

Abstract: *In this work, the design and implementation of an AMBA based advanced DMA controller is proposed. The DMAC has 6 channels which support hardware triggers, linking operation and channel chaining transfer and provides three dimensions transmission by parameter sets to improve the real-time processing capability, so as to perform data block moving, data sorting and sub-frame extraction of various data structures. All channels can also be used for channel chaining transfer triggered automatically by Interrupt and Error module. The channel chaining capability for the DMAC allows the completion of a DMAC channel transfer to trigger another DMAC channel transfer.*

Keywords: AMBA, BUS, ARB BUS, TX-FIFO, RX-FIFO, IP INTERFACE

REFERENCES

[1]. Guoliang Ma, Hu He , "Design And Implementation Of And Advanced DMA controller On Amba-Based SoC", ASIC, 2009. ASICON '09. IEEE 8th International Conference on Digital Object, Page(s): 419 – 422

[2]. A. Olugbon, S. Khawam, T. Arslan, I. Nousias, I. Lindsay, "An AMBAAHB-based reconfigurable SoC architecture using multiplicity of dedicated flybyDMA blocks", Design Automation Conference, 2005. Proceedings of the ASPDAC2005. Asia and South Pacific, Volume: 2,Year: 2005 , Page(s).1256 – 1259

[3]. S. Hessel, D. Szczesny, F. Bruns, A. Bilgic, Hausner, J. Vehicular,"Architectural analysis of a Smart DMA Controller for Protocol StackAcceleration in LTE terminals",Technology Conference Fall (VTC 2010-Fall),2010 IEEE 72nd Digital Object, Page(s). 1 – 5

[4]. Jaehoon Song, Piljae Min, Hyunbean Yi, "Design of Test AccessMechanism for AMBA-Based System-on-a-Chip",Sungju Park VLSI TestSymposium, 2007. 25th IEEE , Page(s).375 – 380

[5]. Hang Yuan, Hongyi Chen, "An improved DMA controller for high speeddata transfer in MPU based SOC",GuoqiangBai Solid-State and Integrated Circuits Technology, 2004. Proceedings. 7th International Conference onVolume: 2 Digital Object, Page(s). 1372 – 1375

[6]. LufengQiao, "Design of DMA controller for multichannel PCI bus frame engine and data link manager",Zhigong Wang Communications, Circuits and Systems and West Sino Expositions, IEEE 2002 International Conferenceon Volume: 2 Digital Object,Page(s). 1481 – 1485.

[7]. D, Szczesny, S. Hessel, S. Traboulsi, "Optimizing the Processing Performance of a Smart DMA Controller for LTE Terminals",Bilgic, A. Embedded and Real-Time Computing Systems and Applications (RTCSA),2010 IEEE 16th International Conference on Digital Object , Page(s). 309-315

[8]. Chia-Hao Yu, Chung-Kai Liu, Chih-Heng Kang, Tsun-Hsien Wang, Chih- ChienShen, "An Efficient DMA Controller for Multimedia Application in MPU Based SOC", Shau-Yin Tseng Multimedia and Expo, 2007 IEEEInternational Conference on, Page(s). 80 – 83.

[9]. Prokin, "DMA transfer method for wide-range speed and frequency measurement", M.Instrumentation and Measurement, IEEE Transactions Volume: 42 , Issue: 4 , Page(s). 842 – 846.

[10]. Tai-Yi Huang. Liu, J.W.-S., "A method for bounding the effect of DMA I/O interference on program execution time", Hull, D.Real-Time Systems Symposium, 1996., 17th IEEE , Page(s). 275 – 285

[11]. S. Osborne, A.T. Erdogan, T. Arslan, "Bus encoding architecture for low-power implementation of an AMBA-based SoCplatform",Robinson, .Computers and Digital Techniques, IEEE Proceedings- Volume: 149 , Issue: 4 , Page(s). 152 – 156

IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 2, Issue 2, July 2022
Impact Factor: 6.252

[12]. M. Pockrandt, P. Herber, "Model checking a System C/TLM design of the AMBA AHB protocol", Glesner, S.Embedded Systems for Real-Time Multimedia (ESTIMedia), 2011 9th IEEE Symposium on, Page(s). 66 – 75

[13]. Yi-Ting Lin, Chien-Chou Wang, "AMBA AHB bus potocol checker with efficient debugging mechanism",Ing-Jer Huang Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on , Page(s). 928 – 93

[14]. M. Dubois, Y. Savaria, "A generic AHB bus for implementing high- speed locally synchronous islands",Bois, G.Southeast Con, 2005. Proceedings. IEEE , Page(s). 11 – 16

[15]. C. Toal, S. Sezer, "A pipelined SoPC architecture for 2.5 Gbps network processing",Xing Yu Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on , Page(s), 271 – 272

[16]. S. Sezer, C. Toal, "A pipelined SoPC architecture for data link layer protocol processing",Xing Yu SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip] , Page(s). 277 – 278

[17]. C. Toal, "A 32-bit SoPC implementation of a P5,Sezer", S.Computers and Communication, 2003. (ISCC 2003). Proceedings. Eighth IEEE International Symposium on ,Volume 1, Page(s). 504 – 507

[18]. M. Prokin, "DMA transfer method for wide-range speed and frequency measurementt", Instrumentation and Measurement,IEEETransactions,Volume: 42 , Issue: 4 1993 , Page(s).842 – 846

[19]. AN2548 Application note. http://www.st.com.

[20]. AMBA Specification (Rev 2.0). http://www.arm.com.

[21]. TMS320DM643x DMP EDMA3 User's Guide. SPRU987, January 2007.