IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 2, Issue 3, May 2022
Impact Factor: 6.252

A Multibit Storage Element for Power Minimization in Sequential Logic System

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Abstract: *Power consumption is an important issue in modern high frequency and low power VLSI design. In modern VLSI designs, power consumed by clocking is taken as a major part of the design. The storage elements of designer considerations are Latches and flip flops. One way to boost the flip-flop performance is to combine the clock pulse given to MBFFs. The multi-bit flip-flop is configured by a single clock pulse thereby supporting the same functionality as that of two Single bit Flip-Flops. In the proposed work, the result of the power dissipation is compared with that of the conventional D Flip-Flops. The Sequential logic system is coded using Verilog using Vivado design suite. Simulator and it has been concluded from the comparison that the clock buffer, the number of flip-flops used, by using MBFFS..*

Keywords: Flip-Flops, Multi-bit Flip-Flop, Power Dissipation, Clock Gating, Low Power Techniques

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