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Deep Learning-Based Number Recognition in Verilog

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Abstract: *Network convolutional neural networks (CNNs) are utilized in image and video categorization, recommendation systems, and NLP. These networks are driven by complex connections in animals' visual processing systems. Regardless of how effective CNNs are, training them is challenging because of the storage and computational costs.Data from the CNN model was removed in order to resolve these difficulties. Data volume and computing efficiency are both optimized by this strategy. The study's novel FPGA-based handwriting recognition system can identify MNIST digit sets using CNN. It is feasible to use the hardware design for picture cropping, activation, pooling, pipeline processing, and multiple convolution kernels. Through the utilization of hardware circuits' parallel computation, the MNIST detection approach enhances processing performance. This Verilog HDL-based Altera DE2 FPGA development board is a work of art. Among the image processing techniques included in the hardware design study are cropping, convolution, activation functions, pooling, and the simultaneous processing of several convolution kernels. This study effectively uses VLSI CNN to recognize handwritten numbers. Space efficiency, processing speed, accuracy of classification, and power consumption are some of the criteria. In this research, we present novel approaches to hardware design that enhance MNIST detection and make real-time image recognition possible.*

Keywords: Convolution Neural Networks (CNNs), VERILOG, FPGA, Hand-written number recognition

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