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VLSI Design and Implementation of Multipliers for DSP Applications

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Abstract: *A multiplier is a critical building block found in processors, embedded systems, VLSI applications, application specific integrated circuits, and most DSP applications. Speed, area, and power are the three primary thrust characteristics in VLSI design. Low power and high speed is the desirable characteristic in many applications that can extend the battery's life expectancy and increase the frequency of operation. The goal of this project is to design, implement and analyse the performance of array multipliers, booth multipliers, Wallace tree multipliers, and modified booth multipliers. In this work multipliers with different bit widths are implemented on Spartan 3E FPGA and their performances are analysed. Among these architectures Wallace tree multiplier provides higher speed of operation and consumes lesser power.*

Keywords: Wallace tree, Array, Booth algorithm, Spartan 3E FPGA, Xilinx ISE 14.7 Design Suite, Speed, delay, power

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