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Designing 10T SRAM for noise and Leakage Power Reduction using Stack Transistor Technique – A Review

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Abstract: *The SRAM Semiconductor memory, utilize a bistable latch circuit to store logic 1 or 0 data. It differs from dynamic RAM (DRAM) which requires a periodic refresh operation to store logical data. SRAM power consumption varies with operating frequency, i.e., at higher frequencies, it consumes very high power, similar to DRAM. Because the cache included in the microprocessor required high-speed memory, SRAM can be used in the microprocessor for this purpose. DRAM is often used in processor main memory, where density is more important than speed. SRAM as well used in industrial, scientific electronics, and automotive subsystems. In this paper, the SRAM investigation report was studied to develop a new SRAM design for low power consumption.*

Keywords: Static Random Access Memory (SRAM), Stability, Power Consumption, Read Write modes

REFERENCES

[1]. T. Suzuki, H. Yamauchi, Y. Yamagami, K. Satomi and H. Akamatsu, "A Stable 2-Port SRAM Cell Design Against Simultaneously Read/Write-Disturbed Accesses," IEEE Journal of Solid-State Circuits, vol. 43, no. 9, pp. 2109-2119, Sept. 2008.
[2]. N. Verma, "Ultra-Low-Power SRAM Design in High Variability Advanced CMOS," May 2009.
[3]. N. Rahman and B. P. Singh, "Design and Verification of Low Power SRAM using 8T SRAM Cell Approach," International Journal of Computer Applications, vol. 67, no. 18, pp. 11-15, April 2013.
[4]. A. Tajalli and Y. Leblebici, "Subthreshold SCL for ultra-low-power SRAM and low-activity-rate digital systems," in Proceedings of ESSCIRC, Athens, Greece, Sept. 2009.
[5]. S. Birla, N. K. Shukla, K. Rathi, R. K. Singh and M. Pattanaik, "Analysis of 8T SRAM Cell at Various Process Corners at 65 nm Process Technology," Circuits and Systems, vol. 2, no. 4, pp. 326-329, Oct. 2011.
[6]. V. Venmathi and C. Vivekanandan, "A SRAM Memory Cell Design in FPGA," International Journal of Computer Applications, vol. 71, no. 1, pp. 23-26, June 2013.
[7]. P. V. Kiran and A. Mondal, "Modelling and Simulation of Low Power SRAM Cell with Improved Read Speed at 45nm Technology," American International Journal of Research in Science, Technology, Engineering & Mathematics, vol. 7, no. 1, pp. 85-89, Aug. 2014.
[8]. D. N. Mandal, N. P. Mohapatra, R. Prasad and A. Singh, "Analysis and Design of Low Voltage Low Power Dynamic Comparator with Reduced Delay and Power," International Journal of Engineering Research and General Science, vol. 2, no. 3, pp. 239-246, May 2014.
[9]. P. Sanvale, N. Gupta, V. Neema, A. P. Shah and S. K. Vishvakarma, "An improved read-assist energy efficient single ended P-P-N based 10T SRAM cell for wireless sensor network," Microelectronics Journal, vol. 92, April 2019.
[10]. S. Saun and H. Kumar, "Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization," vol. 561, no. 1, pp. 1-9, 2019.
[11]. S. Ahmad, M. K. Gupta, N. Alam and M. Hasan, "Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell," IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 24, no. 8, pp. 2634-2642, Aug. 2016.
[12]. L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini and W. Haensch, "Stable SRAM cell design for the 32 nm node and

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beyond," Digest of Technical Papers Symposium on VLSI Technology, pp. 128-129, 2005.