IJARSCT



International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)

Volume 2, Issue 1, April 2022

Review on Vedic Mathematics

Raksha¹, Shravan Ravi Shetty², Shravan Kumar³, Monisha M⁴

Students, Department of Computer Science and Engineering Alva's Institute of Engineering and Technology, Tenkamijar, Karnataka, India mijarrakshaacharya1102@gmail.com¹, shravan2003ravi@gmail.com², shravanshetty02@gmail.com³, monishamanjunath10@gmail.com⁴

Abstract: Vedic mathematics is claimed by its founder to be a present given to the current by the traditional sages of Asian countries, although there is no historical evidence that for this claim. It is a system for limited computation and polynomial calculation which his easier and more convenient than the corresponding algorithm in present math. Vedic Mathematics is the ancient technique used to mentally solve add, subtract, and multiply. In this era of digitization, engineers are working to enlarge digital circuits' speed while reducing the size and energy consumed. Arithmetic operations are the basic units of all the digital circuitry and hence rewriting these units increases the efficiency of the entire digital design. By using this technique answer any question in one line. Vedic Mathematics doesn't get its due importance; it is a fantastic method. Vedic Mathematics is a great technique to master calculations, being more adequate and authentic. In this survey paper, we will come up with reader. An overview of Vedic mathematics, as well as some progressive works in space.

Keywords: Vedic Mathematics, Sutras, Nikhilam sutra, RSA algorithm, Urdhva-tiryagbhyam, Vedic multiplier.

REFERENCES

- [1]. Himanshu Thapliyal, "A Time-Area- Power Efficient Multiplier and Square Architecture Based On Ancient Indian Vedic Mathematics".
- [2]. Mr Shripad Kulkarni, "Discrete Fourier Transform by Vedic mathematics".
- [3]. HimanshuThapliyal, "VLSI Implemen
- [4]. -tation of RSA Encryption System Using Ancient Indian Vedic Mathematics".
- [5]. William Stallings, "Cryptographyand Nework Security", Third Edition, Pearson Education, 2003
- [6]. Poornima M, Shivaraj Kumar Patil, "Implementation of Multiplier using Vedic Algorithm", International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-6, May 2013.
- [7]. D. Kishore Kumar, A. Rajakumari, "Modified Architecture of Vedic Multiplier for High speed applications", International Journal of Engineering Research and Technology (IJERT), ISSN: 2278-0181, vol. 1 Issue 6, August 2012
- [8]. Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho. "Multiplier design based on ancient Indian Vedic Mathematics", 2008 International SoC Design Conference, 2008
- [9]. Nikhil R. Mistri, S. B. Somani, V. V. Shete. "Design and comparison of multiplier using vedic mathematics", 2016 International Conference on Inventive Computation Technologies (ICICT), 2016
- [10]. ShamainAkhter, "VHDL Implementation of Fast NxN Multiplier based on Vedic Mathematics", Jaypee Institute of Information Technology University, Noida, 201307op, India, IEEE 2007.
- [11]. Himanshu Thapliyal and M.B Srinivas, "High-Speed Efficient N by N Bit parallel Hierarchical Overlay Multiplier Architecture Based", pp.225-228,Dec. 2004.

DOI: 10.48175/IJARSCT-3127